PROCEEDINGS OF SCIENCE

IBL – ATLAS Pixel Upgrade

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The upgrade of the ATLAS Detector will progress through different phases as we prepare for the transition to the sLHC. The first upgrade for the innermost tracker, the Pixel Detector, will be the IBL, an additional insertable B-Layer. This layer will be included into the Pixel Detector to compensate for the degradation of the B-layer, the one currently closest to the beam pipe. The IBL project consists of many R&D projects covering electronics, sensors, mechanics, readout, etc. It will be the first step of the upgrade and will address already some of the aspects to be covered for a sLHC tracker detector. In this paper we discuss the different aspects of developing a more radiation hard Pixel Detector layer which will be placed closer to the interaction point, and we provide an overview of the status of the project.

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1. Introduction

The ATLAS [1] Pixel Detector [2] (see Fig. 1) is the innermost sub-detector of ATLAS and therefore the one suffering the most from the severe radiation environment induced by the LHC in ATLAS. Due to the proximity of the B-layer sensors (the layer closest to the beam pipe) to the interaction point, an upgrade of the whole innermost layer is necessary after about 5 years of operation, which coincides with the timing of the LHC phase-I upgrade. Given the anticipated luminosity profile and the installation foreseen in 2014 the current B-layer will still participate in the data taking, but its efficiency will decrease with further time. Taking into account the time needed to replace the existing B-Layer would be more than a year due to the activation of the material which needs to be deinstalled the only possible solution to provide an additional space point close to the interaction point is to introduce an additional layer to the existing detector. The new insertable B-Layer (IBL) [3] is currently under development and all items which are addressed here are still preliminary. The general idea of how to realize the new layer will be described here, since for some items several options need still to be explored while for others the details will certainly change in the course of the development process.

The new layer should be realized using new technologies; chips developed using current technology, and updated off-detector electronics using modern components. It must withstand the irradiation until the end of LHC. A study for the 1 MeV equivalent fluence for different radii is given in Fig. 2.

The IBL needs to be integrated as a part of the existing Pixel Detector. Therefore it will be the 4th Pixel layer and must be compatible with the control system and operation of the existing detector. Since almost all of the addressed items are still under development, this paper outlines the most important components and describes the basic idea for the development.

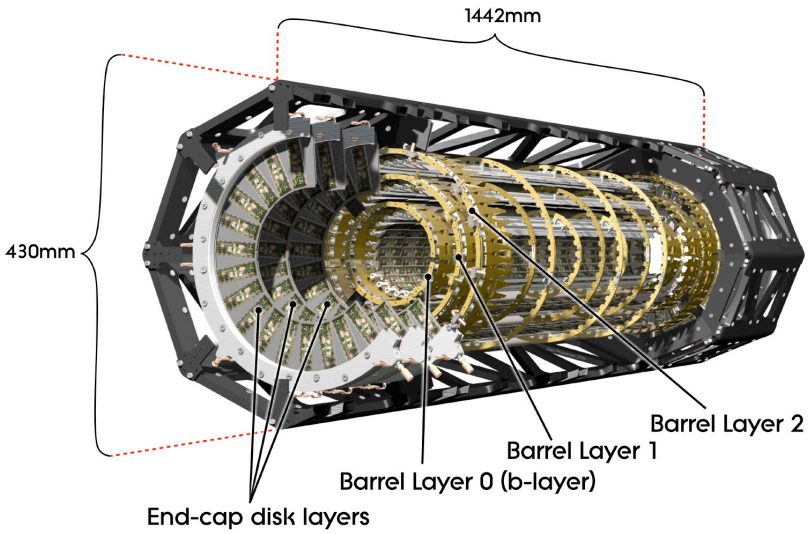


Figure 1: The current ATLAS Pixel Detector

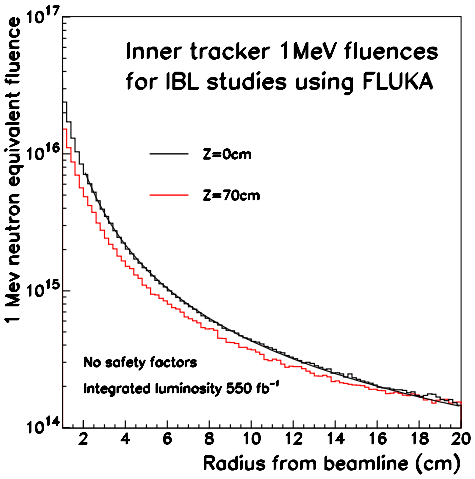


Figure 2: 1MeV fluences versus radius R from the beam line, for the cases z=0 cm and z=70 cm [4]. The parameterization is $\Phi(r) = (\frac{2.9}{r^2} + \frac{0.14}{r}) \cdot 10^{16}$

2. Layout

The baseline for the geometry of the IBL is a barrel layer consisting of 14 staves. Each of these will have 16 modules, which each consist of two front-end chips bonded to a sensor. This can be either two independent sensor tiles or one common sensor tile (see later). The staves are tilted by 14° to guarantee an overlap region in Φ. The inner radius of the IBL will be ~ 32 mm, which can only be realized with a beam pipe inner radius of 25 mm. The outer radius of the IBL will be ~ 38.3 mm, which leaves enough clearance to the current innermost Pixel Detector layer. A section of the baseline design is sketched in Fig. 3. The sensor surface of the IBL will only ~ 0.2 m^2 and located at a radius of ~ 33 mm from the interaction point. The dimensions for the layout of the IBL are summarized in Table 1. The total material budget sums up to a radiation length of $X/X_0 \approx 1.5\%$.

Staves	14
Length of stave	80 cm
Width of stave	2 cm
Inner radius	3.2 cm
Outer radius	3.835 cm
Tilt angle	14°

Table 1: Planned dimensions (current status).

3. Electronics

The front-end chip which is foreseen for the IBL is the FE-I4 chip [5] [6]. It serves 26 880

pixels arranged in 80 columns (250 μm pitch) by 336 rows (50 μm pitch). It is designed in a 130 nm feature size bulk CMOS process. The chips are connected to the sensors via bump bonding using DC coupling and collecting negative charges.

Each FE-I4 pixel contains an independently running amplification stage with adjustable signal shaping, followed by a discriminator with an independently adjustable threshold. The chip keeps track of the threshold crossing time of each discriminator as well as the time over threshold (TOT) with 4-bit resolution, in counts of an externally supplied clock, nominally 40 MHz. Information from all hits triggering the discriminator is kept in the chip for a latency interval, programmable up to 256 cycles of the external clock. Within this latency interval, the information can be retrieved by supplying an external trigger. The data output is transmitted on a serial line using a current-balanced pair (similar to LVDS). The primary output mode is 8b/10b encoded with 160 Mb/s rate. The FE-I4 is controlled by a serial LVDS input synchronized to the external clock. No additional I/O connections are required for regular operation, but several others are provided for testing. The basic specifications of the FE-I4 are listed in Table 2. The first iteration of chips will provide capabilities to test for different powering options. A DC-DC converter is integrated as well as serial powering regulators. With the first submission of chips expected to be received back in 2010, testing of these options will help to choose the powering scheme for the on-detector components.

4. Sensors

The functional module outline for the IBL can be satisfied with either single chip assemblies that have very narrow sensor edges (Fig. 4(a)), or two-chip assemblies with slightly larger edges of insensitive material (Fig. 4(b)). Since there is no shingling in the Z direction of the IBL modules, due to the extreme radial space constraints, these options result in slightly different active coverage. For single-chip (two-chip) assemblies the nominal active coverage for particles normal to the beam

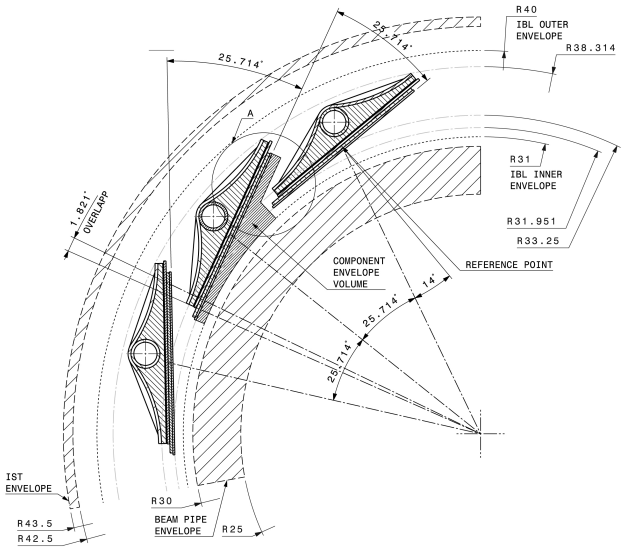


Figure 3: Radial dimensions in the IBL baseline layout.

Item	Value	Units
Pixel size	50×250	μm^2
Maximum charge	$100,000$	e^-
Pixel array size	80×336	Col $\times$ Row
Hit-trigger association resolution	25	ns
Same pixel two-hit discrimination (time)	400	ns
Single channel ENC sigma (400 fF)	< 300	e^-
Tuned threshold dispersion	< 100	e^-
ADC method	Time Over Threshold (TOT)	
Radiation tolerance (specs met at this dose)	250	MRad
Average hit rate with $< 1\%$ data loss	400	MHz/cm^2
Nominal operation voltage for main chip	$1.2 - 1.5$	V
Nominal currrent for main chip	~ 0.6	A

Table 2: Basic specifications for FE-I4.

is 98.8% (97.4%) of the full solid angle. A gap of 100 μm (200 μm) between single-chip (two-chip) assemblies has been assumed in order to take into account the need for higher bias voltages in case of the 2-chip (planar) sensors. A 200 μm gap is considered sufficient for adding a polyimide insulation film, if necessary.

There are three candidate sensor technologies (planar silicon, diamond, 3D silicon) that may meet the IBL requirements with their respective trade-offs. The module format required for the IBL can be satisfied with any of these technologies, thus permitting the overall design to be somewhat independent. However, the two parameters operating temperature and bias voltage are different for each technology and have serious implications on the rest of the system.

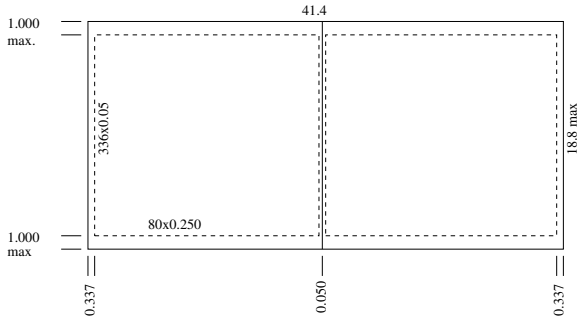
Planar sensors require the lowest temperature and highest bias voltage within the three sensor options, but have very well understood manufacturing sources, mechanical properties, are available at relatively low cost, and offer a high yield.

The 3-D sensors require the lowest bias voltage, an intermediate operating temperature, and achieve the highest geometrical acceptance due to their active edges, but their manufacturability with high yield and good uniformity must be demonstrated.

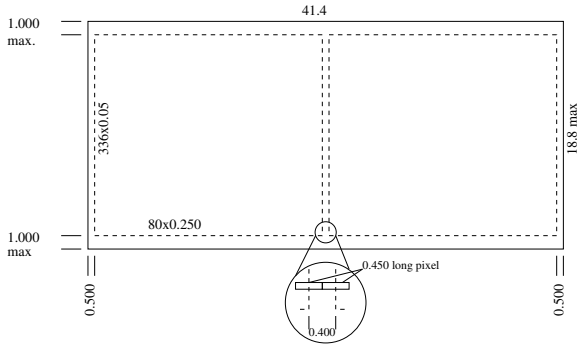
Diamond sensors require the least cooling and have similar bias voltage requirements as planar sensors, but their manufacturability with high yield, at moderate cost, and with good uniformity have also still to be demonstrated.

For all three sensor types the charge collection with increasing dose has to be quantified as a function of operational conditions. While the charge collection efficiency does not directly depend on temperature, the power and leakage current do which in turn affects the charge collection efficiency. All these studies are under investigation for the different kinds of sensors and the specific description of the sensor types can be found in Refs. [7], [8], and [9].

Charge collection is not a decisive figure of merit by itself. A significant factor in choosing a sensor technology will be the electrical performance with the FE-I4 chip. In particular, the minimum stable operating threshold is considered to be the decisive parameter that determines



(a) IBL Envelope for 2 single-chip 3-D modules. All numbers are given in mm.



(b) IBL 2-chip planar sensor tile module. All numbers are given in mm.

Figure 4: Module format layouts as been foreseen for different sensor types.

the required charge at the sensor's end of life, and not the single pixel white noise. However, the minimum stable threshold can not be determined with confidence from simulations, because it depends on coherent effects within the chip and sensor assembly. An analog simulation of the full system has not been technically feasible, and the exact impedance network presented by an irradiated, bump bonded sensor is not well known. Measurements on bump-bonded assemblies will provide critical input to a sensor technology choice once the FE-I4 chip is available.

5. Mechanics

The mechanical structure which is under development for the IBL is made from a carbon-carbon carrier filled with carbon foam and containing a cooling pipe. Several design options are under investigation. The mechanical properties of stiffness, stability under thermal stress, and low mass must be optimized in conjunction with the thermal behavior, which is important for controlling the temperature of the modules (sensor and electronics). The cooling fluid choice will be made between C_3F_8, as used in the current silicon detectors in ATLAS and therefore well known in handling and behavior, and CO_2 which will be an option for upgraded detectors and is already used in LHCb. Different layout options are under investigation. Prototypes of different solutions have been built or are under construction to perform measurements for comparison with simulation

Figure 5: Prototype of a full carbon fibre homogeneous stave. Two carbon fibre pipes, which are fully qualified for the IBL usage have been integrated into the carbon foam.

results. Heat load and cooling measurements, mechanical stress tests, etc., are to be performed. Options in the design phase are single and double pipe solutions, usage of light and heavy foam, pipe material choices between carbon fibre and titanium. Fig. 5 shows the prototype of the full carbon stave equipped with two 3 mm inner diameter carbon fibre pipes.

6. Readout

The IBL will be operated as part of the current Pixel Detector and therefore the detector steering and control as well as the readout must be compatible with the present detectors. The communication with the IBL will be performed via an optical transmission line which is similar to that currently used by the Pixel Detector. The down link to the detector will be operated at 40 Mb/s. Clock and commands are encoded into one bi-phase-mark-encoded stream which is sent to the detector. The clock and data will be decoded on-detector on the optoboard, which serves as the optical-electrical interface. The clock and the data signals per module are transferred via electrical lines to the detector modules. The output data is foreseen to be transmitted at 160 Mb/s. The front-end chip sends 8b/10b encoded data via an electrical line to the optoboard from where it is transmitted via optical fibres to the off-detector electronics.

In the counting room the electronics need to be upgraded as well, as the readout speed and scheme is different from the present system. The two card types, the Read Out Driver (ROD) and the Back of Crate card (BOC), are paired together in VME crates. The ROD serves as control machine and the BOC as optical interface. The cards are being designed to maintain compatibility with the existing readout electronics, with the additional benefit that the IBL cards may also be used with the present detector, either as spares or to increase the readout bandwidth.

7. Summary

The IBL project was initiated in July 2009 and combines many projects aimed at developing a

4^{th} ATLAS Pixel Detector layer to be installed in 2014. The mechanics will be realized in carbon-carbon and carbon-foam structures (staves) to be set up in a turbine structure with 14 staves around the beam pipe.

The sensor will be chosen from three candidates (planar silicon, 3D silicon, diamond) and will be connected to front-end chips which are currently in the prototype phase (FE-I4). The assembled sensor and chip package will undergo a complete testing and qualification cycle during the decision process.

The on-detector electronics is read out via an optical link terminating in the counting rooms. The off-detector readout hardware needs a new design and development in order to accommodate the higher bandwidth and the different transmission protocols for the IBL.

These recently developed components need to be integrated into the existing ATLAS Pixel Detector as a 4^{th} layer. It will be operated as part of the Pixel Detector and therefore the software for data acquisition and detector control is constrained to fit into the existing software environment.

The scheduled installation date is end of 2014. By then all the components need to be produced and tested individually as well as in a combined system test.

8. Acknowledgements

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