

In-situ Storage Image Sensor for a Vertex Detector at the ILC

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In-situ Storage Image Sensor (ISIS) is a new detector concept being developed by the Linear Collider Flavour Identification collaboration for a future vertex detector at the ILC. ISIS1 was the first prototype and was used to test the operational principles. ISIS2 is the second generation of the family, and is made on a submicron CMOS process to reduce the pixel size. Characterisation of the test structures built along with the main part of the sensor array are reported here, including the readout noise, the cell well-capacity and the fringing-field effects. Preliminary results of the test on the main array are also discussed. The results indicate that ISIS is an extremely promising design for the ILC.

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1. Introduction

In-situ Storage Image Sensor (ISIS) has been developed in the Linear Collider Flavour Identification collaboration (LCFI) for use in a vertex detector at the ILC. The accelerator design foresees 1 ms-long bunch trains at a rate of 5 Hz [1]. The detector occupancy due to background is highest for the inner layer of the vertex detector. For typical detector and machine parameters [2], the integration of all events during the bunch train would make the occupancy in the first layer of the vertex detector too high for reliable pattern recognition. To keep the background to an acceptable level, 20 readouts during the bunch train will be needed for the inner layer sensors. In the ISIS design, this is achieved by storing 20 signal samples within the storage cells during the bunch train (~1 ms) and reading them out in the long gaps in between (~200ms).

The principle of the ISIS is shown in Figure 1. It uses a CCD register to store the raw charge generated by traversing Minimum Ionizing Particles (MIP) in each pixel for consecutive readout. For ILC vertex detector design, the signal charge is collected under a photogate and then shifted every 50 μs to a 20-cell deep linear CCD register *in situ* during the bunch train. After 20 samples have been stored, the charge is shifted out for readout as in a typical CCD and converted to voltage in the 200 ms gap between the bunch trains, avoiding any beam-induced EMI during the bunch train. This is equivalent to 20 complete device readouts during the train and reduces the pixel occupancy to manageable levels.

A 1MHz clock frequency with column parallel readout is sufficient to retrieve all stored charge from the full scale device. This low frequency makes it possible to use longer shaping times and thus to help achieve low readout noise and possibly improve the point resolution of the detector by reduced error in the centroid hit finding.

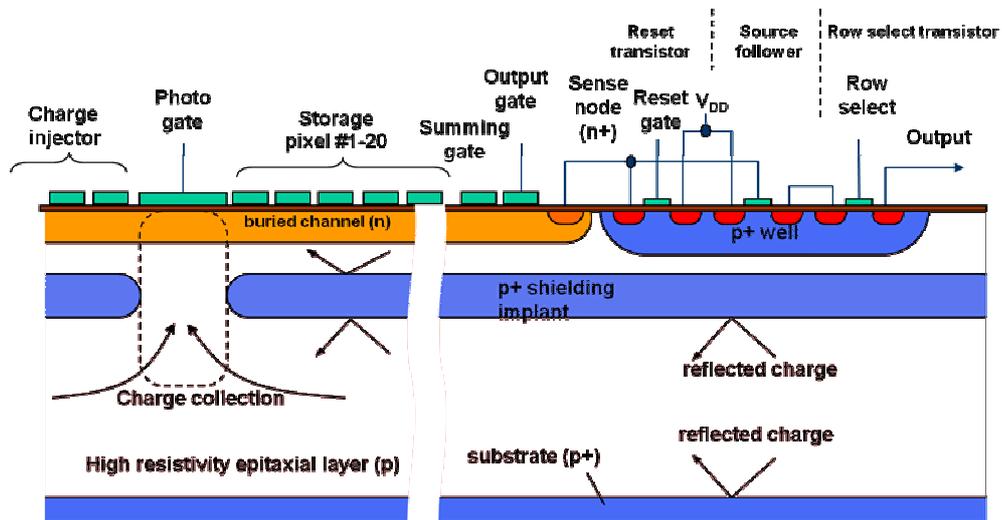


Figure 1 ISIS principle

The LCFI collaboration has designed two generations of ISIS, ISIS1 (a proof-of-principle manufactured by e2V technologies [3]) and ISIS2. ISIS1 has been tested both in the lab and in a beam test with several publications [4][5][6]. A summary will be given here. After the success of ISIS1, ISIS2 was designed and submitted in May 2008, manufactured by Jazz Semiconductors [7]. It is intended to demonstrate integration of a buried channel, low voltage CCD manufactured in CMOS process. A description of the device and some test results will be presented in section 3 and 4.

2. ISIS1

The LCFI collaboration designed the first proof-of-principle device ISIS1 which was manufactured by e2v in their CCD process. The device is an array of 16×16 imaging pixels, each containing a photogate, a 3-phase CCD with 5 storage cells, a reset transistor, a source follower and a row select transistor. The pixels are arranged on $40 \mu\text{m} \times 160 \mu\text{m}$ pitch. There are two variations of the device: with and without deep p-well shielding underneath the register. The devices have been successfully characterised using radioactive sources and in a beam test.

2.1. Beam test

A beam test was performed at DESY (Hamburg) with a 6 GeV/c electron beam. Five ISIS1 devices without p-well were precision-mounted in a stack to form a beam telescope. The readout clock was operated at 2.5 MHz. The integration time for each of the 5 memory cells was 6 ms. The sensors were operated at -20°C . Further details can be found in [4].

2.2. Response on X-ray Source and Charge Shielding by the p-well

The shielding effectiveness of the p-well, a potential barrier at the boundary between p+ and p layer, similar to that in Figure 1, was also studied using the ^{55}Fe radioactive source. The X-rays are converted virtually everywhere in the epitaxial layer, following the usual exponential dependence with absorption length of $30 \mu\text{m}$. Therefore if the p-well works as designed, the charge collected by storage pixels will be different between devices with and without p-well. So the ratio between charges collected by photogate and the storage pixels per unit time was used as a measure of the effectiveness of the p-well. The results show that the p-well can suppress the parasitic charge collection by almost two orders of magnitude, satisfying the requirements for the application. The details can be found in [6]

3. ISIS2 design

After the success of ISIS1, the LCFI collaboration designed and submitted the ISIS2 chip in May 2008. The ISIS2 sensor is intended to demonstrate integration of a buried channel, low voltage CCD with a $0.18 \mu\text{m}$ CMOS process, a step towards satisfying the requirement of a vertex detector at the ILC: $20 \times 20 \mu\text{m}^2$ with 20 storage cells. This pixel size is required to achieve point measurement resolution better than $3.5 \mu\text{m}$ [2]. The technology was not available for a conventional CCD process to make 20 storage cells and readout electronics (3 transistors)

inside a $20 \times 20 \mu\text{m}^2$ area. We therefore focused on a CMOS process. The ISIS2 has 256 rows and 32 columns. Each sensor has 8 different pixel variations.

3.1. Requirements for miniaturisation

In the ISIS2 design the pixel size is $80 \times 10 \mu\text{m}^2$ with twenty storage cells, which represents a major step in miniaturization of the approach. This became possible due to the smaller feature size of the chosen foundry, Jazz Semiconductors. The $0.18 \mu\text{m}$ CMOS process used has been modified to implement a buried n-channel and deep p-implant. This prototype enables the production of ISIS by more industrial methods.

The imaging pixel size is defined by the layout of the charge-collecting photogate since the charge collection occurs independently of the sensor organization above the deep p-implant. The ISIS2 imaging pixel size is $20 \times 40 \mu\text{m}^2$, while the size of associated physical array is $80 \times 10 \mu\text{m}^2$. Figure 2 illustrates the

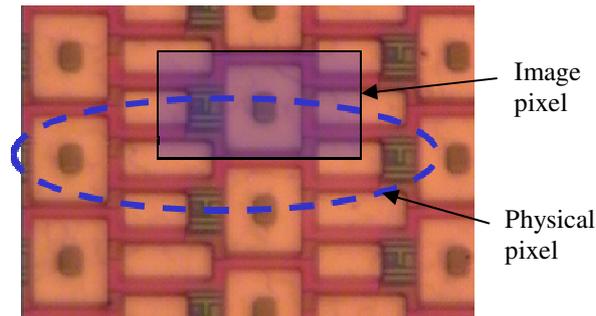


Figure 2 Top view of ISIS2 pixel layout

mapping between imaging pixels and the physical array. In ISIS2 a two-fold repeat was used to connect two staggered rows to one source follower at the end of the column. The total size of the ISIS2 sensor is $5 \times 5 \text{mm}^2$. The device is being evaluated to understand the crucial features of the in-situ charge storage CCD cell manufactured in this CMOS process.

3.2. CCD register in CMOS

In the ISIS2 design, the main challenges arise from the non-overlapping polysilicon gates and the low voltage supply as required by a CMOS process. The nominal 5 V drain voltage implies that the buried channel threshold V_z has to be at least 1 V lower to take into account the threshold of the reset transistor and the process fluctuations. Designing a CCD with such low V_z inevitably limits the amount of stored charge, because the potential barriers to the surface and in between the potential wells cannot be as high as in typical CCDs, where V_z could be in excess of 10 V. The loss of stored charge due to insufficient depth of the potential well depends on the temperature and decreases exponentially as the potential barrier increases. For ISIS2 the goal is to create barriers of 1 V in both directions, which limits the escape of charge to a few electrons per second at room temperature. Simulations with Synopsys TCAD were used to determine the optimal doping profile of the buried channel to achieve the required potential barriers. A particular challenge is to prevent the charge from coming into contact with the surface in the inter-gate gaps. The 5V gate oxide in the $0.18 \mu\text{m}$ process is not very thick, therefore the distance between a gate and the potential peak in depth is almost entirely contained in the silicon. To reduce the influence of the gaps and smooth out the potential, it is necessary to increase that distance. The approach taken in the ISIS2 was to position the peak of the buried

channel implant at a depth of at least 200 nm. This makes the channel potential peak at 200-300 nm, approximately the same as the inter-gate gaps. The full well capacity is estimated at 2000 e-/μm² by design.

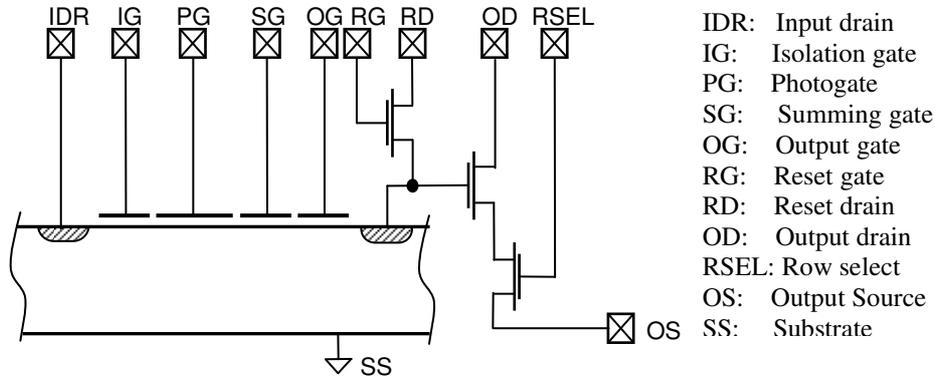


Figure 3 Schematic of the test structure

4. ISIS2 characterisation

Test structures are also included in the design. These are “compact” versions of the pixels used in the main array, but without storage cells. These structures were tested by the collaboration first. Tests are starting now on the main array of the device with some preliminary results available. Both results will be discussed in this section.

4.1. ISIS2 test structure

The schematic of the test structure is shown in Figure 3. For the full pixel used in the main array, there are 20 storage cells between the photogate and the summing gate. With this simple version, many useful measurements have been made, such as the noise and the x-ray response on the node and the fringing field effect.

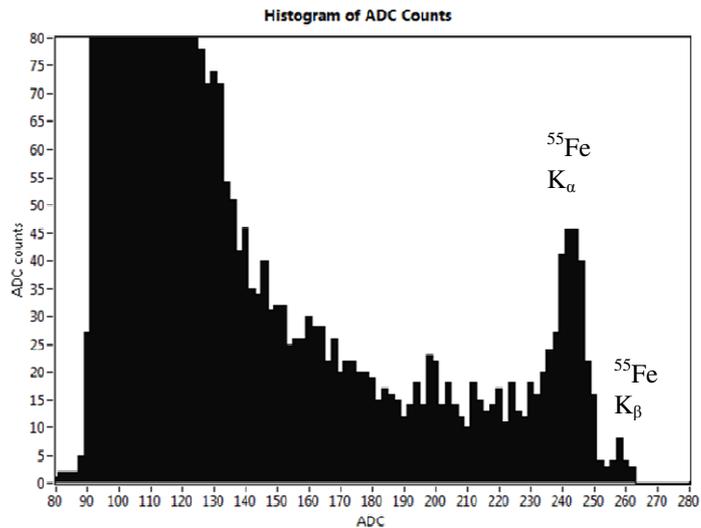


Figure 4 Histogram of X-ray on node

Figure 4 is a

histogram of the ^{55}Fe source direct hits on the node. The risetime is 133 ns and the time interval between correlated double sampling (CDS) is 800ns. With this result, the sensitivity the noise of the node can be calculated. The sensitivity is $24\mu\text{V}/e^-$ and the measured noise is $5.5 e^-$ rms. With this low noise device it is no surprise that a K_{β} peak can be resolved.

As the feature sizes are reduced, the fringing-field effects becomes more profound. A significant effect is the

potential on output gate being influenced by the potential on the output node. During the operation, the potential of the output node is 5V (by reset), and the output gate should be biased to a level such that when the summing gate is high, charge can be held under the summing gate. The effect was investigated as follows. A certain charge was generated under the photogate by a LED flash of a fixed duration on the sensor, and then the bias voltage on photogate (PG) was set low while still keeping the summing gate (SG) and the output gate (OG) voltage high. The signal measured at

this stage is the charge transferred directly to the output node. SG voltage then set low, the charge held by the SG will be transferred to the output node. Repeating the measurement with different OG voltage, the result is shown in Figure 6. In this figure the PG curve means the charge transferred from

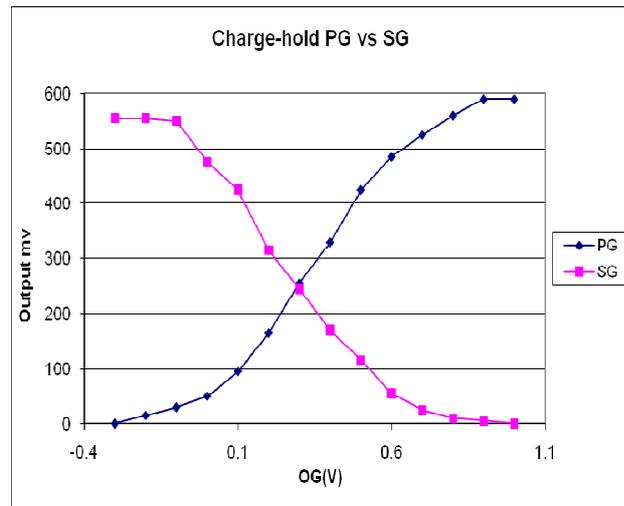


Figure 6 Charge held by PG vs SG with different OG

Charge Capacity vs gate voltage
1X5 μm @0°C

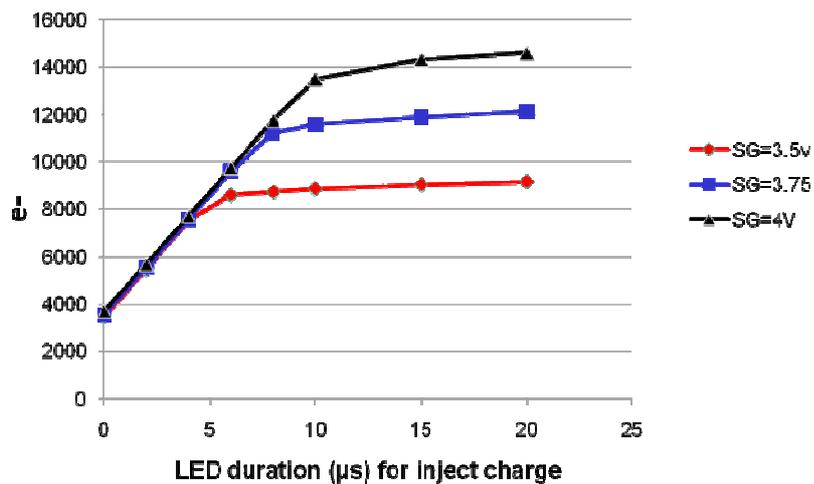


Figure 5 Charge capacity of storage cell

PG directly to the output node and the SG curve means the charge held by SG. As can be seen, the charge cannot be held by the SG when $OG > 1$ V. For a conventional CCD, we would expect the charge to be held by the summing gate when the output gate bias is set above 1 volt.

Although there is no storage cell in the test structure, the full well capacity of the storage cell can also be measured, because the full well capacity of summing gate is the same as that of storage cell. During the measurement, different quantities of charge are generated by illuminating the photogate with a LED pulse of variable duration then transferring the signal charge via summing gate to output node. Because the size of photogate is a few times larger than that of summing gate, it can provide more charge than the summing gate can handle. When summing gate reaches its full well capacity, saturation will be found on output node even though the charges transferred to the summing gate still increases. Of course this saturation will vary with bias voltage of the summing gate. Figure 5 shows the results at a controlled temperature of 0°C . The measured full well capacity is close to the design value.

4.2. Main array

The most interesting part of course is the study of the main array. Some preliminary tests have been done on the storage cells: the behaviour as a buried channel CCD on a CMOS process both with a LED light source and an ^{55}Fe x-ray source.

Figure 7 is a snapshot of the scope when examining the signal on the output node. The LED was fired at the beginning of the sequence. As there are metal layers on top of everywhere except the photogate and the output node, when LED is flashed, a clear LED signal can be detected on the output node while the charge collected by

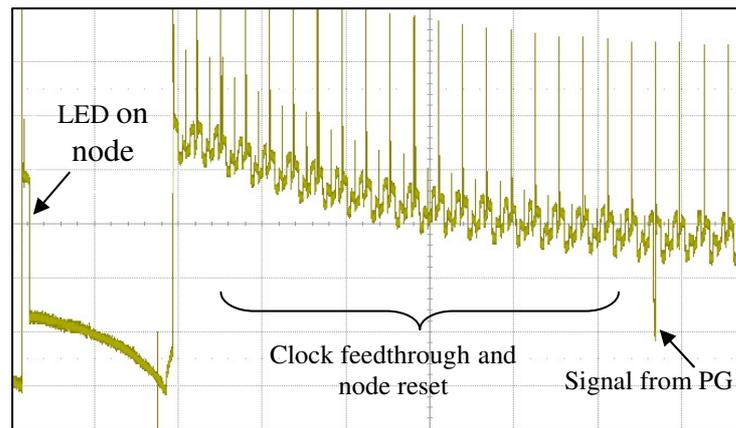


Figure 7 LED signal on main array

the photogate will be detected later after 21 charge transfers through the storage cells. This snapshot clearly indicates both of these signals.

We can also estimate the charge transfer efficiency (CTE) from the ratio between the intensity of LED signal S_{led} and the intensity of the following oversampling signal S_{over} if we assume that the sensor works in the linear range. S_{led} and S_{over} are proportional to the charge transferred to the output node with the sensitivity mentioned above. However the sensitivity is not relevant to the following analysis and can be considered as one, as we only interested the ratio of S_{over}/S_{led} . Suppose the total charge generated by LED on the photogate is T , and

numbering the storage cells 1 to 20 from the cell located closest to the output node, then the charge transferred to each storage cell is:

$$T_i = T \times CTE^{(21-i)}$$

The charge left on the same cell is

$$T_{left,i} = (1 - CTE) \times T_i$$

The left charge on each storage cell will be transferred to the output node at the first oversample. So the total charge on the first oversample is

$$S_{over} = \sum_i^{20} T_{left,i} \times CTE^i = 20 \times T \times CTE^{21} \times (1 - CTE)$$

And

$$S_{led} = T \times CTE^{21}$$

Therefore

$$CTE = 1 - \frac{S_{over}}{20 \times S_{led}}$$

For our case, S_{led} is approximately 300mV; S_{over} is below 50mV, so the CTE should be better than 99%.

In order to further quantify the charge transfer efficiency, the ^{55}Fe source was used. For this test the storage cells were considered as a one-dimensional CCD with 20 pixels. The source was moved on top of the sensor during the integration interval and moved away during the readout period. Figure 8 is the histogram of x-ray on one storage cell. The largest peak is the background noise and the second largest peak is the x-ray signal. The separation between these peaks is a measure of the x-ray signal on that storage cell transferred to the output node. The x-ray signals received by the output node are indicated by the points in Figure 9. For each storage cell, it is:

$$S_i = S_0 \times CTE^i$$

Where S_0 is x-ray signal on the

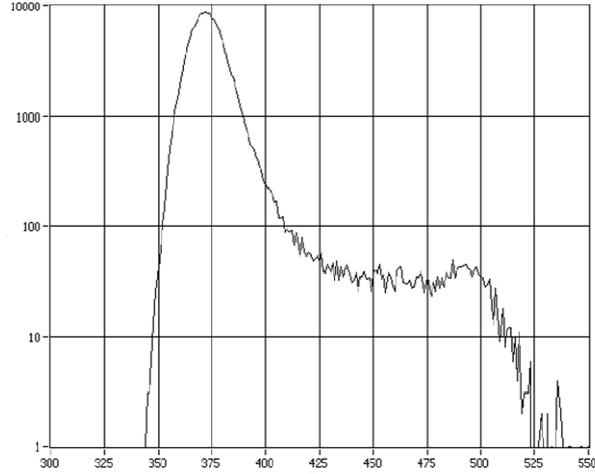


Figure 8 Histogram of x-ray on one storage cell

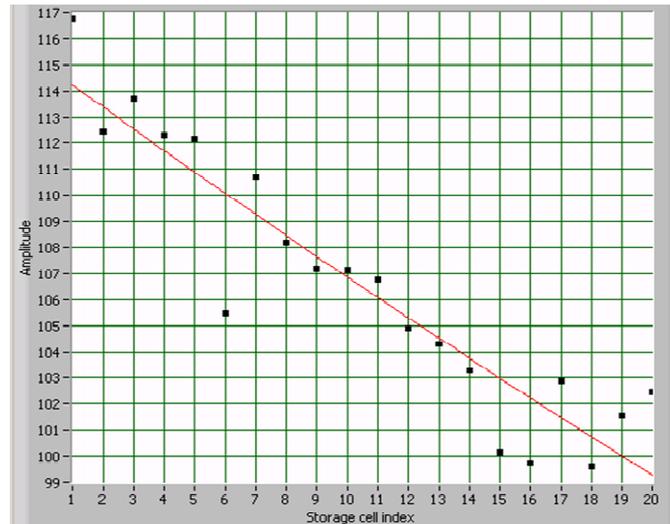


Figure 9 ^{55}Fe signal transferred from storage cells

cell, i is the cell index as mentioned above. The CTE can be calculated by fitting the curve. For these operation conditions, we measured a CTE of 0.9926.

4.3. Further work

The test on the ISIS2 main array was focused on one row so far. The next step is testing all the rows in the main array. There are several challenges if we want to do so. First, as the polysilicon to deliver the clock is not properly doped, the resistance of the track is very high; as a result the sensor cannot be clocked very fast. This will introduce larger dark current during readout. Secondly, there is a bug on the layout of the logical control circuitry which prevents pixel level CDS. Finally, different design variants require different operational conditions, which limit the useful sensor area for beam tests. However it will still be possible to make measurements such as charge collection efficiency and radiation tolerance. The problems encountered with ISIS2 can all be corrected in the next ISIS design.

5. Conclusion

The development of the In-situ Storage Image Sensor in the Linear Collider Flavour Identification collaboration for a vertex detector at the ILC has already established proof-of-principle. The latest version ISIS2 has demonstrated integration of buried channel, low voltage CCD with a 0.18 μm CMOS process, a major step towards satisfying the requirement of the vertex detector. Further study will be needed such as fine tuning of the operation settings, charge collection efficiency and radiation tolerance. A next-generation ISIS3 design will be needed to demonstrate the target granularity of the pixel array.

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