PROCEEDINGS OF SCIENCE

The Silicon Vertex Detector of the Belle II Experiment

Thomas Bergauer[*†]
HEPHY Vienna
E-mail: thomas.bergauer@oeaw.ac.at

The Belle experiment in Tsukuba (Japan) has been designed to measure rare decays in the B system with high statistics. Currently, both the KEKB e+/e- collider and the Belle experiment are being upgraded to provide and cope with an ultimate luminosity of $8 \times 10^{35} cm^{-2} s^{-1}$.
Since the previous Silicon Vertex Detector (SVD) cannot be operated with the 40-fold increased luminosity after the upgrade, it needs to be replaced. The future Belle II SVD will also consist of four layers of double-sided silicon strip sensors, but on larger radii and based on 6" silicon wafers, compared to its predecessor. Moreover, an inner double-layer with pixel detectors based on DEPFET technology will complement the SVD as innermost detector and the SVD itself will now contain a slanted forward part. Since the KEKB b-factory operates at relatively low energy, material inside the active volume has to be minimized in order to reduce multiple scattering. This can be achieved by thin, double sided silicon sensors, which are arranged to ladders in the so-called "Origami" chip-on-sensor concept, and a very light-weight mechanical support structure made from carbon fiber reinforced Airex foam. Moreover, CO_2 cooling of the front-end chips will ensure high efficiency at minimum material budget. Fast-shaping readout amplifiers will be used in conjunction with an online hit time reconstruction algorithm in order to reduce the occupancy to the level of a few percent at most.

The European Physical Society Conference on High Energy Physics
18-24 July, 2013
Stockholm, Sweden

*Speaker.
†For the Belle II SVD collaboration.

PoS(EPS-HEP 2013)487

1. From Belle to Belle II

The asymmetric e^-/e^+ collider KEKB at the Japanese High Energy Accelerator Research Organization KEK was successfully operated from 1999 to 2010 serving as a b-factory with high intensity beams of 1.6 A and 1.3 A current of the low energy and the high energy ring, respectively. After more than 10 years of operation, KEKB provided more than 1 ab^{-1} of integrated luminosity in total to the Belle experiment [1], whose measurements have offered important insights into the flavor structure of particles, especially in the violation of the CP symmetry among quarks [2]. The innermost detector used for tracking and vertexing was the Silicon Vertex Detector (SVD) comprising of four layers of double sided strip detectors (DSSDs). Before the shutdown of Belle, the occupancy of its innermost layer exceeded its design value significantly (see fig. 1) and introduced ambiguities for track reconstruction.

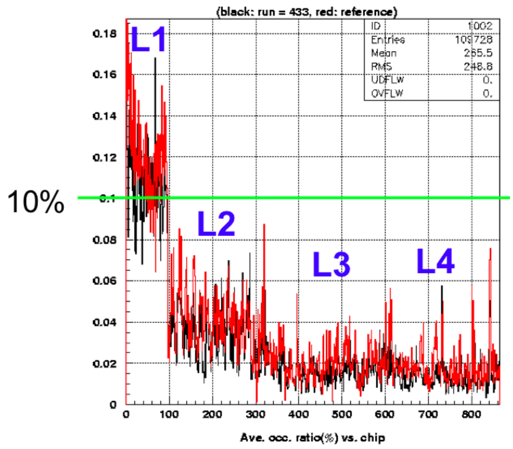

Figure 1: Occupancy during a typical run of Belle at maximum luminosity. The innermost layer L1 observed occupancies of up to 18%, which is above the limit of 10%.

1.1 Belle II

An elaborate upgrade program is currently ongoing to upgrade the KEKB collider to SuperKEKB, which will eventually provide a super-high luminosity of $8 \times 10^{35}\,\text{cm}^{-2}\,\text{s}^{-1}$ and will start in 2016. Many components, and especially the SVD, of the previous Belle experiment cannot handle this 40-fold increase in luminosity and thus needs to be upgraded as well. The upgraded Belle detector is subsequently called the Belle II experiment, which is described in detail in its Technical Design Report (TDR) [3].

1.2 SVD Layout

The Silicon Vertex Detector (SVD) of the previous Belle experiment was equipped with four layers of DSSD covering a radius up to 8.8 cm away from the beam pipe (fig. 2). The strips of sensors of each ladder were daisy-chained and read out by front-end hybrids located outside of the acceptance region by relatively slow VA1TA readout chips. This allowed a very low material budget inside the active volume.

The new Belle II SVD will also contain ladders comprising DSSDs which are arranged in four layers, but the layers extend up to 134 mm away from the beam (see table 1). Moreover, the sensors will be made of larger 6" silicon wafers compared to the old 4 inch sensors. Compared to the previous SVD, the Belle II SVD will have a slanted forward region using trapezoidal sensors in the forward direction caused by the energy asymmetry of the beams. The SVD will be complemented by two inner layers equipped with DEPFET-based pixel detectors called PXD [4].

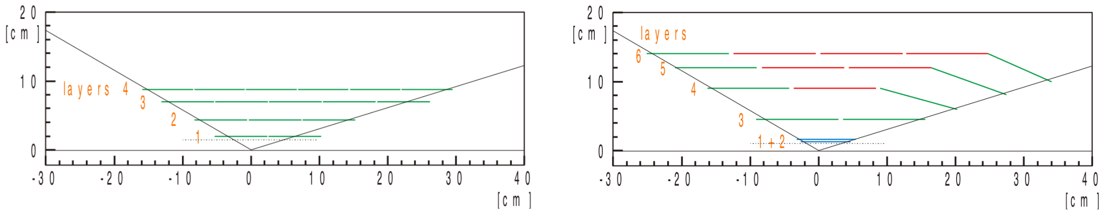

Figure 2: Layout of the layers of the Belle (left) and Belle II SVD (right). In the latter case, layers 1 and 2 (shown in blue) are an additional sub-detector of Belle II called PXD which is made of DEPFET pixels detectors. Layers 4-6 comprise double sided silicon strip detectors (DSSDs). Each red line corresponds to a so-called Origami module with readout electronics inside the active volume, while the green lines show modules read out by hybrids outside the acceptance region.

Layer #	**Radius [mm]**	**No. of Ladders**	**Rectangular sensors per ladder**	**Trapezoidal sensors per ladder**
6	134	16	5 (large)	1
5	105	12	4 (large)	1
4	80	10	3 (large)	1
3	38	7	2 (small)	-

Table 1: Table summarizing the key parameters of the four SVD layers of Belle II.

2. Double-Sided Silicon Strip Sensor R&D

The sensors for the Belle II SVD are double-sided silicon strip detectors made on 6" wafers with AC coupled readout and perpendicular strips on both sides. The silicon substrate is of n-type and has a active thickness of 300 μm. Only three different layouts are necessary for the whole SVD, which are summarized in table 2. The sensors are being fabricated by Hamamatsu (rectangular) and Micron Semiconductor (trapezoidal shape). The small rectangular sensor is only used in the innermost layer (L3) and therefore has a smaller pitch to increase the hit resolution toward the PXD. All other layers (L4–L6) use ladders composed of a variable number of large rectangular sensors in the barrel region and one trapezoidal sensor in the slanted forward part. Ladders are tilted with respect to the tangential plane by 5–7 degree (depending on the layer) and overlap their neighbors in a windmill-like structure in order to improve the alignment and compensate for Lorentz shifts in the magnetic field of 1.5 T.

	Readout strips #	Readout strips #	Readout pitch [μm]	Readout pitch [μm]	# of Sensors (+ spares)	Active area (length × width) [mm^2]
Sensor Side[1]	p	n	p	n		
Coordinate[2]	$r\phi$	z	$r\phi$	z		
Large rectangular	768	512	75 μm	240 μm	120+18	$122.90 \times 57.72 = 7029.88\,mm^2$
Small rectangular	768	768	50 μm	160 μm	14+4	$122.90 \times 38.55 = 4737.8\,mm^2$
Trapezoidal	768	512	50-75 μm	240 μm	38+6	$122.76\times (57.59+38.42)/2 = 5893.09\,mm^2$

Table 2: Table summarizing the three different sensor layouts.

2.1 Optimization of p-stop layout

On the wafers hosting the trapezoidal sensors additional baby sensors featuring different p-stop patterns on the n-side (ohmic side) of the sensors have been placed. Figure 3 shows sketches of these patterns, where p-type implantation is shown in red, n-type implantation in green.

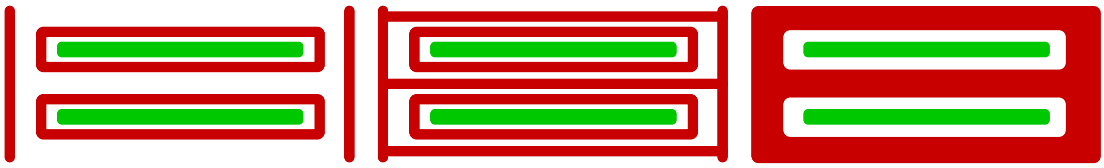

Figure 3: Schematic layout of atoll (left), combined (center) and common (right) p-stop layout. P-type implantation is shown in red, n-type implantation in green.

For the common p-stop layout, the n-type doped strips are surrounded by a p-type doped area covering the whole sensor. Only small regions around the strips are left unimplanted. This interrupts the accumulation layer which hence cannot short the n-type strips. In the atoll p-stop scheme, the n-type doped strips are embedded in isolated ringlike p-type implants. The combined scheme is a combination of the previous schemes where the n-type doped strips are surrounded by atoll p-stop implants. In addition to that, both strip and atoll implants are embedded in a p-type doped area covering the whole sensor, like in case of the common pattern.

On each sensor there are four zones, each with a different variant of its p-stop pattern. So in total, we compare twelve different p-stop geometries. The geometry variant is defined by the distance between the n-type strip implant and the p-stop implant. Hence the geometries are called "wide", "half-wide", "half-narrow" and "narrow", where for the "wide" geometry the p-stop implant

[1]Sensor side denotes to the physical side of the DSSD. **p** means the p-strips or junction side, while **n** denotes the n-strip or ohmic side of the detector.

[2]Coordinate inside the SVD and Belle coordinate system. **r**ϕ means transverse to the beam axis while **z** means along the beam axis.

is far away from the strip, and for the "narrow" geometry it is close. Reference [6] shows details of these designs.

The baby sensors hosting the structures described above have been tested in a beam test at CERN, and have been irradiated with gammas from a Co-60 source to 70Mrad. The beam test has been performed at CERNs SPS north area hall (zone H6) using 120GeV/c hadrons (mostly pions) to determine the signal-to-noise-ratios (SNR) of the different structures and geometric variants. Figure 4 shows the obtained SNR values. The atoll half-wide geometry performed best in both, the unirradiated and the irradiated case.

Figure 4: Signal to noise ratios of the three different p-stop layouts. The left bars (dark colors) show the unirradiated case while the right bars (bright colors) show the irradiated figures. The geometry which performed best is marked with a red box.

3. Readout and DAQ Chain

3.1 Front-End Chip

The front-end electronics of the SVD for Belle II utilizes the APV25 readout chip [7], initially developed for the CMS experiment at CERN, where 70.000 of those chips have been deployed and are being successfully operated. These chips have a fast shaping time of 50 ns which reduces the off-trigger background in Belle II by one order of magnitude compared to the previous readout chip and therefore reduces the occupancy problem described in section 1 [9]. A concept called *hit-time finding* has been developed to reduce the occupancy even further, which takes advantage of a special readout-mode of the APV chip called "multi-peak". This allows to read out multiple of three consecutive pipeline cells and therefore allows to sample the signal along the shaping curve. Using offline fits (during beam tests) and lookup-tables in FPGA (for Belle II), the maximum of the shaping curve can be determined with a precision of 2-3 ns RMS, which again reduces the occupancy by one order of magnitude [10].

3.2 Readout and DAQ chain

All other components of the front-end and back-end electronics for Belle II have been developed independently and are different from CMS. Figure 5 sketches the full DAQ chain. The analog signals from the APV front-end chips are time-multiplexed and transmitted via electrical cables to junction boxes (called DOCK) which sit inside the Belle II experiment, but outside the SVD (approx. 2 m away). There, level translation takes place and DC-DC converters [8] are located, which provides the correct voltages for the readout chips. The analog signals are relayed further out of the experiment to VME crates housing FADC boards, where the analog-to-digital-conversion, pedestal subtraction, data sparsification and hit-time finding takes place.

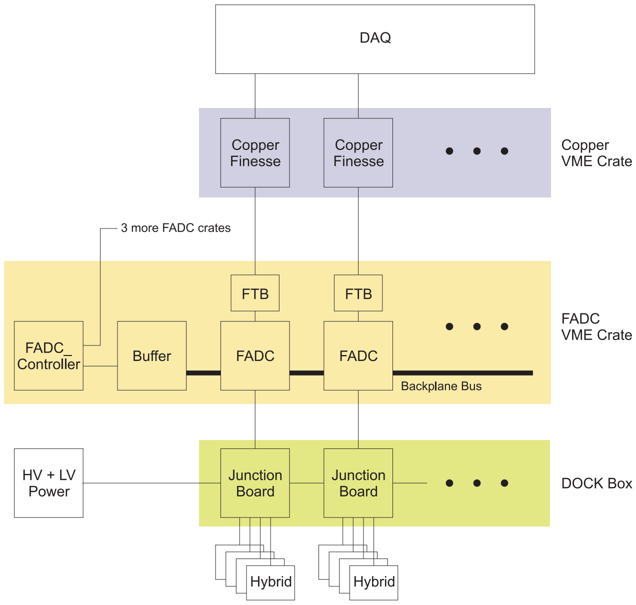

Figure 5: DAQ chain. The DOCK boxes are located inside the Belle II experiment (but outside of the SVD), the FADC VME crates are located on top of the experiment in dedicated racks, while the interface to the central DAQ of Belle II (called COPPER) is housed in the electronics hut next to the experiment.

4. Mechanics and Ladder Assembly

One drawback of the fast shaping time of the APV readout chips is a increased noise compared to the old readout chip. Therefore, daisy-chaining of more than one DSSD to shift the readout electronics outside the acceptance region is not possible anymore. Because of the hard requirements on material budget, a very light-weight, but active detector module and ladder concept has been developed. This concept utilizes one single CO_2 cooling pipe along a ladder. All readout chips are being placed underneath this pipe. This implies that the strips of the downward-facing side of the sensors have to be connected to the chips using fan-outs which are wrapped around the sensor edge. This concept is shown in figure 6 has therefore been named "Origami" [11].

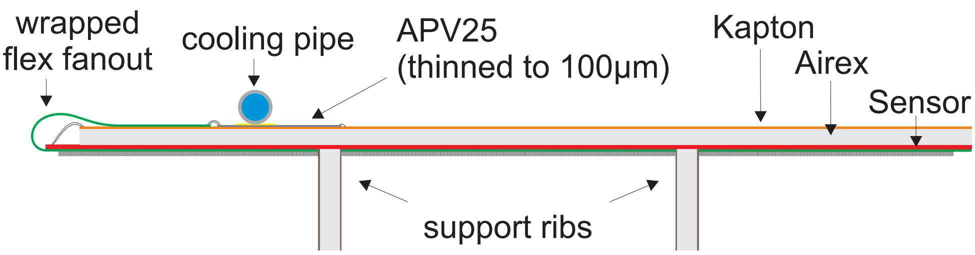

Figure 6: Chip-on-Sensor concept with wrapped flex fanout around the sensor edge.

The design of the ladders utilizes this concept for every sensor not directly being accessible from the outside of the acceptance region (modules shown in red on the right-hand side of figure 2).

Because of the this, and to keep the material budget low, the modules cannot be placed individually onto a support structure, but are interweaved by each other, forming a whole ladder as "elementary unit" of the SVD design. An exploded view of a longest ladder of the outermost layer 6 is shown in figure 7.

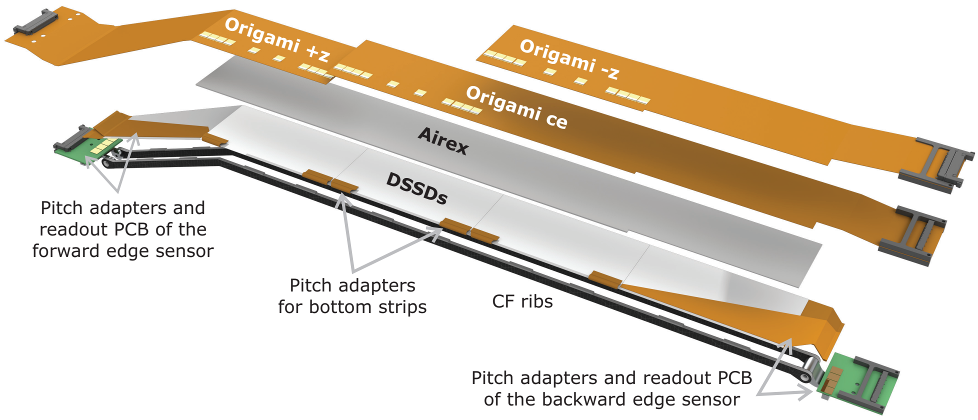

Figure 7: Exploded view of one ladder of outermost layer 6.

It shows the Kapton flex PCBs for three origami sensors, one trapezoidal sensor for the forward region and one conventionally read out sensor for the backward side. The Kapton is separated from the sensors by a thin layer of Airex foam. The mechanical structure is maintained by two ribs, made of a sandwich of thin carbon fiber layers with Airex foam in between. This results in an average material budget of 0.59% of X_0 per ladder [12].

5. Summary and Outlook

The SVD for the Belle II experiment is a completely new device utilizing a very light-weight ladder concept called "Origami", necessary to maintain a low material budget. The operational limits in terms of occupancy of the previous detector is circumvent by using readout chips with faster shaping times and hit-time finding to reduce the off-trigger background by a factor of 100 in total. The R&D for the silicon sensors has been performed to determine the best p-stop geometry for the double sided silicon strip sensors. The project is currently during a transition from the design to the production phase with the mass production of around 50 ladders starting soon.

References

[1] A. Abashian et al., *The Belle Detector* Nucl. Instrum. Meth. A479, 117 (2002), 10.1016/S0168-9002(01)02013-7.

[2] M. Kobayashi, T. Maskawa, *CP-Violation in the Renormalizable Theory of Weak Interaction*, Prog. Theor. Phys. (1973) 49 (2): 652-657. doi: 10.1143/PTP.49.652

[3] Z. Dolezal, S. Uno (ed.), *Belle II Technical Design Report*, KEK Report 2010-1 (July 2010)

[4] C. Marinas (for the DEPFET collaboration), *The Belle-II Pixel Vertex Tracker at the SuperKEKB Flavour Factory*, Nucl. Instr. and Meth. 628 (1), p. 95-98, 2011, doi:10.1016/j.nima.2010.06.292

[5] T. Bergauer, *Recent Progress in Sensor- and Mechanics-R&D for the Belle II Silicon Vertex Detector*, Nucl. Instr. and Meth. A 54867 (2013), pp. 279-282

[6] M. Valentan et al., *Optimization of Strip Isolation for Silicon Sensors*, Proceedings of the TIPP 2011 conference in *Physics Procedia Volume 37, 2012, Pages 891Ð898*

[7] M. French et al., *Design and results from the APV25, a deep sub-micron CMOS front-end chip for the CMS tracker*, Nucl. Instr. and Meth. A 466 (2001), 359–365

[8] S. Michelis et al., *A complete DCDC converter ASIC for LHC upgrades*, in Topical Workshop on Electronics for Particle Physics 2012, 17Ð21 September 2012, Oxford, U.K.

[9] M. Friedl, C. Irmler, M. Pernicka, *Occupancy reduction in silicon strip detectors with the APV25 chip*, Nucl. Instr. and Meth. A 569, Issue 1 (2005), 92-97

[10] C. Irmler et al., *Online data processing and hit time reconstruction for silicon detector readout*, Nucl. Instr. and Meth. A 617 (2010) 280-282

[11] C. Irmler, M. Friedl, M. Pernicka, *Construction and Performance of a Double-Sided Silicon Detector Module Using the Origami Concept*, TWEPP-09, CERN-2009-006, 211–215, `http://cdsweb.cern.ch/record/1234895/files/p211.pdf`

[12] C. Irmler et al., *A Low Mass On-Chip Readout Scheme for Double-Sided Silicon Strip Detectors*, Proceedings of VCI2013 conference (in press), `http://dx.doi.org/10.1016/j.nima.2013.05.169`

PoS(EPS-HEP 2013)487