

## First Results from Cherwell, a Monolithic Active Pixel Sensor for Particle Physics.

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Cherwell is a CMOS Monolithic Active Pixel Sensor (MAPS) developed for digital calorimetry and charged particle tracking applications. Here, we outline the initial tests carried out to characterise the performance of Cherwell, give details of the test beam carried out at CERN and include the first results from this analysis. Three variations of the chip were tested; Type A, a high resistivity, low noise sensor, Type B, a standard resistivity, low noise sensor and Type C, a standard resistivity, standard noise sensor. The sensors yield an average RMS noise value per pixel of  $9.6 e^-$  and a gain of  $0.17 \text{ ADCs}/e^-$ . The sensor efficiencies are 99.89% for Type A, 99.77% for Type B and 99.73% for Type C, with an average efficiency of 99.80%.

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## 1. Introduction

Cherwell was designed by the Rutherford Appleton Laboratory (RAL) CMOS Sensor Design group and manufactured by TowerJazz Semiconductor Ltd [1] with  $0.18\mu\text{m}$  technology, using a four-transistor (4T) pixel architecture for charged particle detection. The Arachnid collaboration [2] are currently analysing the performance of the Cherwell sensor for potential applications in particle physics. As particle accelerators progress to higher luminosities, the requirements put upon detector hardware are becoming more severe. Cherwell aims to demonstrate crucial properties, such as high granularity, fast data processing and radiation hardness, as needed for vertexing and tracking in high particle density environments. Additionally, the current devices have the potential to be back thinned to produce reduced mass devices, whilst leaving the electronic design unchanged. Thicknesses of  $50\mu\text{m}$  are already achievable with high yield and could be back thinned to a theoretical minimum of  $\approx 12\mu\text{m}$ , which would significantly reduce the level of multiple Coulomb scattering experienced by charged particles traversing a sensor.

In order to achieve fast data processing, in-pixel intelligence is required, which demands the use of PMOS transistors. The associated PMOS n-well competes with the charge collecting n-well diode, parasitically collecting some of the charge deposited by the incoming particle, leading to inefficient regions within a pixel. Cherwell is a variant of CMOS MAPS called INMAPS, which incorporates both NMOS and PMOS transistors, maximising charge collection in n-well diodes whilst minimising signal loss. This is achieved by introducing a deep p-implant to shield the PMOS n-well, thereby increasing the charge collection below that region and increasing the sensitive area within the pixel to approximately 100%. This deep p-well also provides a potential volume for circuitry to be embedded within, as an alternative to the pixel edges, resulting in an increased fill factor.

The design for the Cherwell sensor is an amalgamation of two previous sensor designs; **Tera-Pixel Active Pixel Sensor for CALICE (TPAC)** [3], originally developed by CALICE-UK [4] as the first MAPS device to employ the  $0.18\mu\text{m}$  process and **Fortis** [5], a prototype  $0.18\mu\text{m}$  CMOS Image Sensor with a 4T pixel architecture, developed by the SPiDeR collaboration [6], a **Silicon Pixel Detector R&D** programme which precedes Arachnid. TPAC was developed for digital electromagnetic calorimetry, underpinning the design of half the active area of Cherwell. Fortis was designed primarily for tracking and vertexing and was optimised for minimal noise and high conversion gain, as adopted by the two designs in the second half of Cherwell. Both TPAC and Fortis tested the effects of including a deep p-well to the pixel structure.

## 2. Cherwell

Cherwell has been developed to include both digital calorimetry and tracking capabilities in a low power, low noise pixel detector. Cherwell directly draws on the experience and knowledge obtained through Fortis and TPAC in a combination to increase the active area of the chip, reduce the noise and increase the readout speed. Being an INMAPS device, all the Cherwell wafers have been fabricated including a deep p-implant. We have tested four wafers with an epitaxial layer resistivity of  $10\text{-}100\Omega\text{cm}$  [5], which is typical of CMOS MAPS devices. Also tested were two wafers with

a higher epitaxial layer resistivity of 1-10 k $\Omega$ cm [5], in order to investigate the effects on charge collection. An increase in resistivity leads to an increase in the depletion depth which will extend the depletion region from the PN junction further into the epitaxial layer. For high resistivities, the majority of the charge deposited should be within this depletion volume and therefore collected via drift rather than diffusion, decreasing both the charge collection time and charge spread. Two of the six wafers also include a low noise Vt implant for the source follower.

The 4T architecture in Cherwell allows for high conversion gain and Correlated Double Sampling (CDS) to remove the reset noise. The chip itself is divided into four separate pixel designs which all share a common back-end. Half of the chip is dedicated to digital electromagnetic calorimetry, represented by the 'DECAL-25' and 'DECAL-50' segments whilst the other half of the chip is devoted to vertexing and tracking using the 'strixel' and 'reference pixel' segments.

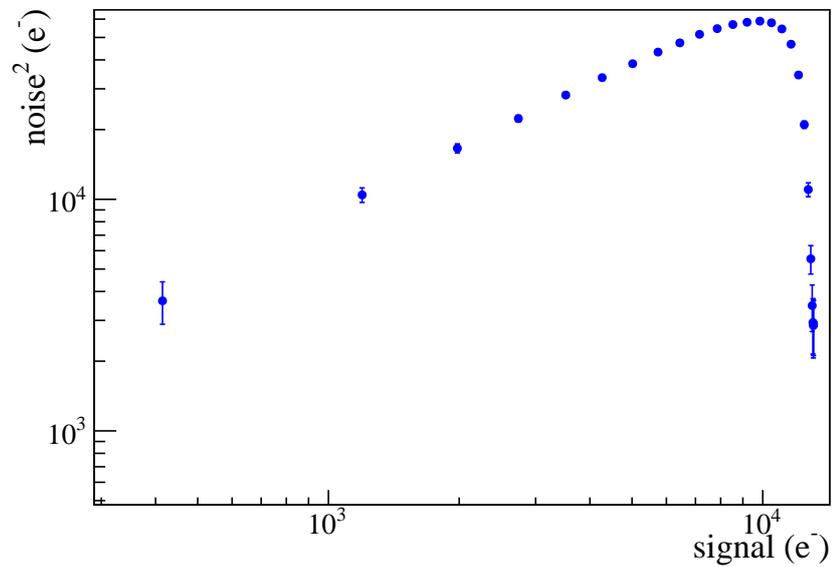
The DECAL-50 and DECAL-25 pixels have dimensions 50x50  $\mu\text{m}^2$  and 25x25  $\mu\text{m}^2$  respectively. The DECAL-50 is made up of 1152 pixels in a 48x24 pixel array and the DECAL-25 has the same size with 4608 pixels in a 96x48 pixel array. The DECAL-25 pixels have been fabricated with circuitry to allow the pixels to be grouped together to create virtual 50x50  $\mu\text{m}^2$  pixels by summing 2x2 pixels on readout. This facilitates the study of charge sharing between pixels. One can compare the individual DECAL-25 pixels that are summed with the larger DECAL-50 pixels. Both DECAL segments of the chip feature an analogue-to-digital converter (ADC) at the base of the columns for rolling shutter readout, in which the different columns within the array are exposed at different times and readout in a wave-like fashion. The DECAL sections also have the faculty for a global shutter mode or 'snapshot readout' in which all pixels within the sensor begin and end the exposure simultaneously.

Both the reference pixel and strixel architectures consist of 4608 pixels arranged in a 96x48 pixel array with pixel sizes of 25x25  $\mu\text{m}^2$ . The reference pixels are the baseline design which resemble the previous Fortis design. This design is included to test the integrity of the chip and interpret the consequences of the new technology implemented in the other three designs. Like the DECAL sections, the reference pixels have an ADC at the base of each column for rolling shutter readout. The strixel is electrically identical to the reference pixel but has islands of electronics within the deep p-well of each pixel into which the entire ADC is folded, eliminating dead regions at the end of column where the readout electronics are usually placed and so increasing the active area of the chip.

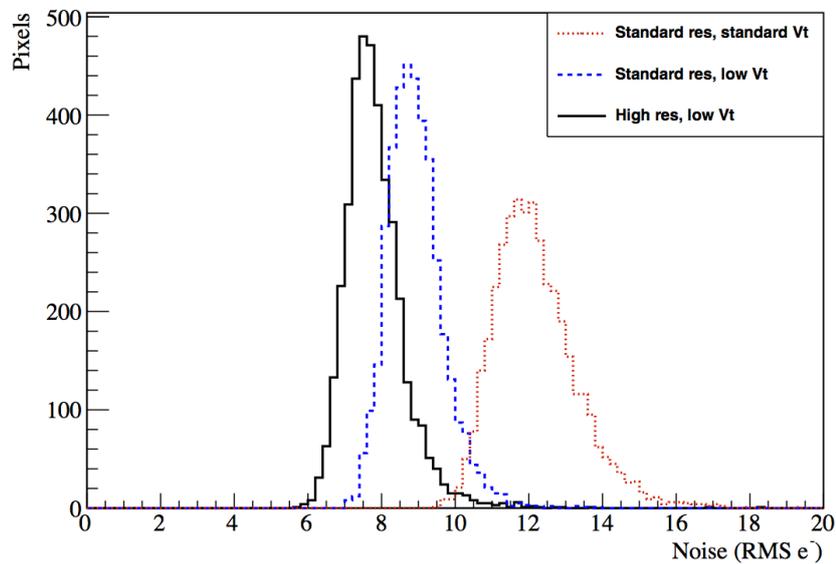
For the results shown in this paper, only the reference pixels have been used.

### 3. Initial Tests

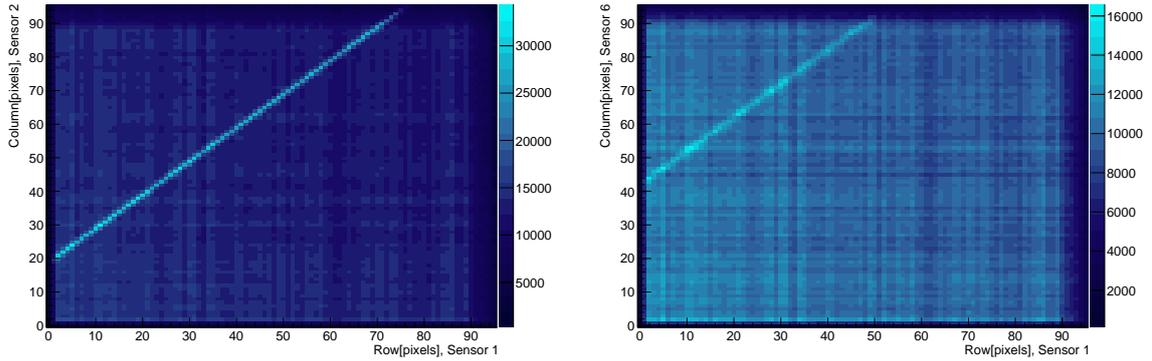
Photon Transfer Curves (PTCs) were used to characterise the Cherwell chip by illuminating the sensor with a uniform distribution of UV light from LEDs in varying intensities. Figure 1 shows the PTC for a Type A Cherwell sensor. The PTC yields a linear full well of 11500 $e^-$  and a maximum full well of 14700 $e^-$ , values in agreement with previous measurements made using an  $^{55}\text{Fe}$



**Figure 1:** Photon transfer curve for a Type A Cherwell sensor, demonstrating a maximum full well capacity of  $14700e^-$ .



**Figure 2:** The average RMS noise values for the three variations of Cherwell sensor are  $7.8e^-$ ,  $8.9e^-$  and  $12.2e^-$  per pixel, for the sensors of Type A, B and C respectively.



**Figure 3:** Correlation of particle hits between the first and second sensor (left) and between the first and sixth sensor (right). The y-intercept represents the physical offset between the sensors in pixels and was subsequently used to correct the alignment for tracking.

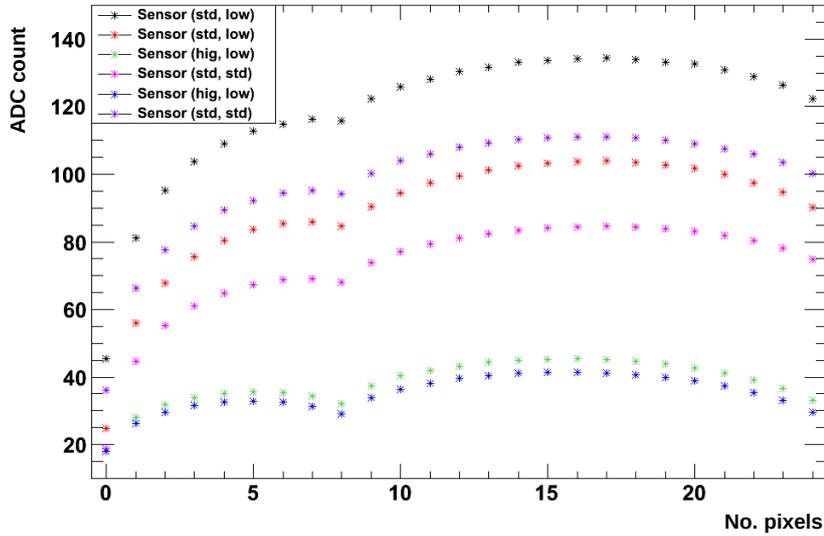
source [7]. The RMS noise distributions per pixel sensor types A, B and C are  $7.8e^-$ ,  $8.9e^-$  and  $12.2e^-$  respectively, as shown in Figure 2. The noise is uniform across each sensor, with the width and mean values decreasing for high resistivity epitaxial layers and low Vt implant, as expected. Additionally, the average gain was found to be  $0.17 \text{ ADCs}/e^-$ .

## 4. Test Beam

The Arachnid collaboration took six Cherwell sensors to a test beam in November 2012 at the North Hall on the Preveessin site at CERN with aims to understand the charge sharing, efficiency and resolution of the chip. The six sensors consisted of two Type A, two Type B and two Type C Cherwell sensors, positioned in a stack along the direction of the T4 beamline of 120 GeV pions. The sensor stack was placed on an x-y stage, which was controlled remotely for alignment, with two scintillators placed downstream of the sensor stack and an additional scintillator immediately upstream of the stack to act a triple coincidence trigger. The total data collection time spanned 2.5 days with a trigger rate of  $\approx 3\text{Hz}$ . The data was readout using a USB interface.

### 4.1 Correlation Plots

The amount of charge deposited in each of the six sensors was readout and processed, subtracting the pedestals and correcting the data for common-mode noise. Particle ‘hits’ were defined as pixels with an ADC count  $5\sigma$  above the remaining background noise. Correlation plots were made to compare the hits in the reference sensor, chosen to be the sensor furthest downstream of the beam, to the ADC counts in each other sensor in turn, pixel by pixel, for the rows and columns. The results shown in Figure 3 demonstrate that particles were detected passing through all six sensors.



**Figure 4:** A ‘seagull plot’ demonstrating an increase in ADC count as the first 9 pixels are summed on the left ‘wing’. The ADC count then stabilises, with no increase to the total ADC count after 25 pixels are summed. This implies no useful information is gained from including the second ring of pixels surrounding the seed, placing an upper limit on the cluster size.

## 4.2 Sensor Efficiency

The pixels were grouped together into ‘clusters’ corresponding to the same particle hit. An upper limit on the cluster size was chosen from the results shown in Figure 4. Here, the seed was identified as any pixel with an ADC count  $5\sigma$  above the background noise. The 8 pixels surrounding the seed were added, successively in descending order of their ADC counts to the seed pixel, as shown on the left hand side, or left ‘wing’, of the figure. The entire  $3 \times 3$  pixel matrix was then taken to be the seed and the surrounding 16 pixels were added in the same fashion, represented by the right wing. Figure 4 demonstrates that only noise, not useful information is obtained through the inclusion of the second set of surrounding pixels, so an upper limit on the cluster size was taken to be 9 pixels within a  $3 \times 3$  matrix, where, excluding the seed, only pixels exceeding an ADC count  $3\sigma$  above the noise value were added to the cluster.

The efficiency of each sensor was calculated using two other sensors as a double coincidence trigger, comparing the number of clusters seen in the trigger system,  $N_{tot}$ , with the detection of clusters in the sensor under study,  $N_{succ}$ . Hence, the detection efficiency,  $\epsilon$ , given by  $\frac{N_{succ}}{N_{tot}}$  acquires a value between 0 and 1. The average efficiency for each sensor type was calculated and results are shown in Table 1.

Sensor Type	Resistivity	Vt	Efficiency
A	High	Low	99.89%
B	Standard	Low	99.77%
C	Standard	Standard	99.73%

**Table 1:** The average detection efficiencies for three types of Cherwell sensor. The efficiencies are based on test beam data using 50,000 triggers.

## 5. Conclusions and Future Work

Laboratory tests and the initial results from the CERN test beam demonstrate the Cherwell reference pixels are working well. Three variations of Cherwell sensor were tested; Type A, a high resistivity, low noise sensor, Type B, a standard resistivity, low noise sensor and Type C, a standard resistivity, standard noise sensor. PTC scans found a maximum full well capacity of  $14700 e^-$ , an average gain of  $0.17 \text{ RMS}/e^-$  and average RMS noise values of  $7.8e^-$ ,  $8.9e^-$  and  $12.2e^-$  per pixel for sensor types A, B and C respectively. The detection efficiencies were measured to be 99.89% for Type A, 99.77% for Type B and 99.73% for Type C, with an average overall efficiency of 99.80%.

Presently the resolutions of the reference pixels are being calculated for each sensor type, after which particle tracking will be implemented. Tests on the strixel part of the chip are underway and these shall be extended to the DECAL half of the chip in the near future. Cherwell is the first iteration of a design being used for a prototype chip for the phase 1 Alice Inner Tracker System upgrade at CERN [8].

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