

## Development and Evaluation of an Event-Driven SOI Pixel Detector for X-Ray Astronomy

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We have been developing a monolithic active pixel sensor with silicon-on-insulator technology for use in X-ray astronomical satellite missions. Our aim is to replace the X-ray charge-coupled device—which is the standard detector in the field—with a device that exhibits a high-coincidence time resolution (i.e.,  $\sim 1 \mu\text{s}$ ), superior hit-position readout time (i.e.,  $\sim 10 \mu\text{s}$ ), and wider bandpass (i.e., 0.3–40 keV), in addition to having comparable performance in imaging spectroscopy. To realize this detector, we have developed prototype detectors called the “XRPIX” series. XRPIX contains a comparator circuit in each pixel to detect an X-ray photon, and it offers an intra-pixel hit trigger (timing) and two-dimensional hit-pattern (position) outputs. Therefore, XRPIX is capable of direct access to selected pixels to read out the signal amplitude. X-ray signal readout by this function is called an “event-driven readout.” In our previous study, we successfully demonstrated the X-ray spectra acquisition by the event-driven readout. However, there were some problems in the circuit operation. Recently, these investigations progressed because of many evaluation tests. In this paper, we describe the development and the evaluation of the event-driven readout by XRPIX.

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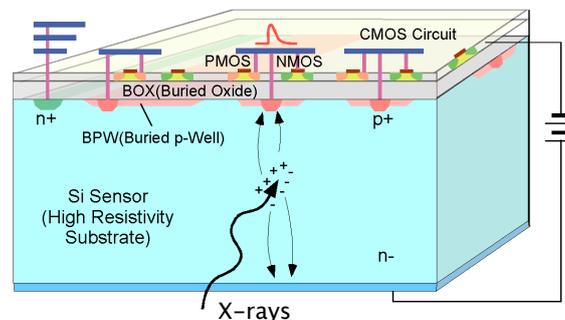
## 1. Introduction

The standard imaging spectrometers of modern X-ray astronomical satellites are X-ray charge-coupled devices (CCDs) [1]-[3]. The X-ray CCD offers Fano-limited X-ray spectroscopic performance with a readout noise of approximately three electrons. This enables us to obtain wide and fine imaging with a sensor size of 20–30 mm square and a pixel size of  $\sim 30 \mu\text{m}$  square. However, this X-ray CCD has some limitations. The most serious issue is the non-X-ray background (NXB) generated by cosmic rays in orbit, which has a serious influence on the energy spectrum above 10 keV. The NXB rate is extremely high to study faint sources. Therefore, a low-background detector is preferred in the next generation. Moreover, the time resolution is very poor to conduct a fast timing study of time-variable sources.

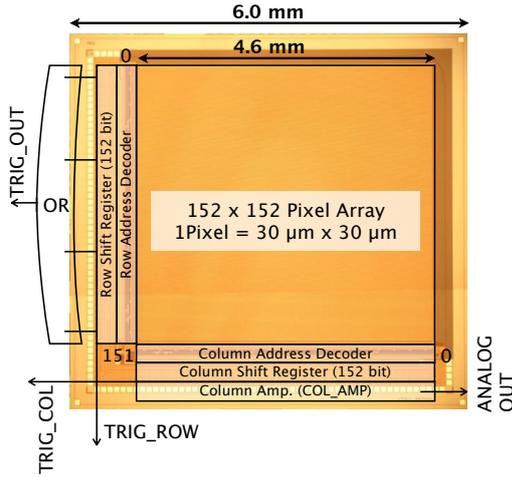
By introducing an anticoincidence method between the hit signal and the external active shield detector [4][5], the background produced by the cosmic-ray tracks [6] can be significantly reduced. The new detector must have good coincidence time resolution (i.e.,  $\sim 1 \mu\text{s}$ ) and a superior hit-position readout time (i.e.,  $\sim 10 \mu\text{s}$ ) to reduce the NXB by cosmic rays. This is important for hard X-ray observation with energies above 10 keV. In addition, the detector must have a wide bandpass (from soft to hard X-rays, 0.3–40 keV) and comparable performance in terms of imaging spectroscopy [7][8].

To realize the detector described above, we have been developing a new type of active pixel sensor based on a semiconductor pixel detector with silicon-on-insulator (SOI) complementary metal-oxide-semiconductor (CMOS) technology. This new SOI pixel detector (SOIPIX) has been recently developed by the High Energy Accelerator Research Organization (KEK) [9]. The SOI wafer consists of two bonded silicon wafers with a thin oxide film in between. The pixel detector consists of a circuit with low-resistivity silicon and a sensor with high-resistivity silicon. The SOIPIX utilizes a thick handle wafer for the SOI structure as a radiation sensor to detect charged particles and X-rays (Figure 1). Therefore, the SOIPIX is realized with ideal monolithic active pixel sensors. Thus, we designed an “event-driven SOIPIX” with a trigger information output function as the “XRPIX (X-Ray PIXel) series.” Furthermore, we realized a spectroscopy system in which the NXB background rate is reduced to 1% as compared with a CCD.

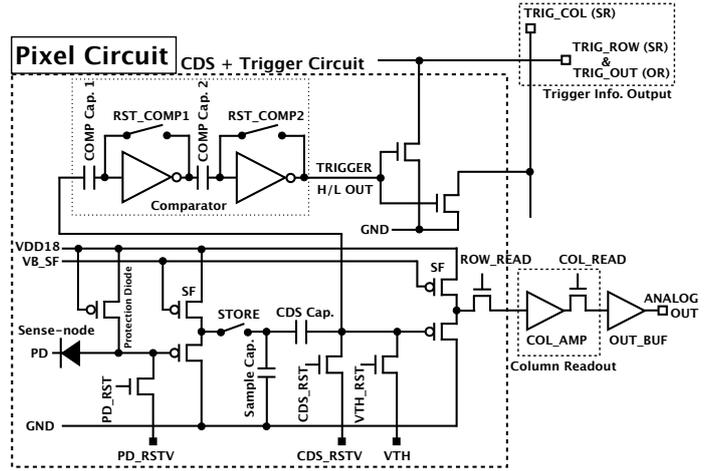
In our previous study, we successfully demonstrated the X-ray detection by the event-driven readout [10]. However, some unexpected behaviors were also observed. Recently, these behaviors were investigated with a detailed test of the pixel signal. In this paper, we describe the development and the evaluation of the event-driven SOIPIX.



**Figure 1:** Cross-sectional view of SOIPIX.



**Figure 2:** Chip photograph of XRPIX2b and its block diagram.



**Figure 3:** Pixel circuit of XRPIX2b. The comparator circuit for trigger detection is an inverter chopper-type.

## 2. Description of XRPIX2b

### 2.1 Specifications

By 2013, the XRPIX series included six devices: XRPIX1/1b/2/2b/3/3b. In each chip, the spectroscopic performance and event-driven readout are tested and improved. As described in Section 1, we have investigated the source of the problem in the event-driven readout. For this evaluation test, we used the XRPIX2b device, which has a medium-sized sensing area. The effective area is  $4.6 \text{ mm} \times 4.6 \text{ mm}$ , the pixel size is  $30 \mu\text{m} \times 30 \mu\text{m}$ , and the number of pixels is 20,000 (Figure 2).

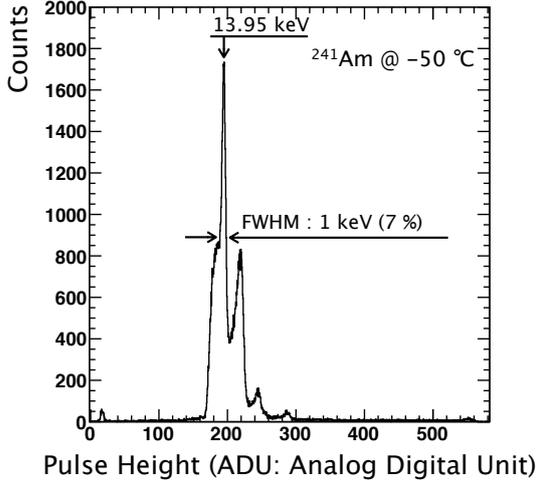
### 2.2 Pixel Circuit

The pixel circuitry of XRPIX2b is shown in Figure 3 and can be divided into two main parts, i.e., the signal processing part containing the correlated double sampling (CDS) circuit and the trigger part. The CDS circuit suppresses the  $kT/C$  reset noise in the sense node and subtracts the offset levels. The trigger circuit generates a trigger signal when an X-ray signal crosses the threshold voltage (VTH) of the pixel. This function is realized by two inverter chopper-type comparators. The reason for using two inverter stages is to increase the detection sensitivity. This comparator contains a cascade of inverter stages, which is basically a bistable multivibrator.

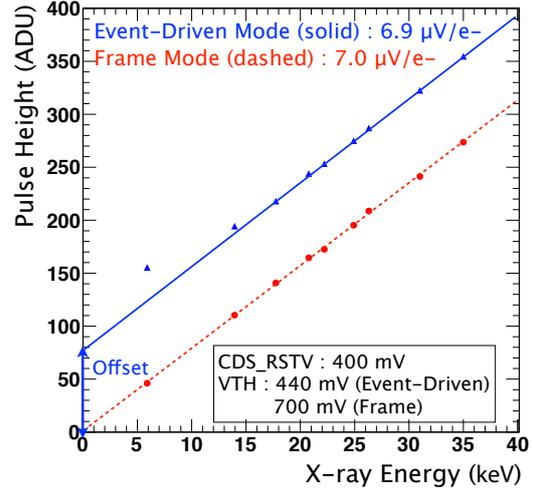
### 2.3 Readout Architecture of the Trigger Information

The readout operation method using intra-pixel trigger information that is event-driven is described below. XRPIX resets the pixel circuit periodically. A comparator circuit is reset first (VTH level), and an analog signal circuit (sense node) is then reset (PD\_RSTV and CDS\_RSTV level). Then, an exposure is started. The output of the comparator circuit is reversed when the voltage at the sense node exceeds the VTH by an X-ray or charged-particle signal (i.e., a trigger signal).

The trigger output signal from a pixel is wired-OR'ed in the row and column directions and stored in the shift registers at the edges of the sensor array. The 152 wired-OR'ed row signals are then OR'ed again. After receiving the trigger output signal with an external circuit, the X and Y addresses of the hit pixel are available from the row and column shift registers. Refer to [10] for more detail.



**Figure 4:** X-ray spectrum of the  $^{241}\text{Am}$  radioisotope in the event-driven readout mode. One ADU is  $\sim 244 \mu\text{V}$  ( $1 \text{ V}/12 \text{ bit}$ ). The CDS\_RSTV voltage is 400 mV, and the VTH is 440 mV.



**Figure 5:** Calibration between the X-ray energy and the signal pulse height (ADU). The solid/dashed lines represent a linear fit to the event-driven and the frame readout modes, respectively. The data at 5.9 keV ( $^{55}\text{Fe}$ ) were omitted from the fit.

### 3. Evaluation of the Event-Driven Readout

XRPIX can be also operated in the “frame readout mode,” which reads an analog signal from all pixels periodically. In this section, we evaluate the data obtained in the event-driven mode in comparison with those taken in the frame readout mode.

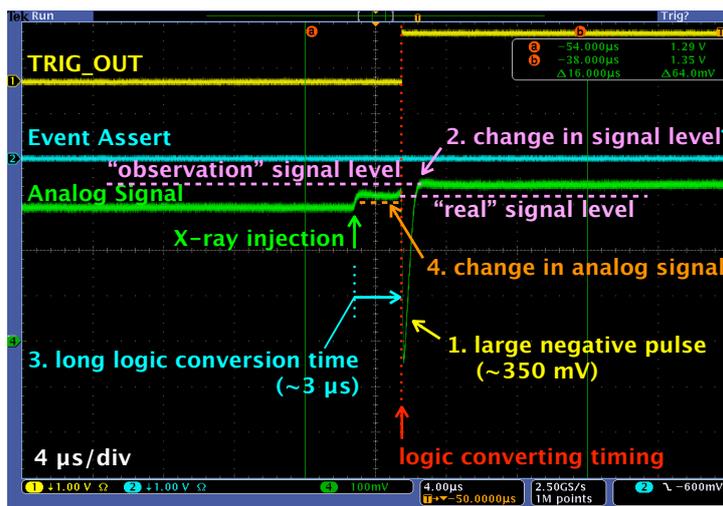
#### 3.1 X-Ray Spectrum

In the previous study, there was a problem in the response to X-rays. For discussing this test, the X-ray spectrum obtained by the event-driven readout of XRPIX2b is shown in Figure 4. To conduct this test, a voltage of 100 V is applied to the sensor, which is cooled to  $-50 \text{ }^\circ\text{C}$ . The CDS\_RSTV voltage is 400 mV, and the VTH is 440 mV. Figure 4 shows the X-ray emission spectrum (i.e.,  $\sim 100,000$  events) from a  $^{241}\text{Am}$  radioisotope sample. The energy resolution is  $\sim 1 \text{ keV}$  at full width at half maximum (FWHM) at 13.95 keV. This result is poor compared with the frame readout mode (650 eV at FWHM at the same line). It is shown that this difference has some problems.

#### 3.2 Energy Calibration

The difference between the event-driven and frame readout modes becomes evident in the X-ray energy calibration. Figure 5 shows the calibration plot using the  $^{55}\text{Fe}$ ,  $^{241}\text{Am}$ ,  $^{109}\text{Cd}$ , and  $^{133}\text{Ba}$  X-ray lines at 5.9, 13.95, 17.74, 20.77, 22.2, 24.9, 26.3, 31, and 35 keV. The analog-to-digital converter gain is 7.7 (ADU/keV) from the slope of the linear fitting. Thus, the gain of the X-ray response is  $6.9 (\mu\text{V}/e^-)$  in the event-driven readout mode. In this case,  $^{55}\text{Fe}$  is not used as data because the 5.9 keV line is shifted from the fitting line.

This calibration plot has two unexpected points. First, the plot has an offset of  $\sim 80 \text{ ADU}$  (i.e.,  $\sim 20 \text{ mV}$ ). Second, as described above, the pulse height of the output deviates from linearity at low energy (i.e., 5.9 keV). These differences are due to the comparator circuit operation. It is necessary to investigate these causes and to understand the phenomena.



**Figure 6:** Waveform expanded during X-ray injection. The time range is  $4 \mu\text{s}/\text{div}$ . There are four problems in this waveform.

## 4. Investigation of the Event-Driven Problem

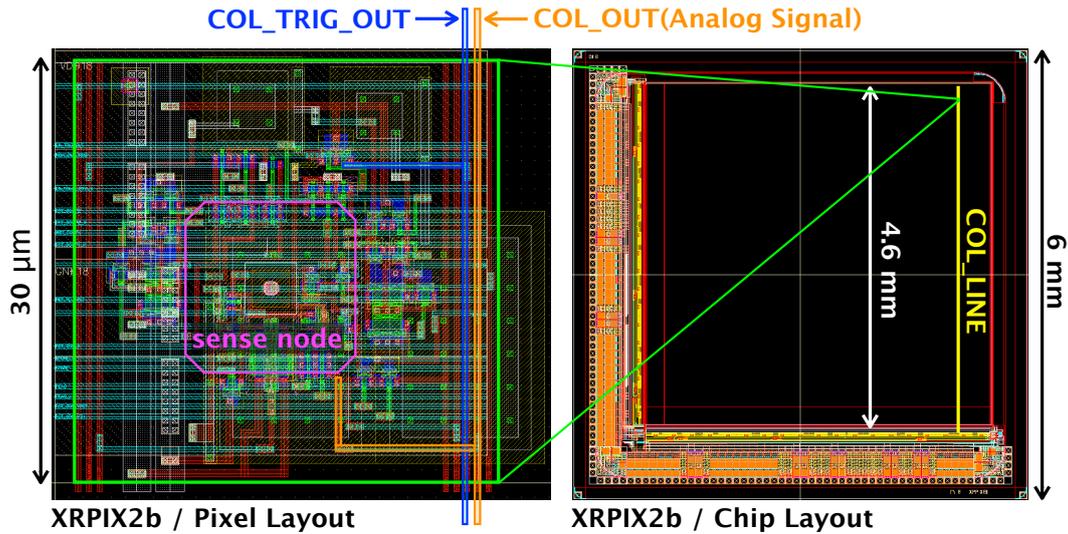
### 4.1 Analog Signal Waveform

To understand the results obtained in Section 3.2, the analog waveform of the pixel circuit was observed with an oscilloscope. Figure 6 shows the waveform in the event-driven readout mode when a 22.2 keV X-ray from the  $^{109}\text{Cd}$  radioisotope is detected. The control signal shows TRIG\_OUT—which is the logic output signal from the comparator circuit of XRPIX2b—and Event Assert—which is the fixed signal of the X-ray event by the field-programmable gate array.

In this waveform, we found four unexpected phenomena. First, there is a large negative pulse of  $\sim 350$  mV when TRIG\_OUT changes from a logical low to high. Second, there is a difference between the “real” signal level, which is the true detection signal from the X-ray, and the “observation” signal level, which is the recorded signal by the electronics. Third, the logic conversion time is longer than expected. In this case, this conversion time is  $\sim 3 \mu\text{s}$  (typically,  $\sim 100$  ns). Fourth, the analog signal changes after X-rays enter until the logic of TRIG\_OUT is converted. It is necessary to understand these phenomena to solve the event-drive readout mode problem. Although it was difficult, we were able to understand these phenomena.

### 4.2 Reason for the Large Negative Pulse

It was assumed that the large negative pulse in Figure 6 appears because of the cross-talk by capacitive coupling. In fact, the trigger and analog signal lines were found to be adjoined by the inspection of the layout design file and searching for the capacitive coupling point. Figure 7 shows the pixel and chip layouts of XRPIX2b. The trigger and analog signals in the direction of a column are parallel. This results in a capacitive coupling of  $\sim 250$  fF. The negative pulse is also confirmed by adding a parasitic capacitance to the HSPICE circuit simulation. Fortunately, this does not occur during typical data acquisition. This phenomenon appears only when a pixel is fixed, and it observes the analog signal. However, it is necessary to consider this phenomenon in future designs to reduce cross-talk.



**Figure 7:** Relationship between the COL\_TRIG\_OUT signal and the COL\_OUT signal in the pixel and chip layouts.

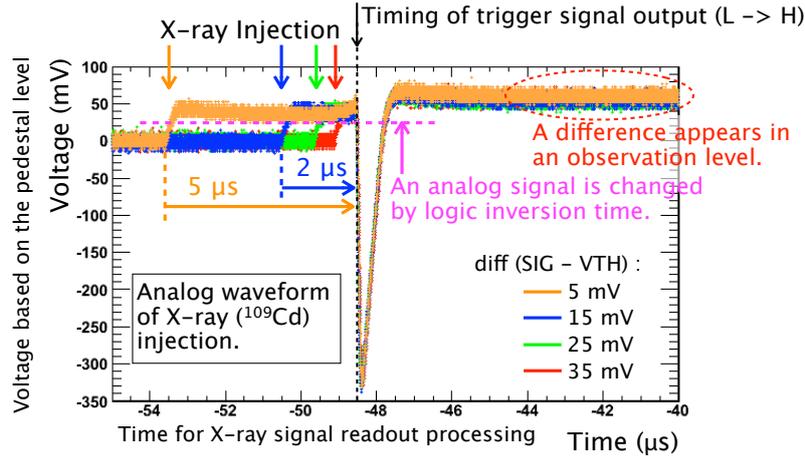
### 4.3 Reason for the Change in Signal Level

The difference between the “real” and “observation” signal levels in Figure 6 appears because of the capacitive coupling of the trigger signal line and the sense node (i.e., the floating line). This is visualized by an abrupt increase in the analog signal level that does not return to the original level that is unrelated to the large negative pulse. The difference in the observation signal level is equivalent to the offset in the calibration plot (Figure 5). This is an existing offset that cannot be prevented under the present circumstances.

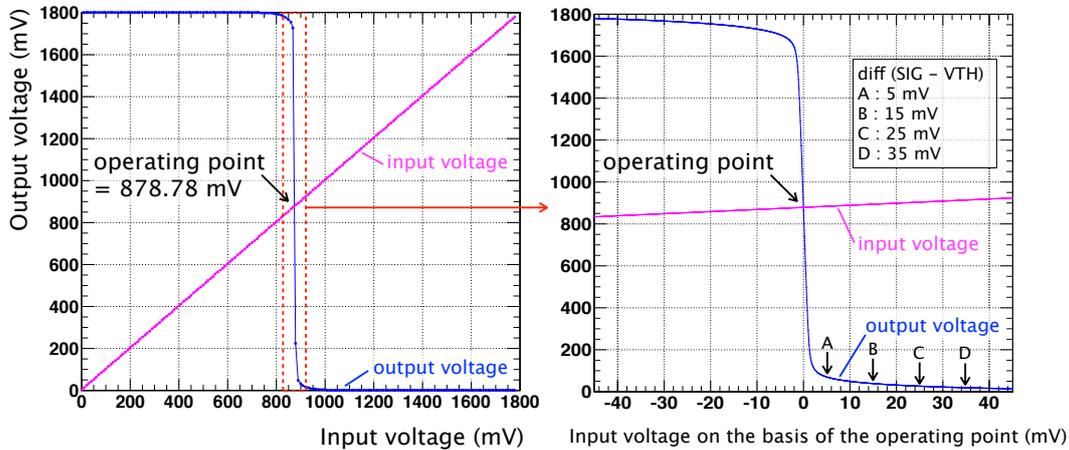
In SOIPIX, the parasitic capacitance is large because the distance between the sense node and the transistor layer is very short (i.e.,  $\sim 200$  nm). The design of a general large-scale integration circuit requires careful consideration of the difficulties associated with the capacitive coupling of the wiring. Therefore, the design of the SOIPIX is more difficult. To reduce the capacitive coupling of the sense node and circuit layer, we have been developing a Double-SOI wafer [11], which has an additional conduction (middle silicon) layer between the sensor and the circuit. The capacitive coupling can be reduced by fixing the potential of the middle silicon layer.

### 4.4 Reason for the Long Logic Conversion Time

The long logic conversion time in Figure 6 appears to be the characteristic of a comparator circuit. From many test results, we showed that this conversion time was dependent on the signal level and VTH. Figure 8 shows the analog signal waveform for X-ray injection from  $^{109}\text{Cd}$  by changing the VTH. The CDS\_RSTV voltage is 400 mV. VTH was manually set from 440 to 470 mV in 10 mV steps. Because the signal level of  $^{109}\text{Cd}$  is  $\sim 475$  mV, the difference between the signal level and the VTH [=  $\text{diff}(\text{SIG} - \text{VTH})$ ] is from 35 to 5 mV. In Figure 8, the horizontal axis represents the time for the X-ray signal readout processing, and the vertical axis represents the voltage based on the pedestal level. Time is required for logic reversal such that the difference between the signal level and the VTH is small. This time is  $\sim 5 \mu\text{s}$  at the maximum. This is exactly the characteristic of a comparator circuit (an inverter circuit in this case), as confirmed by HSPICE circuit simulation.



**Figure 8:** Analog signal waveform of X-ray injection of  $^{109}\text{Cd}$  ( $= 22.2$  keV) by changing the threshold voltage. The CDS\_RSTV voltage is 400 mV. The VTH is every 10 mV from 440 to 470 mV. Because the signal level of  $^{109}\text{Cd}$  is  $\sim 475$  mV, the difference between the signal level and the VTH [=  $\text{diff}(\text{SIG} - \text{VTH})$ ] is from 35 to 5 mV.



**Figure 9:** Input–output characteristics of the first stage of the comparator (i.e., inverter) circuit by HSPICE circuit simulation. The operating point is 878.78 mV. The left graph shows all input ranges (0–1800 mV). The right graph shows a magnified view near the operating point. In the right graph, the x axis is re-zeroed at the operating point.

#### 4.5 Reason for the Change in the Analog Signal

The change in the analog signal in Figure 6 is due to the behavior and the layout of the comparator circuit. This is confirmed for a value of 5 mV for  $\text{diff}(\text{SIG} - \text{VTH})$  in Figure 8. To understand this phenomenon, further information about the comparator circuit is required. In the pixel, the comparator circuit consists of a CMOS inverter circuit. Figure 9 shows the input–output characteristics of the first stage of the CMOS inverter circuit by HSPICE circuit simulation. The operating point is 878.78 mV. The logic is reversed on the basis of this point. Thus, the output voltage of the CMOS inverter circuit changes as per the difference between the signal level and the VTH (Figure 9 on the right). A larger through-current is obtained for a smaller value of  $\text{diff}(\text{SIG} - \text{VTH})$ . Because the analog and digital power supply lines are not separated in the pixel, the consumption of local current influences the analog circuitry by a voltage drop. The reason  $^{55}\text{Fe}$  has shifted from the linear fitting in Figure 5 is because of this change in the analog signal.

## 5. Conclusions

We have been developing an event-driven SOIPIX (XRPIX series) for future X-ray astronomical satellite missions. In our previous study, event-driven readout was successful. However, a phenomenon, which we only partly understood, was observed. Since that time, it has been understood that these problems were based on two main causes. One is the cross-talk including the circuit layer and a sense node. This is peculiar to the SOIPIX, and we have to consider the capacitive coupling for layout design. The other is the characteristic of an inverter chopper-type comparator circuit. We therefore expect that the next design will show a clear improvement.

## Acknowledgments

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