

CMS Tracker Upgrades: R&D Plans, Present Status and Perspectives

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The present CMS pixel detector designed for a luminosity of $10^{34}\,\mathrm{cm^{-2}s^{-1}}$ will have to be replaced at the end of 2016. The new upgraded detector will have higher tracking efficiency and lower mass with four barrel layers and three forward/backward disks to provide a hit coverage up to absolute pseudorapidities of $|\eta| < 2.5$. In a second stage, in order to maintain its physics reach during the high luminosity phase of the LHC (HL-LHC), when the machine is expected to deliver an instantaneous luminosity of $5\times10^{34}\,\mathrm{cm^{-2}s^{-1}}$ for a total of $3000\,\mathrm{fb^{-1}}$, CMS will build a new tracker, comprising a completely new pixel detector and outer tracker. The ongoing R&D activities on both pixel and strip sensors are presented. The present status of the Inner and Outer Tracker projects are illustrated, and the possible perspectives are discussed.

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1. Introduction

During the next years, CERN will pursue an extensive upgrade program of the LHC and its injector complex. The LHC upgrades will make several long shutdowns of the LHC necessary. Finally, this will lead to further improved beam parameters. The most relevant parameters under change from the experiments' point of view are the instantaneous luminosity, manifesting itself in the average number of pile-up events per bunch crossing, and the delivered integrated luminosity, affecting the expected radiation damage. An overview of the prospective LHC beam parameters as well as the schedule of the long shutdowns is illustrated in Figure 1.

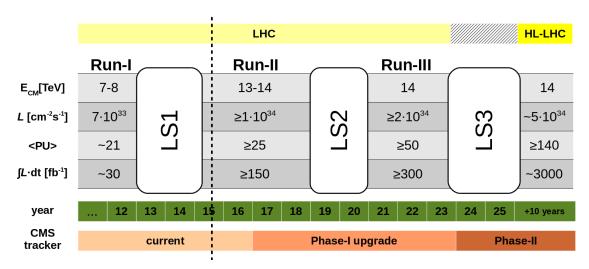


Figure 1: Long-term LHC schedule [1] and the corresponding schedule for the CMS tracker upgrade program. The given values for (instantaneous/integrated) luminosity and pile-up are only approximate numbers in order to sketch the working environment of the tracker.

It is clear that the LHC experiments need to follow the machine upgrades in order to be able to cope with the more demanding experimental conditions. The CMS experiment [2] pursues a rich synchronized upgrade program. In this paper, the focus is put on the upgrade program of the CMS silicon tracker. The tracker upgrade is organized in a two stage approach as shown in Figure 1. In a first stage (Phase I), the CMS pixel detector is replaced in an extended year-end technical stop of the LHC between 2016 and 2017 with a new detector. This is necessary in order to maintain a high hit finding efficiency for the larger hit rates expected in LHC Run II (2015-2018) and Run III (2021-2023). The pixel Phase I upgrade is currently in the production/assembly phase. In a second stage (Phase II), CMS will upgrade the whole central tracker (pixel and strip detector) during LS3, which matches the high-luminosity upgrade of the LHC (HL-LHC). This upgrade becomes necessary because of the further increased hit rates, expected radiation doses and harsher pile-up conditions. In the following, the status and perspectives of both upgrade programs are discussed.

2. CMS Phase I Pixel Upgrade

2.1 Limitations of the Present CMS Pixel Detector

The present CMS pixel detector has performed extremely well during LHC Run I with a hit

resolution of $\sigma_{r-\phi} < 10 \,\mu\text{m}$ and $\sigma_z = 20 - 40 \,\mu\text{m}^1$ and an average hit finding efficiency of more than 99%. The detector has been designed for an integrated luminosity of $500 \, \text{fb}^{-1}$ and instantaneous luminosities of $L = 1 \cdot 10^{34} \, \text{cm}^{-2} \text{s}^{-1}$. This corresponds to an average number of pile-up events of about 25.

Both parameters will increase before LHC LS3 such that performance limitations due to data losses at higher occupancy and trigger rates, due to the higher fake rate, and due to radiation damage are expected. For these reasons, the pixel detector will be replaced before LS3 [3].

2.2 Detector Geometry

The CMS Phase I pixel detector will feature several improvements in its geometry. A comparison between the old and the new geometry is shown in Figure 2. The most striking feature is the extension of the pixel detector by an addition layer/disk. Thus, a four-hit-coverage up to a pseudorapidity of $|\eta| < 2.5$ will be ensured. The first pixel layer will be placed closer to the beam pipe $(r_1 = 43 \rightarrow 29 \, \text{mm})$, which is possible because a smaller beam pipe was installed during LHC LS1. In the forward region, the pixel modules will be arranged in a turbine-like geometry. The tilt and rotation of these modules will ensure an optimal charge sharing between the pixels and, thus, an improved hit resolution.

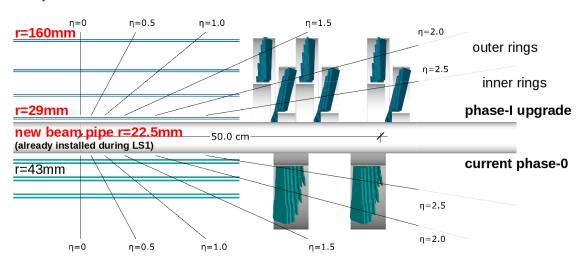


Figure 2: Detector geometry of the CMS pixel Phase I upgrade detector.

2.3 Material Budget

In Figure 3, the material budget in terms of radiation lengths of the Phase I upgrade pixel detector compared to the present pixel detector is shown. It is eye-catching that although an additional pixel layer is added, the used material is even a bit lower than in the present detector. This is possible because the electronic boards and connectors, which caused a significant amount of material

¹The coordinate system adopted by CMS has the origin centered at the nominal collision point inside the experiment, the *y*-axis pointing vertically upward, and the *x*-axis pointing radially inward toward the center of the LHC. Thus, the *z*-axis points along the beam direction toward the Jura mountains from LHC Point 5. The azimuthal angle ϕ is measured from the *x*-axis in the *x*-*y* plane and the radial coordinate in this plane is denoted by *r*. The polar angle θ is measured from the *z*-axis. Pseudorapidity is defined as $\eta = -\ln(\tan(\theta/2))$. [2]

in the forward region, have moved to a higher pseudorapidity range. Also the support structure has been redesigned. For the barrel pixel detector, a system of very lightweight carbon fiber reinforced polymer (CFRP) and Airex is used with cooling loops as the backbone. The forward pixel detector uses Thermo Pyrolytic Graphite (TPG) for the individual blades. Another important ingredient for the reduced material budget is the use of very lightweight 2-phase CO_2 cooling. The corresponding cooling plant has already been installed and commissioned during LHC LS1. Finally, the power connections will stay unchanged compared to the present pixel detector although the number of channels is significantly increased. This makes a more evolved powering concept necessary. DC-DC converters have been developed, produced, and will be installed in order be able to reuse the present cable plant and power supplies.

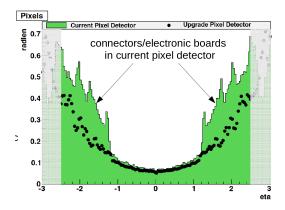


Figure 3: Material budget of the CMS pixel Phase I upgrade detector (data points) compared to the present pixel detector (green).

2.4 Module Design

One major upgrade concerns the pixel detector modules. The building blocks of a typical module are shown in Figure 4. It consists of the silicon sensor which is bump-bonded to 16 readout chips (ROCs). A Token-Bit-Manager (TBM) coordinates the module readout and a flex print high density interconnect (HDI) connects the different components. The sensor is completely unchanged compared to the present pixel detector. All other components received some updates. The new ROC is based on the current ROC PSI46, but features a few improvements, like on-chip digitization (8 bit ADC), increased buffer sizes of the hit buffer ($32 \rightarrow 80$) and time stamp buffer ($12 \rightarrow 24$), increased radiation tolerance, and lower noise/charge threshold ($3200e^- \rightarrow 1900e^-$). Due to the most challenging conditions in the first pixel layer a dedicated ROC for this layer is currently under development. Also the TBM received an update: It is also now a digital chip, improving from $40\,\mathrm{MHz}$ analog coding to $160\,\mathrm{Mbit/s}$ digital coding with an overall module outbound data bandwidth of $400\,\mathrm{Mbit/s}$. Concluding, all the module components are now ready to cope with the expected higher integrated and instantaneous luminosities of Run II and Run III.

2.5 Time Schedule

At the time of the writing of this paper, the module production for pixel layer 2-4 and disks 1-3 is ongoing. The production for the small number of modules for layer 1 will happen mid



Figure 4: Schematic picture of the components of the pixel Phase I upgrade modules.

of 2016 once the layer 1 ROC is ready. The procedure of module production and qualification is described in [4]. In parallel to the module production the mechanics for the shells and disks as well as the service cylinders are being produced and assembled. This will be done by the end of March 2016. By the end of 2015, the module mounting as well detector integration and testing will sequentially start such that the CMS pixel Phase I detector will be ready for installation by the end of 2016.

3. CMS Phase II Tracker Upgrade

3.1 Design Principles of the CMS Phase II Tracker

According to Figure 1, the experimental conditions become much more challenging after the high-luminosity upgrade of LHC. This make fundamental upgrades of the whole detectors necessary as described in detail in Reference [5]. Thereby, the Phase II upgrade of the CMS tracker rests on four pillars:

- In order to deal with the increased hit density due to the enormous number of pile-up events
 of at least 140, a finer granularity of the whole tracker (pixel and strip detector) by a factor
 of 4 6 is necessary.
- The level 1 calorimeter and muon triggers will be no longer sufficient to reduce the enormous event rate in the high-luminosity regime. Thus, it is desirable to make also tracking information available on that trigger level in order to reject events with only low momentum tracks or to trigger on high-momentum tracks.
- The Phase II tracker needs to be extremely radiation hard, capable to withstand a radiation dose equivalent to at minimum 3000 fb⁻¹ without significant performance degradation.
- As particle reconstruction in the forward direction becomes more and more of interest (vector boson fusion, vector boson scattering, forward b-jet tagging), the pixel instrumentation is extended to this detector region up to a pseudorapidity of $|\eta| < 4.0$. The geometry of the updated CMS Phase II tracker is depicted in Figure 5. It should be noted that an alternative geometry with tilted barrel modules, which are oriented towards the interaction point, is also under investigation.

In the following, the strategies followed in the R&D programs for the CMS Phase II pixel and strip detector in order to meet the described requirements are outlined.

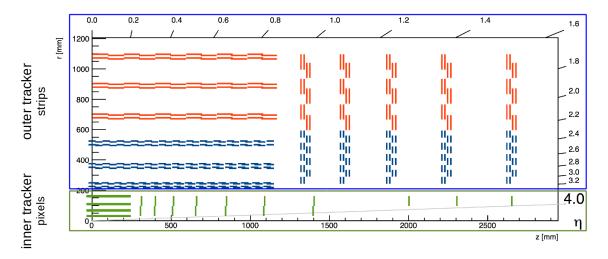


Figure 5: Quadrant view of the detector geometry of the CMS Phase II tracker. The green box marks the inner tracker (pixel detector), whereas the blue box indicates the outer part of the central tracker (strip detector).

3.2 Inner Tracker Sensor Option, Pixel Size and Readout

Especially in the first pixel layer, a total particle flux of about $2 \times 10^{16} \, n_{eq}/cm^2$ is expected. This means that charge trapping due to defects in silicon will reduce the cluster charge and, thus, the signal hit efficiency. A solution to this problem is to reduce the drift distance in the sensor, which also reduces the probability for charge trapping. Two silicon sensor options are under consideration: In Figure 6 (left), the concept of thin planar sensors is sketched. The thickness d and, thus, drift length L in this kind of sensors is smaller than $200\mu m$. In irradiation studies, it has been found that a signal of 4000e⁻ is still collectible at a bias voltage of 800 V after an irradiation of $1.3 \times 10^{16} \, n_{eq}/\text{cm}^2$. As this sensor option makes use of relatively cheap and well-established production procedures, it is considered as option for the whole pixel detector. An alternative to the thin-planar sensors design is 3D technology, as depicted in Figure 6 (right). In this case the doping is done in vertical pillars. This allows to reduce the drift length L significantly, however, the technology is much more challenging compared to the planar sensor types. Irradiation studies showed that a signal of about $7000e^-$ at a bias voltage of 150 V after an irradiation of $5 \times 10^{15} \, n_{eq}/cm^2$ is measureable. So, this type of sensors is especially interesting for the inner pixel layers. The final decision on the sensor design will be based on performance, radiation tolerance, and cost/yield arguments and will be taken in the near future.

The pixel size will be reduced by a factor of six compared to the Phase I pixel detector. Different pixel aspect ratios $(50 \times 50 \, \mu \text{m}^2, 25 \times 100 \, \mu \text{m}^2)$ are currently under investigation. Also the option to have larger pixels in the outer region of the pixel detector is considered in recent performance simulations.

For the CMS Phase II pixel detector, a completely new read-out chip will be developed. Due to reasons of power consumption and radiation hardness, it will be based on 65 nm CMOS technology. It needs to be able to process hit rates of $2 \, \text{GHz/cm}^2$ and at the same time comply with the increased level 1 trigger rate (1 MHz) and trigger latency of $12.5 \, \mu \text{s}$. The chip is supposed to

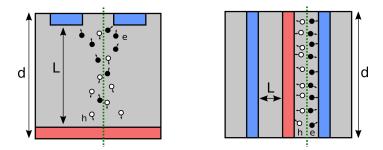


Figure 6: Schematic picture of considered sensor options for the Phase II pixel detector. Left: Thin-planar sensor. Right: 3D sensor.

feature a very low noise level such that charge thresholds of 1000e⁻ are possible. As the ROC requirements overlap to a large extend with ATLAS pixel upgrade requirements, a dedicated joined RD collaboration has been formed [6] which is going to present a demonstrator chip in 2016.

3.3 Outer Tracker Modules and Prototyping

In order to make track information available at the level 1 trigger level (40 MHz) not all hits can be read out by the front end electronics. A hit belonging to a high p_T track ("stub") needs to be found already at the module level. This is possible combining two concepts: First, a module consists of two sensor layers, which are separated by $1-4\,\mathrm{mm}$. Thus, in a magnetic field the track curvature can be estimated by comparing the hit positions in both layers. Second, the read-out chip needs to be electrically connected with wire-bonds to both sensor layers in order to run the stub finding algorithm on the module level. This is possible by using a flexible connector board (flexible hybrid), which can be bent by 180° .

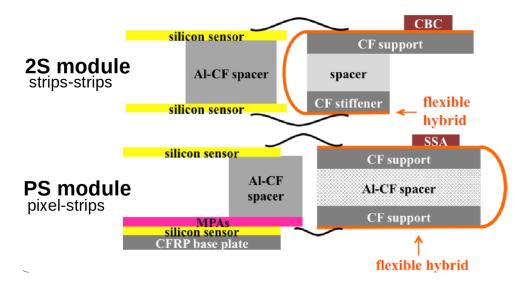


Figure 7: Cross section of the two foreseen module types in the outer Phase II tracker. Top: 2S-Module with the CMS Binary Chip (CBC) as readout ASIC. Bottom: PS-Module with the Short Strip ASIC (SSA). The pixelated sensor is bump-bonded to the Macro Pixel ASIC (MPA), which further connects to the flexible hybrid. All flexible components are supported by carbon fiber (CF) structures.

In the Phase II outer tracker, two different types of modules will be used. In the outer part of the strip detector (red marks in Figure 5), a combination of two strip sensor layers will be used (2S modules). The sensor area amounts to $10 \times 10 \, \text{cm}^2$ with a strip size of $5 \, \text{cm} \times 90 \, \mu \text{m}$. There are in total $2 \cdot 1016$ strips per module. In the inner part of the strip detector (blue marks in Figure 5), a combination of one strip and one macro-pixel layer will be used (PS modules). The sensor area amounts $5 \times 10 \, \text{cm}^2$ and, thus, is smaller compared to the 2S module. For the strip sensor layer a strip size of $2.4 \, \text{cm} \times 100 \, \mu \text{m}$ is implemented with in total $2 \cdot 960$ channels per module. The macro-pixel layer features pixel sizes of $1.5 \, \text{mm} \times 100 \, \mu \text{m}$ with in total $32 \cdot 960$ pixels per layer. The macro-pixels are bump-bonded to the MPA readout-chip. Due to the pixel segmentation, the PS module also offers some resolution in the z direction. Schematic pictures of both module types are shown in Figure 7.

The definition of the module design is well advanced and first prototypes exist. A down-scaled 2S module has been built in 2013 and since then operated in different test beams. It could be shown that the stub-finding logic works by simulating the track bending by rotating the prototype module with respect to the beam axis. Also a down-scaled prototype of the pixel part of the PS module has been developed recently and will be investigated in the future.

4. Conclusions

The CMS tracker faces a rich R&D and upgrade program within the next 20 years. In the near future the CMS pixel detector will be replaced by an improved, 4-layer pixel detector based on digital read-out. The production is ongoing and there are no obstacles in sight preventing the installation by the end of 2016. Concerning the mid-term future, CMS has recently proposed the upgrade scenarios for the HL-LHC including the upgrade of the CMS tracker. The final Phase II pixel detector concept is still under development evaluating different options. The Phase II outer tracker concept is already well advanced and for many aspects the prototyping phase has already started.

References

- [1] F. Bordry, LHC schedule beyond LSI, http://lhc-commissioning.web.cern.ch/lhc-commissioning/schedule/LHC%20schedule%20beyond%20LS1%20MTP%202015_Freddy_June2015.pdf, presented to the CERN Scientific Policy Committee and Finance Committee in June 2015.
- [2] S. Chatrchyan et al. [CMS Collaboration], *The CMS experiment at the CERN LHC*, JINST 3, S08004 (2008).
- [3] CMS Collaboration, CMS Technical Design Report for the Pixel Detector Upgrade, CERN-LHCC-2012-016 (2012).
- [4] B. Freund, *Module Production and Qualification for the Phase I Upgrade of the CMS Pixel Detector*, EPS-HEP 2015 proceedings.
- [5] CMS Collaboration, *Technical Proposal for the Phase-II Upgrade of the CMS Detector*, CERN-LHCC-2015-010 (2015).

[6] RD53 Collaboration, *RD Collaboration Proposal: Development of pixel readout integrated circuits for extreme rate and radiation*, CERN-LHCC-2013-008 (2013).