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An Associative Memory Chip for the Trigger System of the ATLAS Experiment

Seyed Ruhollah Shojaii*

On behalf of the FTK Collaboration
INFN - Sezione di Milano, Via G. Celoria 16, 20133 Milano, Italy
E-mail: sshojaii@cern.ch

The AM06 is the 6th version of a large associative memory chip designed in 65 nm CMOS technology. The AM06 operates as a highly parallel ASIC processor for pattern recognition in the ATLAS experiment at CERN. It is the core of the Fast TracKer electronic system, which is tailored for on-line track finding in the trigger system of the ATLAS experiment. The Fast TracKer system is able to process events up to 100 kHz in real time. The AM06 is a complex chip, and it has been designed combining full-custom memory arrays, standard logic cells and IP blocks. It contains memory banks that store data organized in 18 bit words; a group of 8 words is called a pattern. It accepts as input 16-bit words at a rate of 100 MHz, which are serialized with an 8b/10b encoding, thus giving a serial data rate equal to 2 Gbit/s. The chip silicon area is 168 mm^2; it contains 421 millions of transistors and it stores 2^{17} patterns. Moreover, the associative memory is suitable also for other interdisciplinary applications (i.e., general purpose image filtering and analysis). In the near future we plan to design a more powerful and flexible chip in 28 nm CMOS technology.

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*Speaker.

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1. Introduction

After the next upgrade, the Large Hadron Collider (LHC) will reach a luminosity of $2-3\cdot 10^{34}$ cm^{-2} s^{-1}, and experiments will produce a huge amount of data, thus requiring a tight selection of events to be transferred to the mass storage system [1].

The Fast TracKer (FTK) [2] is an electronic system in the ATLAS experiment [3] that rapidly finds and reconstructs tracks in the inner silicon detector layers (pixel and strip), for every event that passes the Level-1 trigger. It uses 12 logical layers of the silicon detector over the full rapidity range covered by the barrel and end-caps; 4 for pixel layers, including the new Insertable B-Layer (IBL), and 8 for the strip SemiConductor Tracker (SCT), including both the axial and stereo sides on each of its' 4 physical layers.

2. FTK architecture

Figure 1 shows a schematic overview of the whole FTK system. The FTK receives the hits at full rate as they are sent from the pixel and SCT Read Out Drivers (ROD), following a Level-1 trigger accept. After processing, FTK fills the data acquisition Read Out System (ROS) with the helix parameters and hits for all tracks having a transverse momentum p_T above a minimum value, typically 1 GeV/c.

The pixel and strip data are transmitted from the RODs on S-LINK fibers and received by the Input Mezzanines (IM) sitting on the Data Formatter (DF) cards: the IMs perform one or two dimensional cluster finding, for the strip and the pixel layers, respectively. The DFs reorganize the data into solid-angle towers and transmit the cluster centroids (hits) to the Data Organizers (DO). The DOs are smart databases mapping the received full resolution hits onto lower-resolution hits (called superstrips). The superstrips are matched against pre-calculated patterns stored in Associa-

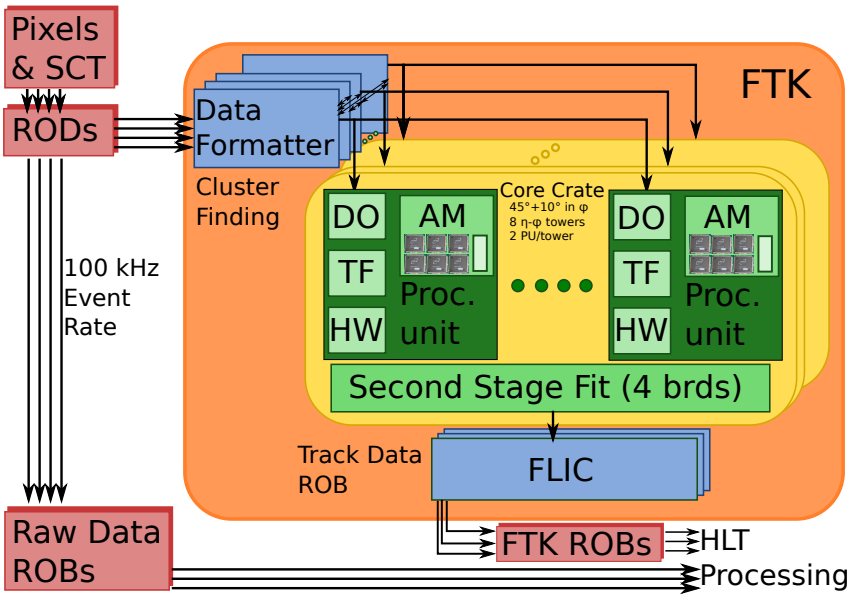

Figure 1: Schematic overview of the whole FTK system

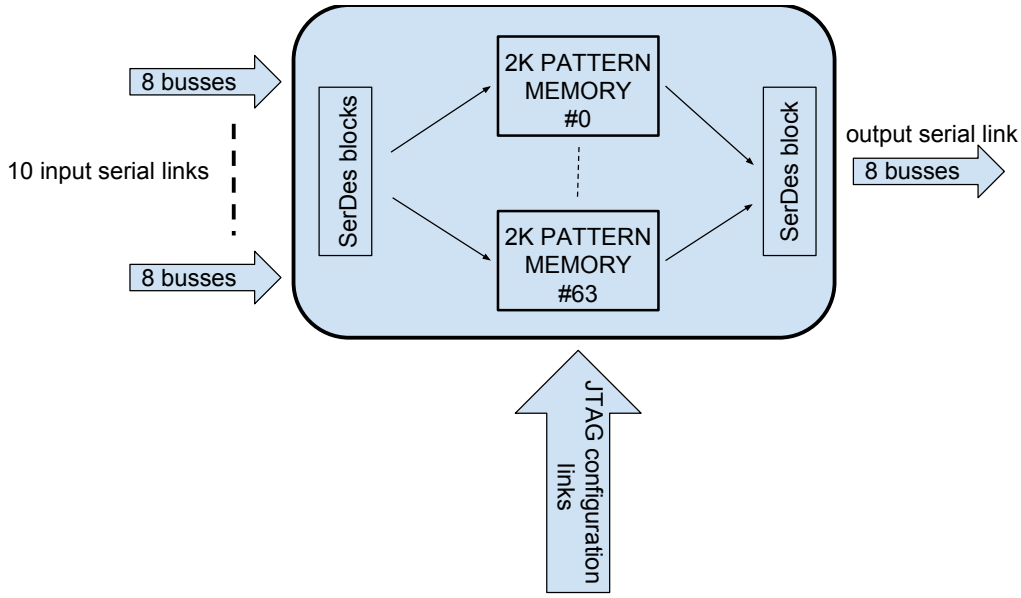

Figure 2: AM06 architecture includes 64 of 2K pattern memory blocks which are interfaced by SerDes blocks

tive Memories (AMs); these patterns have been determined from a full ATLAS simulation of single tracks. Patterns matched in AMs with the requested number of superstrips are called "roads". The full resolution hits in the DO are stored in a format that allows rapid access based on the pattern recognition road identifier ("road ID").

The associative memory boards contain a very large number of stored patterns, which correspond to the possible combinations of a superstrip in each of 8 silicon layers for real tracks. The AM is a massively parallel system in that all pre-calculated patterns see each silicon hit nearly simultaneously [5]. As a result, pattern recognition in FTK is completed shortly after the last hit has been transmitted from the silicon RODs. When a pattern matches 7 or 8 layers hits, the AM sends the road ID number back to the Data Organizer which fetches the associated full resolution hits and sends them and the road number to the Track Fitter (TF), which provides a high resolution fit of track helix parameters. After fitting, the Hit Warrior (HW) function carries out duplicate track removal in each road, among those 8-layer tracks which pass the fit quality cut. This completes the "stage-1" of track finding.

When a track passes the stage-1 criteria, the road number and hits are sent to the Second Stage Boards (SSB). In addition, the SSBs receive from the DFs the cluster centroids in the 4 layers not used in stage 1. The track is extrapolated into the 4 additional layers, nearby hits are found, and a full 12-layer fit is carried out. SSB output tracks, consisting of the hits on the track, the fit parameters, the helix parameters, and a track quality word that includes the layers with a hit, are sent to the FTK-to-Level2 Interface Crate (FLIC). The FLIC organizes the tracks and sends them to the High Level Trigger ROSs using the standard ATLAS protocols, and carries out monitoring functions.

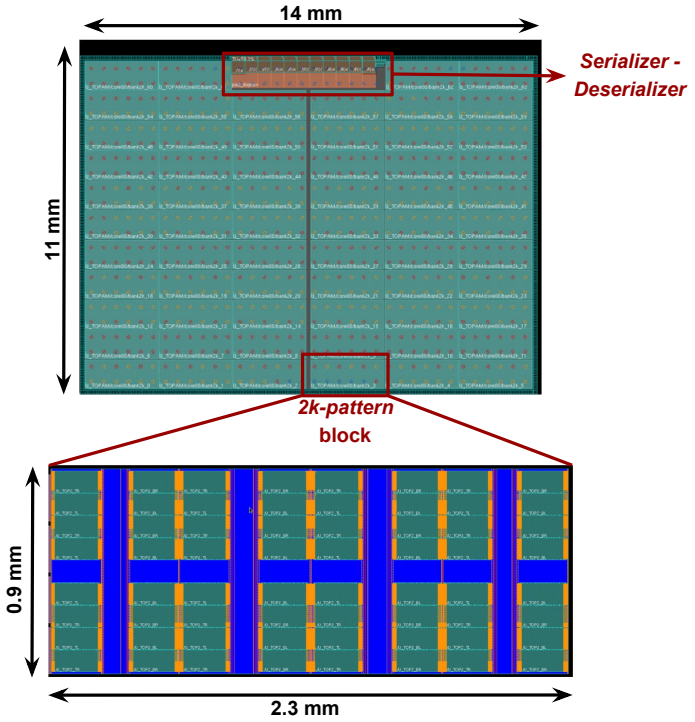

Figure 3: Layout of the whole AM06 chip and one of the memory blocks

3. The associative memory chip

The AM chip stores the pre-calculated tracks and makes a bitwise comparison in parallel with the input data; the addresses of matching patterns are delivered at the output [5].

The AM06 is the 6th version of the AM chip and the third one designed in 65 nm CMOS technology. Smaller prototypes were designed to demostrate the chip functionality and performance at the 65 nm node: the AM04 [6], and the two versions of the AM05 [7].

The AM04 employed conventional memory cells, with NAND- and NOR-type associative memory cells [8]. A new type of associative memory cell, called XORAM and based to the XOR logic function [9], was specifically designed for the FTK project and integrated in the two versions of the AM05 chip. The second version of the AM05 chip includes also serializer-deserializer (SER/DES) blocks provided by Silicon Creation [10], which are needed for serial comunication between the AM chips and between the AM chips and the DOs. Input 16-bit words have a rate of 100 MHz, and are serialized with an 8b/10b encoding, thus giving a serial data rate equal to 2 Gbit/s. SER/DES input blocks convert the serial input to parallel data, which are sent to the core memory blocks. The use of a serial communication protocol simplifies the design of the AM board.

The AM06 architecture, sketched in figure 2, is based on the SER/DES interface and on the AM core. The input buses are organized in 10 serial links, each of them receiving serialized data. The associative memory core is made of 64 blocks, each of them containing 2 k patterns. The core stores the patterns which the AM06 should find among the incoming data. Figure 3 shows the floorplan of the AM06 chip, and a detail with the layout of one of the 64 memory blocks.

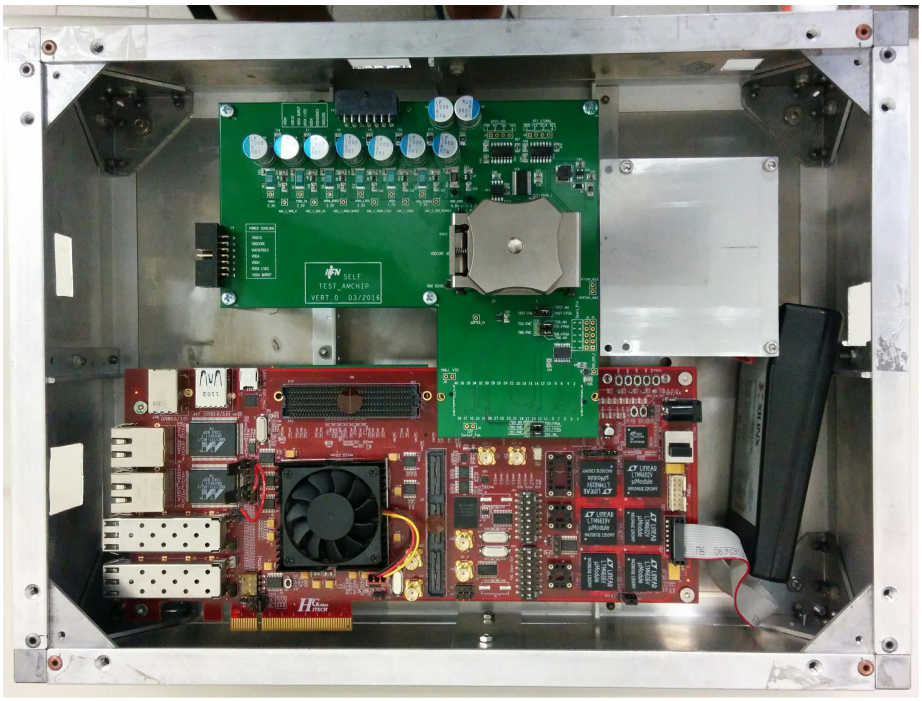

Figure 4: AM06 test setup to test a large number of chips in a company

The AM06 has a standard JTAG interface for configuration and testing. One of the JTAG registers contains the ID code of the AM chip family.

4. AM06 characterization and test

The AM06 chip has been characterized with the test system at a INFN laboratory in Milano. The test setup is shown in figure 4. It is made of an FPGA board with a Xilinx Virtex6 FPGA, and a dedicated mezzanine board with a zero-insertion-force socket for the device under test.

The test procedure is remotely controlled by a PC connected to the internet. A set of routines written in Python allow us testing the AM chip in different conditions.

The test sequence has 100 % coverage against single bit errors in the AM core blocks, in the readout, and in the main functions used to configure and run the AM chip.

From the eye diagram of one of the AM06 serial links at 2 Gbit/s, shown in figure 5, we can observe that the jitter is about 25 ps. A similar result has been obtained for all the chip serial links, thus confirming the good quality of the serial communication.

7500 AM06 chips are being fabricated for the FTK system. Therefore, the test setup is finalized to test a large number of chips in a company. The test procedure is automated as much as possible and a graphic interface has been developed to simplify the use of the test system.

The test setup has been assembled successfully at Microtest srl in Altopascio, Italy, where the production lot of 7500 AM06 chips will undergo the test. The test time for each chip has been kept short enough, to limit test costs; moreover, the test procedure is very user-friendly and does not require a specialized training of the operator.

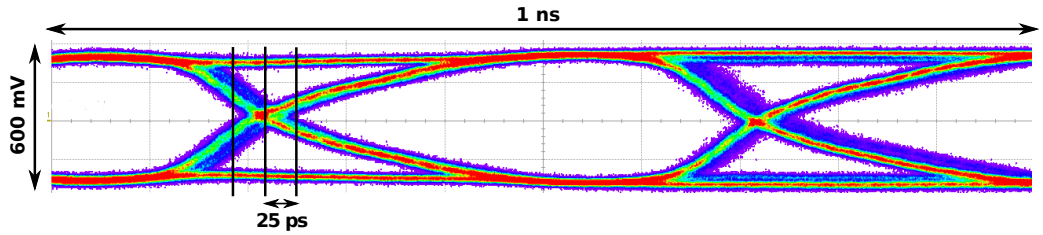

Figure 5: Eye diagram of AM06 serial link at 2 Gbit/s

5. Conclusion

The AM06, the 6th version of a large Associative Memory chip for the FTK system is designed in 65 nm CMOS technology. The AM06 chip has been designed combining full-custom memory arrays, standard logic cells and IP blocks. It contains memory banks that store data organized in 18 bit words; a group of 8 words is called a pattern. The chip silicon area is 168 mm^2 ; it contains 421 millions of transistors and it stores 2^{17} patterns. The FTK system includes 7500 AM chips, therefore, the test setup and the measurement software have been developed to define a standard test procedure suitable for the industrial test of a large number of chips.

The laboratory characterization shows a full functionality of both the AM06 and the test system. The setup has been implemented successfully at the company and the operator is capable to perform the test of a large number of AM06 chips without any interaction with the test setup developers.

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