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A multi-channel PCI Express readout board proposal for the pixel upgrade at LHC

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After having designed and commissioned the readout electronics currently implemented in the Insertable B-Layer, Layer 1 and Layer 2 of the ATLAS Pixel Detector (B-Layer and Disk readout electronics is under commissioning), we have designed a new readout electronic board looking primarily at the upgrade of the LHC Pixel Detectors. Two prototypes of a PCI Express board, namely Pixel_ROD, featuring all the minimal input-outputs interfaces to address the future front-end readout electronics, have already been fabricated and tested. The digital protocols used for the GBTx and for the RD53A chips have been investigated and we have been able to emulate physically a data acquisition chain interfacing with these components.

The Pixel_ROD board might fit a variety of applications, from a test stand to qualify the RD53a chips that are currently under fabrication to a front-end physical emulator, designed via firmware, adaptable to any detector. As we have been working for years on the hardware and firmware of the IBL ReadOut Driver (ROD) card, we can also use this prototype board as a multi-channel FE-I4 emulator. An entire module of a Pixel Detector can be emulated by generating a very fast flux of data according to the desired protocol: FE-I4 compatible format for the current detector of ATLAS experiment and Aurora 64b/66b protocol for the next RD53A chip that will be used for ATLAS and CMS Pixel Detectors. The Pixel_ROD board in fact, features internal high-speed transceivers to interface easily from and to any other electronic board, electrically and/or optically, at the current desired bandwidth of the experiments for LHC. We have already started to carry out some tests, with the supervision of the ATLAS TDAQ collaboration, to interface with the FELIX card, either for data-acquisition or trigger functions, in view of any application towards the LHC phase-2 upgrade.

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1. Introduction

Over the last years the ATLAS Pixel Detector has been upgraded in terms of sensors and readout electronics. In particular for the Insertable B-Layer (IBL) [1] the sensors, which are read out through a new ASIC called FE-I4 [2], are interfaced with off-detector electronics composed of a back-of-crate (BOC) and a readout-driver (ROD) [3] card. By contrast, the Layers 1 and 2 have maintained the current sensors and have updated only the off-detector readout electronics (IBL BOCs and RODs) to stand the continuous increment of luminosity of the collider at CERN. All these layers have already been updated and have taken data. The remaining two layers of the ATLAS Pixel Detector, the B-Layer and the Disks, are under commissioning and their upgrade will be completed during the technical stop of 2018.

To continue the challenge of upgrading the readout electronics for the LHC Pixel Detectors we have designed and fabricated an 8-lane PCI Express board (namely Pixel_ROD) with a variety of input-output ports, electrical and/or optical, to interface with the current and future front-end electronics chains foreseen for the LHC upgrade. In addition, this board has been designed as an upgrade of the current ATLAS Pixel off-detector readout system, which is composed of two BOC and ROD boards originally designed for IBL only. In this way, we have designed a schematic architecture with the chance to profit from the IBL firmware that we have designed and maintained for years. Hence, we have used two different FPGAs with the same modularity of the IBL ROD card. Left picture of Figure 1 shows how the firmware designed for the IBL detector, currently implemented on the BOC main FPGA (BMF), on the BOC Control FPGA (BCF) and on the ROD master and slave FPGAs, can fit the Pixel_ROD board. Right picture of Figure 1 shows again the Pixel_ROD with the on-board high-speed buses that extend the capability of the board to communicate I/O data at the speed of the ser-des transceivers (12 Gb/s). In fact, one of the first tests for the board was to cope with the protocols used in the GBTx [4] and RD53A [5] chips. Both communications have already been tested via on-board optical transceivers at a speed up to 12 Gb/s in a loopback configuration.

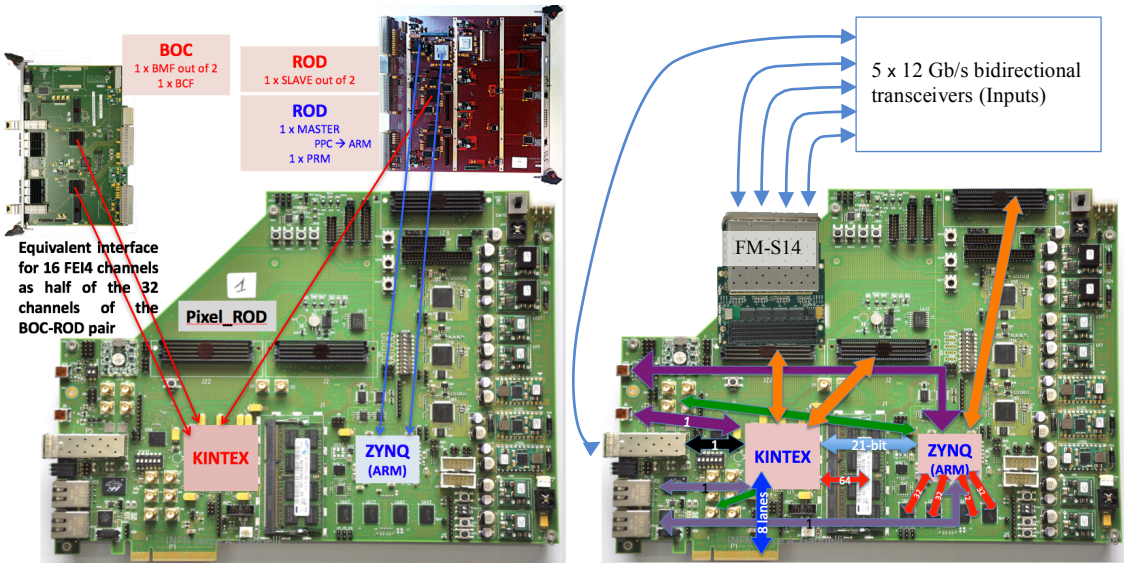


Figure 1: Pixel_ROD board with the BOC-ROD equivalent interface (left) and the interconnection buses between the Kintex and the Zynq FPGAs along with the input optical links (right)

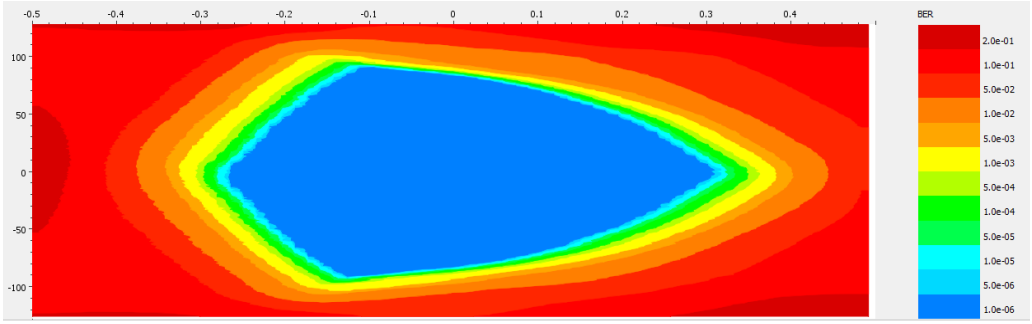
In particular, the right picture of Figure 2 shows a possible data-taking configuration with 5 input optical fibers, 4 via a mezzanine card (FM-S14 [6]) connected electrically to a FPGA Mezzanine Card (FMC) connector, and 1 small-form-factor pluggable (SFP) input. All these inputs can read data at a rate up to 12 Gb/s, resulting to a 60Gb/s input bandwidth. The output rate, using an x8 lane PCI Gen2 bus, can run up to 5 GT/s (Giga-Transfer/s that, for 8 lanes and 8b/10b encoding, results to a 4 GB/s output rate). So far, in our laboratory, we have carried out many 2.5 GB/s read-write tests over the PCI Express bus, by connecting the PC motherboard to the Kintex DDR3 memory in Direct Memory Access (DMA) mode, bypassing the Kintex transceivers.

Technically, the Pixel_ROD board features two Xilinx FPGAs: the Kintex XC7K325T-2FFG900C and the Zynq XC7Z020-1CLG484C, which embeds a physical dual-core ARM Cortex-A9 processor. The Kintex device has 16 internal physical transceivers (GTx) running at up to 12 Gb/s connected to different types of physical ports such as the PCI Express, FMC, SFP and Gb-Ethernet. The Figure 1 shows a 21-bit bus, which is used as an inter-FPGA connection to let the Kintex and Zynq communicate, a 64-bit bus to connect the Kintex with an external 2GB DDR3 memory module and four 32-bit buses to connect the Zynq FPGA to 4 external banks of DDR3 memories (1 GB altogether).

2. Tests

Firstly, using a CERN-made board [7] mounting a GBTx ASIC, we have been physically able to interface with the Pixel_ROD through an optical fiber at a speed of 4.8 GB/s, by emulating a real front-end data acquisition chain using a GBT chip-set.

As far as the RD53A chip interface we are building a demonstrator tool able to emulate a data taking of physical streams, using the Aurora 64b/66b protocol, by connecting two Pixel_ROD boards in a loop-back configuration. One is used to build the expected RD53A emulated data and the other one is used as a receiver. This test was run at data rates up to 10 Gb/s on a single link and in parallel over several links (optical fibers).



Name	TX	RX	Status	Bits	Errors	BER
Ungrouped Links (0)						
Link Group 0 (1)						
Link 0	MGT_X0Y15/TX	MGT_X0Y10/RX	10.000 Gbps	2.421E13	0E0	4.13E-14

Figure 2: Eye diagram of a generic loopback test on SFP connector at: 10 Gb/s, BER ≈ 10^{-14}

Figure 2 shows the eye diagram of a 1-hour test for a high-speed communication that we have carried out to validate the GBT protocol over the SFP connector. These tests are performed also to integrate our work within the ATLAS TDAQ collaboration and in particular with the FELIX group, so to interface with electronic boards called FELIX [8-9]. Eventually the

Pixel_ROD has interfaced with a mini-FELIX card (Xilinx VC709 [10]) by establishing a communication via either GBT (4.8 Gb/s) or Full_Mode (9.6 Gb/s) protocol. For both configurations, the clock (TTC clock) was recovered from the data stream (using the CPLL and QPLL of the GTx transceiver) and was propagated to all the synchronous components of the Pixel_ROD, primarily to the Zynq as master and to the Kintex as slave component, creating a synchronous data acquisition system.

3. Conclusions

The tests carried out so far on the Pixel_ROD have proved the reliability of the board and its capability to be interfaced with other electronics through many different electrical connectors and optical fibres. Furthermore, the first two implementations of important transmission protocols such as the GBT and the Aurora 64b/66b, used in the High Energy Physics research area, have also been successful.

A possible application for this board is a test stand for the ATLAS community to qualify the RD53A chips that are currently under fabrication. In this case the board will interface with the chip and will validate its functional performance. In fact, by exploiting the transceiver channels we are proposing the board as a tool to test, to qualify and to read out the RD53A chips for the new generation of Pixel Detectors at LHC.

Another feasible application is to interface the board with a FELIX card, either for data-acquisition or trigger functions, to help updating any detector that will be upgraded even before the phase-2 of LHC. For this we are settling in Bologna a PCI Express test stand to cope with hardware, firmware and software using our Pixel_ROD board and the mini-FELIX card. The environment is useful in any case to test, in advance, the readout chain for calibration and data taking purposes of any front-end detector.

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