PROCEEDINGS OF SCIENCE

Phase-II Upgrade of the ATLAS Pixel Detector

Matthias Hamer* **on behalf of the ATLAS ITk Community**
University of Bonn
E-mail: hamer@physik.uni-bonn.de

The Large Hadron Collider (LHC) will be upgraded to the High Luminosity-LHC (HL-LHC), which will deliver proton-proton collisions at a much higher instantaneous luminosity than that of present LHC from 2026 on. In order to cope with the significantly higher pile-up at the HL-LHC, the tracking detector of the ATLAS experiment will be upgraded to an all silicon tracking detector, the ATLAS Inner Tracker (ITk), which will consist of a pixel detector in the innermost layers and a strip detector in the outermost layers. There are strong requirements on the ITk pixel detector to perform over ten years in the harsh environment at the HL-LHC, during which the ATLAS experiment is expected to record a dataset of 4000fb^{-1}. The large number of modules in the ITk pixel detector in combination with the limited available space and the expected tracking performance make the design of this detector challenging, in particular the powering scheme and the transmission of the hit data from the front-end electronics to the readout backend at high data rates are more complicated than in the current tracking detector. The expected performance of the ITk pixel detector will, however, enable a rich physics programme, for instance a significantly improved understanding of the Higgs sector.

The 27th International Workshop on Vertex Detectors - VERTEX2018
22-26 October 2018
MGM Beach Resorts, Muttukadu, Chennai, India

*Speaker.

PoS(VERTEX2018)020

1. Introduction

For operation at the High Luminosity-LHC (HL-LHC), the tracking detector of the ATLAS experiment [1] will be upgraded to an all silicon detector, the ATLAS Inner Tracker (ITk). The ITk will consist of two parts, a pixel detector [2] in the innermost layers, and a strip detector [3] in the outermost layers. The ITk will fill the same volume as the current ATLAS Inner Detector (ID), which features a Transition Radiation Tracker in the outermost layers, making both the pixel detector and the strip detector significantly larger than their predecessors; the status of the ongoing design work is summarised in this article.
In Section 2, the requirements on the ITk pixel detector and a candidate layout that fulfils these requirements is presented. Section 3 provides a description of the sensors and front-end electronics of the new detector. The local supports and the services scheme, with an emphasis on powering, readout and monitoring is described on Section 4. In Section 5, the ongoing prototyping activities are summarised, while Section 6 gives an overview on the expected physics performance of the ITk pixel detector.

2. Requirements on and Layout of the ITk pixel detector

The HL-LHC is expected to start colliding protons at a center-of-mass energy of 14 TeV in 2026 and will reach a peak luminosity of 10^{35} cm^{-2}s^{-1} with an average of 200 proton-proton interactions per bunch-crossing. The high collision rate will enable a rich physics program, with a focus on new and high precision measurements in the Higgs sector, in vector boson fusion interactions and in searches for physics beyond the Standard Model. In order to fully exploit the physics potential of the HL-LHC, an upgrade of the ATLAS detector, which will provide a larger coverage and a much better performance at the HL-LHC compared to the current detector layout, is essential.
Many of the physically interesting final states at the HL-LHC feature forward jets. This requires the tracker to cover the large pseudo rapidity region up to $|\eta| = 4$, which will be instrumental for the rejection of pile-up jets by the means of jet-vertex-association. Despite the significantly higher track density at the HL-LHC, compared to Runs 1-3 of the LHC, the occupancy of the tracking detector needs to be kept at low levels to facilitate efficient tracking with a good vertex resolution. The targeted track reconstruction efficiency is $> 99\%$ for muons and pions, and $> 85\%$ for electrons at a fake rate of less than 10^{-5}, which is expected to be achieved by reducing the pixel size significantly compared to the current pixel detector. While this increases the power consumption of the front-end electronics, the overall material in the tracking detector, including the local supports and the services, needs to be kept at a minimum - these goals are met by using low mass carbon local supports with thin cooling pipes and implementing a serial powering scheme to power the readout chips [4].
It is expected that the HL-LHC will deliver a total integrated luminosity of about 4000 fb^{-1} over the course of ten years. With the exception of the innermost two layers, the ITk pixel detector will not be replaceable. This requires the front-end electronics and sensors to operate at high efficiency after receiving a Total Integrated Dose (TID) of about 10 MGy and a total fluence of about $1.4 \cdot 10^{16}$ n$_{eq}$/cm^2.
Figure 1 shows a candidate layout of the ITk pixel detector. It will consist of 5 layers of mod-

ules, which are arranged in three different sections per layer. In the low η region, the modules are placed in parallel to the beam axis (flat section), while modules are placed perpendicular to the beam axis in the high η region (endcaps). In the intermediate η region, the modules will be neither perpendicular nor parallel, but tilted at an angle between 55° and 67° with respect to the beam axis (inclined section). The detector will consist of about 10000 hybrid pixel modules with thin planar sensors in the outermost layers and 3D sensors in the innermost layer. Each pixel will have a size of either $50 \times 50 \mu\text{m}^2$ or $25 \times 100 \mu\text{m}^2$. For the flat section in outermost layer, CMOS modules, are considered as a drop-in solution to replace the hybrid modules.

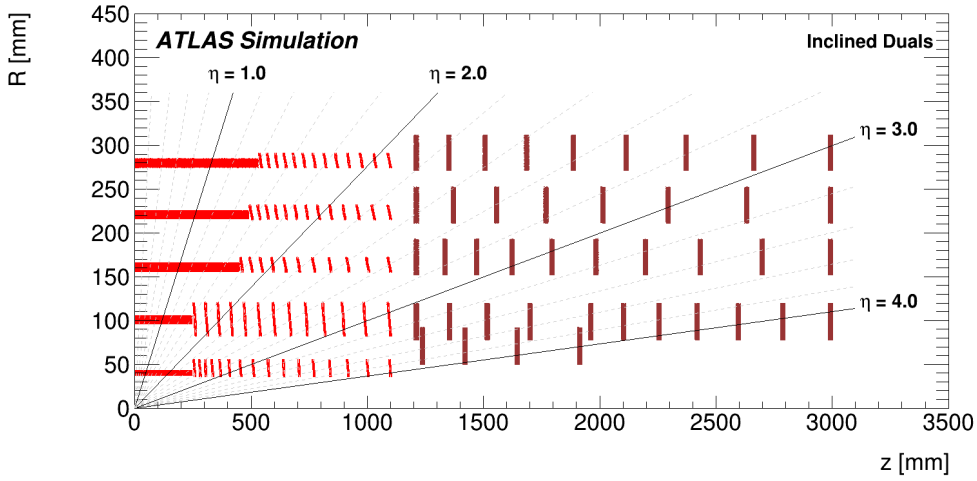


Figure 1: Candidate Layout for the ITk pixel detector with five layers. The layout provides a hermetic coverage for tracks with a pseudo rapidity of up to $|\eta| < 4$. Each layer is divided into three sections, a flat section, an inclined section and the endcap rings [2].

3. ITk Pixel Modules

The hybrid pixel modules consist of one to four readout chips bump-bonded and DC-coupled to a silicon sensor, where each front-end chip has a size of roughly 2×2 cm^2. The innermost layer, Layer 0, will consist of single chip modules with 150 μm thick 3D sensors. Layer 1 will consist of quad chip modules with 100 μm thick planar sensors, and the outermost layers will consist of quad chip modules with 150 μm thick planar sensors.

The front-end chip is being developed in the TSMC 65nm technology by a joint collaboration (RD53 Collaboration) between the ATLAS and CMS experiments. The ATLAS chip will consist of a pixel matrix of 400×384 pixels and a chip bottom, which will cover about 10% of the total chip area. At an average hit rate of about 250 hits per event in L0 and about 35 hits per event in L1, these two layers will be read out with a trigger frequency of 1 MHz. The outermost layers, where the average hit rates are lower, will be read out with a trigger frequency of up to 4 MHz to allow for the operation of an efficient track trigger. The expected data rates are as high as 5.12 Gbits/s per front-end chip, being transmitted over up to 4 AURORA lanes running at 1.28 Gbits/s per chip. In the serial powering scheme, the front-end chips will be powered by means of a constant current, from which the on-chip Shunt-LDO regulators [5] generate the required core voltages - any surplus

current, which is not consumed by the chip, is shunted by these regulators, in order to allow for a varying current consumption of the modules in the same serial powering chain. Three different analogue front-ends are currently being studied in a prototype chip, the RD53A chip [6], which has also been used to characterise and test different sensor prototypes.
The sensor prototypes show a hit efficiency of more than 97% after irradiation to $10^{16} n_{eq}/cm^2$ at bias voltages of about 400 V/600 V for the 100 μm/150 μm thick planar sensors, and below 200 V for the 3D sensors; significant drops in the in-pixel efficiencies are observed however, when the punch-through dots, which are required for sensor testing, are connected to the local module ground after bump-bonding the sensor to the front-end chip. It is therefore considered to leave the bias grid floating for the assembled modules, which almost fully recovers the effiency.
The bare modules will then be glued to a flex printed circuit board (PCB), which will be wire-bonded to the front-end chip. The flex PCB houses all passive components that are required to operate the front-end chips, like filter capacitors and resistors, and provides the high voltage connection to the backside of the sensor. A pigtail with a connector will then be used to connect each module to the electrical services of the detector. Several methods and glues for the attachment of the flex PCB to the silicon sensor are currently being evaluated for radiation hardness and thermal behaviour.

4. Local Supports and Services

The local suppors of the ITk pixel detector will be made of low mass carbon structures with thin titanium pipes for CO_2 cooling. In the inner system, the flat section will consist of staves, whereas there are several different designs for the rings in endcaps of the innermost two layers: coupled rings covering two layers with single chip modules in the inner ring and quad chip modules on the outer ring will be used for the intermediate η region, while stand-alone rings for L0 and L1 will be used in the high η region. In the outer layers, the endcaps and the inclined section will consist of half-rings. The low η region of the outer layers will consist of so-called longerons, carbon truss structures supporting two rows of modules which are slightly tilted with respect to each other. The cooling pipes will be embedded in the carbon structures in all sections of all layers.
The services scheme for the ITk pixel detector is shown in Figure 2. Due to the large number of modules and the high current consumption of the front-end chips a parallel powering scheme for the modules is not reasonable - the required services would not fit into the available volume. A serial powering scheme will therefore be deployed in the ITk pixel detector: while the up to four front-end chips per module are powered in parallel, up to 13 such modules will be connected in series. In order to also reduce the number of high voltage lines, the sensor bias voltage will be distributed in parallel to several modules in the serial powering chain in the outermost layers, where two high voltage lines will be used per serial powering chain, independent from the length of the chain. Therefore, a slightly different effective bias voltage will be applied to each sensor due to the voltage drop on the readout chips on a module. In the innermost layer, where 3D sensors are used, this scheme is deemed too risky due to the low depletion and breakdown voltages of these sensors, and a larger number of high voltage lines will be used, each connecting only sensors which are referenced to the same local ground potential.

In order to mitigate the risk to loose a full serial powering chain in the case of an open module failure, a Pixel Serial Powering Protection (PSPP) chip [7] is connected in parallel to every module. The PSPP chip contains a bypass transistor which, when activated, provides a low impedance path for the current in the serial powering chain. In addition an ADC on the PSPP chip can be connected through external resistors to an NTC temperature sensor on the module to monitor the sensor temperature. At the same time, the ADC can be used to measure the voltage drop across the module, and provides the functionality to automatically switch off a single module in the serial powering chain, if the sensor temperature or the voltage drop across the module gets too high.
A single command stream is sent to all front-end chips on one module at a speed of 160 Mbits/s. A clock for the digital part of the readout chip is derived from this stream. Up to four front-end chips are controlled by the same downlink.
The data from the front-end chip is transmitted through up to four AURORA lanes per chip, each of which can run at a maximum data rate of 1.28 Gbits/s. This data is transmitted electrically to a data aggregation element in the detector, on which several of the 1.28 Gbits/s lanes are serialised into a single stream with a higher data rate, which is transmitted to opto-electrical transceivers, where the signals are transformed into optical signals and transmitted to the off-detector readout system through optical fibre bundles. The pathlength for the electrical data transmission is not fixed yet; several cable types (flex PCBs, twin-ax cables and twisted pairs cables) are considered for an electrical transmission over a combined length of up to 8 m.

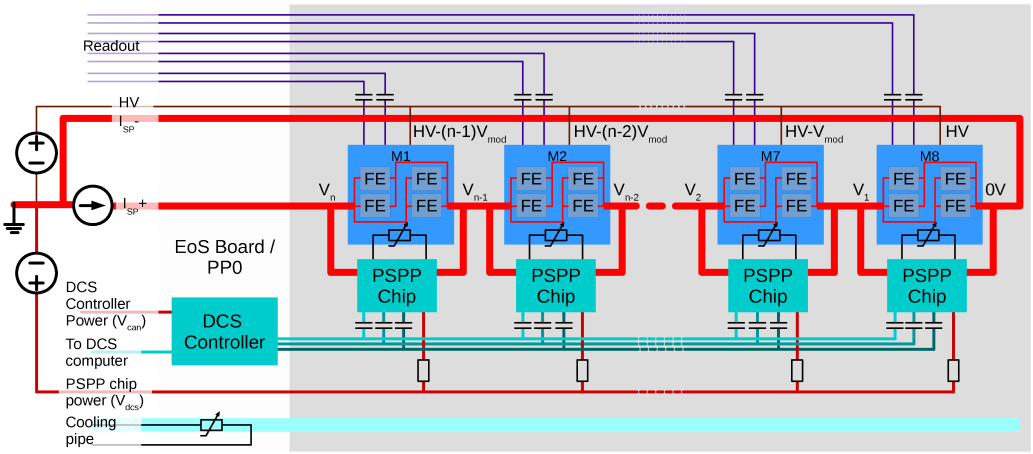


Figure 2: The services scheme for the ITk pixel detector. The modules are grouped into serial powering chains, where a PSPP chip is connected in parallel to each module in order to recover the serial powering chain in case of a module open failure. On each module, four FE chips are powered in parallel, while the sensor bias voltage is distributed to several modules per chain in parallel. All powering lines have a common reference at the Patch Panel 0. Since each module has its own local module ground, all communication lines need to be AC coupled at the module level [2].

The expected data rates per front-end chip are shown in Figure 3. The data rates shown for L0 and L1 correspond to a trigger rate of 1 MHz - while a new data compression scheme is currently being evaluated, which should reduce the data rate significantly, a higher trigger rate for these layers is not feasible, in particular for L0. At higher radii, in L2 to L4, due to the significantly

lower hit rate per chip, the trigger rate can be increased to 4 MHz at manageable data rates. This allows for the inclusion of the hit information from three pixel layers in the Level-0-Track-Trigger which is expected to have a significant impact on the Level-1-Trigger rates.
In addition to the hit data, about 2% of the available output bandwidth are reserved for diagnostics data from the front-end chips as one out of three different monitoring data paths of the Detector Control System (DCS). As an example, detailed, information on the front-end chip temperature distribution, which is not critical for the safety of the detector, will be transmitted through the standard DAQ data path and extracted from the data stream at the off-detector readout elements. A second monitoring path is provided through the PSPP chips, which will measure a reference temperature on each module and the voltage drop on each module, and transmit the data directly to the DCS through a low speed CAN bus. The third path of the DCS exists to ensure the safety of the detector in the case of any problems for instance with the cooling system - one temperature sensor on the the last module - with respect to the direction of flow of the CO_2 - in each serial powering chain is directly connected to an interlock system, without any digitisation between the sensor and the interlock crate, which will switch off both the low voltage and high voltage power supplies connected to the chain in case of any problems.

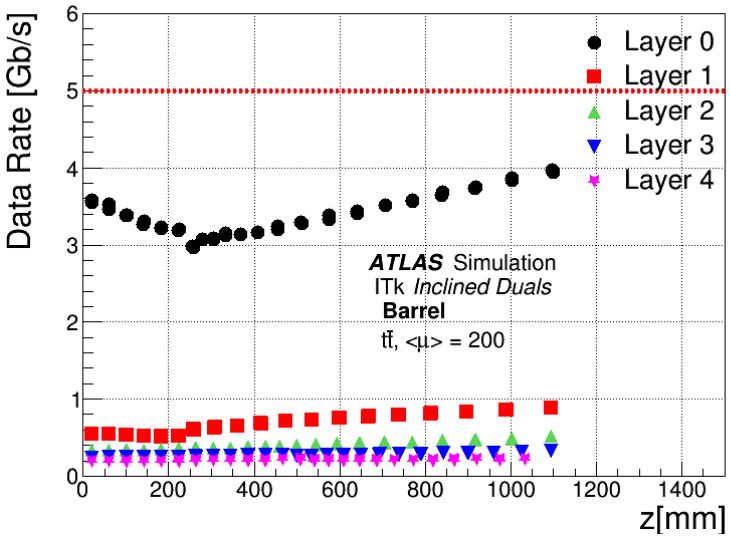


Figure 3: The expected data rates per readout chip in the five layers of the ITk pixel detector as a function of the position along the beam-axis. The transition from the flat section to the inclined section is clearly visible in the data rates for the innermost layer [2].

5. Prototyping Activities

While the final version of the readout chip for the ITk pixel detector is not yet available, an extensive prototyping campaign has been started to demonstratate several aspects of the new detector layout.
Prototypes of functional local supports have been produced to validate their mechanical properties and thermal performance, as well as to prepare the required equipment to transport loaded local

supports from the loading sites to the integration sides.
In addition to the mechanical prototyping, an extensive program has been started to demonstrate the operation of a serial powering chain on a representative local support, with representative services and power supplies. For the flat section in the outer barrel, a small electrical prototype consisting of a single serial powering chain with 7 FE-I4B [8] quad chip modules has been tested. A picture of the prototype is shown in Figure 4. Although a few of the front-end chips on this prototype do not work properly, and two of the integrated modules have damaged sensors, the serial powering chain is in principle fully functional, as data taken with a ^{90}Sr source shows. The result of such a test run is shown in Figure 5. The bias voltage from the two sensors in the center had to be disconnected due to broken sensors on these modules. The empty rectangles indicate that a front-end chip is not working properly, while several working front-end chips have a high number of disconnected pixels - in particular on the rightmost quad chip module.
While certain features, which depend largely on the front-end chip are not representative for the ITk pixel detector, several results that are relevant for the overall system have been obtained with this prototype, thanks to the usage of representative services and power supplies. Most of the observed effects are due to the close electrical coupling of the components of this complex system as shown in Figure 2. As an example, there are different requirements on the off-modes of the different power supplies in the serial powering chain: a high-ohmic off-mode for the high voltage power supply for instance can lead to a significant forward bias on a few sensors in the serial powering chain when no bias voltage is applied to the sensors, which has a potentially damaging effect on the front-end chips.

Figure 4: An electrical prototype for the flat section of the outer layers of the ITk pixel detector. Each electrical module is connected to the Type-0 services through a bent pigtail that is attached to the module flex. The Type-0 services run inside the truss support structure and are routed from the support structure to a patch panel prototype (note in the picture).

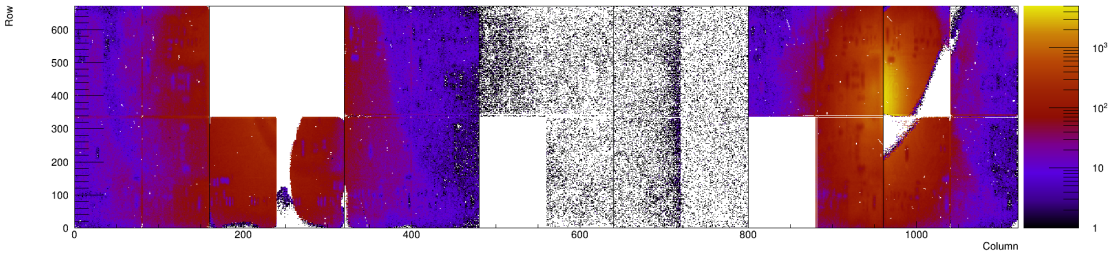
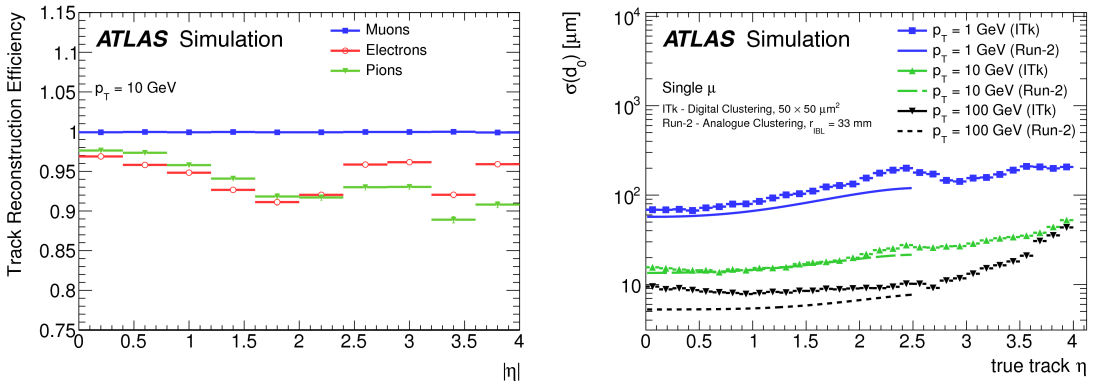


Figure 5: Result of a test run with two ^{90}Sr sources placed on top of the electrical prototype. Non-working readout chips and chips with disconnected bumps can be clearly seen. The sensors in the center of the prototype are not fully depleted, as no bias voltage is applied to the backside of the sensor.

6. Expected Physics Performance of the ITk pixel detector

The performance of the ITk pixel detector has been estimated using simulated events in which a pair of top quarks is produced. Pile-up events are added to the signal events, assuming an average of 200 proton-proton interactions per bunch-crossing. The results for two key figures for tracks using ITk hit information are shown in Figure 6. As shown in Figure 6(a), the reconstruction efficiency for muons with a transverse momentum of 10 GeV is close to 100%; the reconstruction efficiency for electrons and pions is significantly lower, but still higher than 90% over almost the full pseudo-rapidity range up to $|\eta| = 4$, which fully meets the requirements. The transverse impact parameter resolution is shown in Figure 6(b) and compared to the performance of the current ATLAS tracking detector during Run-2. Although digital clustering, i.e. no charge information, was used to estimate the performance of the ITk pixel detector, and analogue clustering, i.e. cluster positions are calculated using charge information, is used in the current pixel detector, the estimated impact parameter resultion of the ITk pixel detector is close to the performance of the current tracker, despite the significantly more challenging environment at the HL-LHC - with analogue clustering, where per-pixel charge information is used to determine the center of gravity per cluster, the performance of the upgraded pixel detector is expected to surpass that of the current detector.

As one of the benchmark scenarios, the production of two Higgs bosons, where one Higgs boson decays into two photons and one Higgs boson decays into two b quarks is considered. This final state provides a sufficiently clean signal due to the two photons, while it also is associated with a reasonably high branching ratio due to the decay of the second Higgs boson into two b quarks. A measurement of the production cross-section of two Higgs bosons provides a direct handle on the Higgs self-coupling and is therefore an important ingredient for probing the SM Higgs sector. The ITk pixel detector will play a key role in identifying the two b quarks from the decay of the second Higgs boson. Projecting a total dataset of 3000 fb^{-1}, the expected limits on the Higgs self-coupling just from the above-described final state, are shown in Figure 7.



(a) Reconstruction Efficiency (b) Impact Parameter Resolution

Figure 6: Projections for some of the key performance parameters of the ITk. The reconstruction efficiency for muons, electrons and pions is shown in the left figure (a), while the impact parameter resolution using digital clustering is compared to the performance of the current ATLAS detector in the LHC Run-2 using analogue clustering in the right figure (b) [2].

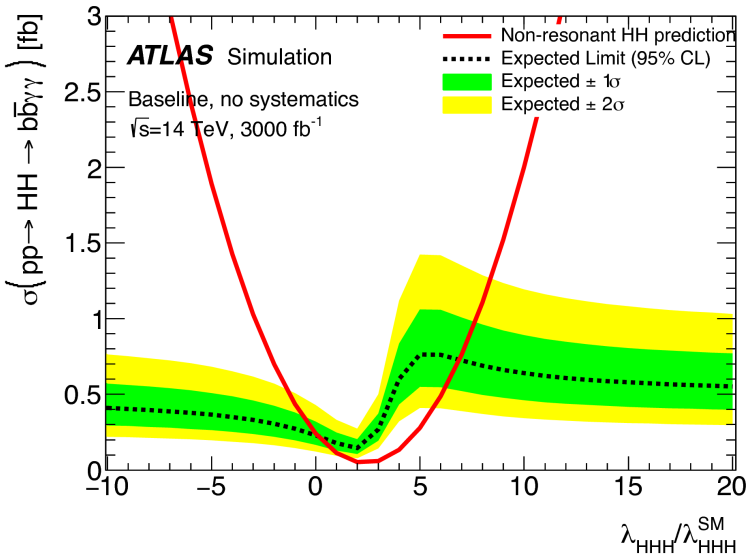


Figure 7: Expected limits on the Higgs self-coupling using the channel $pp \to HH \to b\bar{b}\gamma\gamma$ in ATLAS at the HL-LHC. Compared to limits that are expected at the end of the LHC Run-3, even this single channel provides a significant improvement due the clean final state and the large branching ratio [2].

References

[1] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, 2008 JINST 3 S08003

[2] ATLAS Collaboration, *Technical Design report for the ATLAS Inner Tracker Pixel Detector*, CERN-LHCC-2017-021, ATL-TDR-030, *https://cds.cern.ch/record/2285585*

[3] ATLAS Collaboration, *Technical Design report for the ATLAS Inner Tracker Strip Detector*, CERN-LHCC-2017-005, ATL-TDR-025, *https://cds.cern.ch/record/2257755*

[4] D. B. Ta et al., *Serial powering: Proof of principle demonstration of a scheme for the operation of a large pixel detector at the LHC*, NIM:A, Volume 557 (2006), pp. 445-459

[5] M. Karagounis et al.,*An integrated Shunt-LDO regulator for serial powered systems*, Proceedings of ESSCIRC (2009), pp. 276-279

[6] The RD53 Collaboration, *The RD53A Integrated Circuit*, CERN-RD53-PUB-17-001, *https://cds.cern.ch/record/2287593*

[7] N. Lehmann et al., *Prototype chip for a control system in a serial powered pixel detector at the ATLAS Phase II upgrade*, Proceedings of TWEPP-17, *PoS (TWEPP-17) 026* (2017)

[8] M. Garcia-Sciveres et al., *The FE-I4 pixel readout integrated circuit*, NIM:A, Volume 636 (2011), 1. Supplement, pp. 155-159