

Electronics System of the CMS GE1/1 Muon Upgrade and Lessons Learned From the Slice Test During the 2017-2018 LHC Runs

Elizabeth Rose Starling*, on behalf of the CMS Muon Group

Université libre de Bruxelles

E-mail: elizabeth.rose.starling@cern.ch

In this contribution, we will present the status of the readout electronics system for the triple-GEM detectors of the GE1/1 system, an upgrade which is being installed into the CMS experiment during the present LHC long shutdown (LS2) in 2019-2020. We will also report on the lessons learned from the ten slice test detectors which have been installed in CMS since 2017 and represent the first time that such large triple-GEM detectors have been operated within the LHC environment, and on the first results from the slice test detectors equipped with v3 electronics that were added to the slice test in March 2018. We will also report on the performance of the GE1/1 production chambers recorded on a large cosmic ray test bench sitting outside the CMS environment.

Ten slice test detectors were installed into the CMS muon endcap in January 2017. Data was recorded throughout the 2017-2018 runs, using both cosmic ray muons and LHC collisions. Lessons learned from this slice test allowed the development of the final GE1/1 electronics (hereafter referred to as "v3") for the production GE1/1 chambers which are now being installed during LS2. These new detectors are read out on the front-end by 24 VFAT3 chips, which run at 320 MHz, four times higher than the frequency of the VFAT2 chip, as well as the v3 optohybrid (OH) board, which is equipped with a Xilinx Virtex6 FPGA and three CERN GBT chipsets. The VFAT3 chips communicate with the OH through a 1 meter-long set of PCBs, called the GEM electronics board (GEB), which has been re-designed to accommodate the faster VFAT3 digital signals. The on-detector electronics are powered via nine FEAST DC-DC converters. Optical communication to the back-end, which includes a microTCA crate containing CTP7 and AMC13 boards, is based on the CERN Versatile link, including GBT and SCA chips as well as VTRx and VTTx optical modules. Production, qualification, and installation of the final v3 GE1/1 detectors is currently ongoing.

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^{*}Speaker.

1. Introduction

The GE1/1 project takes place in the context of the CMS endcap muon system. Details on the project, including its goals and purpose, can be found within Reference [1]. The GE1/1 system will consist of 144 triple-GEM (gas electron multiplier) detectors. These are gaseous detectors used across many experiments to detect ionizing particles such as muons. More details on the GE1/1 detectors can be found in Reference [2]. These detectors will be arranged as 36 two-detector "superchambers" in each endcap, organized in an alternating pattern of long (1.55 < $|\eta|$ <2.18) and short (1.61 < $|\eta|$ <2.18) superchambers, as seen in Figure 1. This upgrade will enhance redundancy and muon coverage in a high η region of CMS.

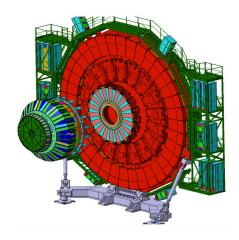


Figure 1: GE1/1 system in CMS

2. Electronics Improvements and Final Design

During the 2017-2018 LHC runs, a demonstrator system consisting of ten triple-GEM detectors operated within CMS. These detectors were arranged within the negative endcap as five two-detector "superchambers" with the naming convention GEMINIm(position)L(layer), where L=1 is the chamber closer to the interaction point and L=2 is the layer further away from the interaction point. At the time of installation the final v3 electronics had not been available. As such, these ten original slice test detectors consisted of v2 electronics. The differences between v2 and v3 electronics are explained in detail in Reference [3]. In 2018, the GEMINIm01 detectors were replaced with detectors equipped with v3 electronics. This "slice test" provided invaluable information about the operational capabilities of the GE1/1 detectors within the CMS environment, and allowed for several design flaws to be uncovered prior to the production of the final GE1/1 detectors.

2.1 Changes to the Optohybrid

The v3 optohybrid features three GBTX chipsets, which are responsible for the transmission of tracking and slow control, driving communication through bidirectional optical links to/from the back-end electronics. They feature a watchdog which prevents broken link and communication issues after events such as a clock change. The watchdog is reset at power-on, controls the initialization procedure and continuously monitors the GBTX. The GBTXs are minimally fused such that they lock to the fiber link, and in the case of a major failure, the watchdog reinitializes the link.

However, the watchdog was found to be non-functional on several previous optohybrids as far back as the first version of the GBTX chip, where not all the fused GBTXs would lock to the fiber link. Because of this, the watchdog was not enabled on the GBTX chips used in the v2 slice test detectors, which made a manual power cycle necessary after every LHC clock change. The cause of this watchdog failure was found to be twofold. For one, the power-on reset was removed too soon, prior to the GBTX power reaching a stable value. For another, the GBTX decoupling capacitance

was too small. Both issues were solved by adding capacitors, increasing the time constant of the RC circuit and increasing the decoupling capacitance from 10 μ F to 47 μ F.

2.2 Changes to the GEM Electronics Board (GEB)

In the v3 slice test detectors, the S-curve scan, normally used to monitor the noise of the detector at each of the 24 VFAT chips, consistently failed at the VFAT5 position. This was determined to be due to a mismatch in track lengths on the GEB, which prevented good communication with the optohybrid. This flaw was fixed in the final GEB design by modifying the track lengths.

2.3 Changes to the VFAT3 Chip and On-Detector HV Filter

Arguably the most complex flaw uncovered during the operation of the slice test was that of channel loss in the v2 detectors. Beginning in April 2018, GEMINIm29L1 began experiencing rapid and severe channel losses, defined as when a channel exhibits a noise value of between 0.0414 and 0.109 fC, which indicates that the capacitance of the strip is no longer being seen. After detailed study, this channel loss was determined to be the result of burn damage caused by discharges within the detectors that propagated to the anode, in which solder flows from the bonding pads to the input channels and where the silicon gets ablated away. Although an internal protection circuit was present on the VFAT2 chips, the damage-causing discharges reached energies of approximately $410~\mu$ J, far greater than the protection circuit could handle. Thus, in order to preserve the lifetime of the GE1/1 system, additional protection measures had to be added which could safely dissipate any propagating discharges. Both on-detector and on-chip protection measures were considered.

For the on-chip protection measures, two proposals were put forward. One, labeled $HV3b_{\nu3}$, utilized resistors in series in front of the VFAT inputs, which would dissipate a portion of the discharge energy. These resistors had a known radiation tolerance that would be suitable for their possible usage in CMS, but added 20% additional noise and 15% additional crosstalk to the system. The other proposal, labeled $HV3b_{\nu4}$, utilized diodes in parallel. These diodes would add no additional noise, but were commercial components with no known radiation tolerance that had not previously been used in an environment like the GE1/1 detectors would be in.

Prototypes of each version were produced and tested extensively. Both chips, when connected to an injection circuit, were able to withstand at least 500 electrostatic discharges of 470 μ J. Similarly, when installed on a 10x10 cm² GEM detector, both chips reduced the probability of damage, operating efficiently at the detector's nominal operating voltage and above. However, when installed on a full GE1/1 detector, a single discharge event resulted in the total destruction of all of HV3b_{ν 4}'s channels on multiple occasions, so this proposal was ruled out [4]. Thus, focus shifted to HV3b_{ν 3}. Two resistance values, 330 Ω and 470 Ω , were tested in conjunction with different resistance values for the on-detector HV filter. The test results can be seen in Figure 2.

Although the 330 Ω resistance proved to be insufficient, 470 Ω was determined to be capable of dissipating discharges of up to 1.5 mJ. Many resistor models of this value were tested for resilience, with the chosen resistor array being Panasonic's EXB2HV471JV. When combined with a minimum of 100 k Ω additional resistance in the on-detector HV filter, this circuit reduces the probability of damage in the event of a discharge from 93% to 3%. To ensure a good discharge damage protection

while maintaining optimal performance, the final design included added resistance of $200 \text{ k}\Omega$.

3. Results

In mid-2019, the production and qualification of GE1/1 detectors began. The qualification process is broken down into eight steps, the final of which, dubbed

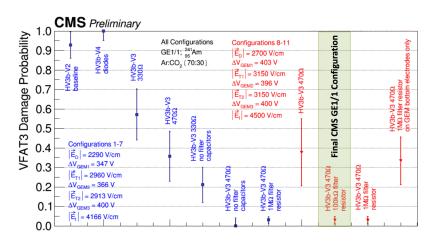


Figure 2: VFAT3 damage probabilities for different circuit configurations

"QC8", utilizes a cosmic ray test bench which can hold 30 GE1/1 detectors at a time. In this step, S-Curves are taken to ensure the electronics are properly working and to assess the noise and hit efficiency. The S-Curves of one VFAT for a chamber (which

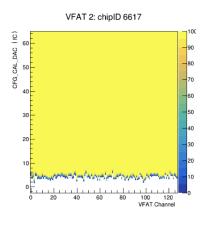


Figure 3: Example of S-Curve scan from the GE1/1 detector GE1/1-X-S-PAK-0001

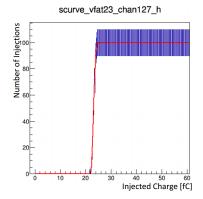


Figure 4: A single channel's S-Curve

was installed into CMS on July 25th, 2019) can be seen in Figure 3. This figure is composed of 128 individual channel S-Curve scans such as the one seen in Figure 4. Although a full set of S-Curves is comprised of 24 scans, one for each VFAT on the detector, this scan is representative. From the full scanset, box plots of the threshold and ENC can be derived, as seen in Figure 5.

The ENC plot seen in the right of Figure 5 exhibits a cyclical trend for the noise, with VFATs closer to the wide end of the detector showing higher noise than the VFATs closer to the narrow end. This is expected, as the VFAT has an intrinsic noise when coupled to the detector, which increases proportionally to the capacitance of the strips that are coupled to each VFAT channel. As the detector width widens, the strips widen as well, increasing the capacitance. However, VFATs 3, 4, 11, 19, and 20 show a higher noise than suggested by the pattern. This is due to the proximity of these VFATs to the optohybrid. This additional contribution is both expected and significantly lower than the contribution that was seen in the v2 slice test detectors.

In QC8, a detector can only be qualified for installation if the efficiency is above 95%. This measurement is made by declaring all chambers other than the chamber under test as reference chambers. A given muon track is reconstructed using the hits in the reference chambers.

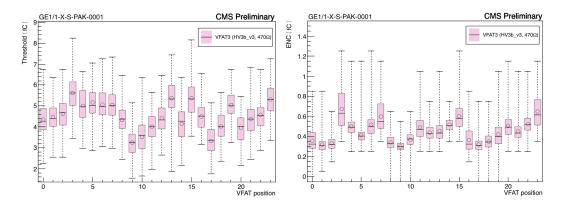
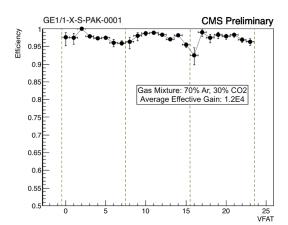


Figure 5: Threshold (left) and ENC (right) values from the S-Curve scans from GE1/1-X-S-PAK-0001. 50% of the values are within the boxes, with the full range within the bars. The circle and line in the box represent the mean and median values, respectively.



The track is then extrapolated to the test chamber, and a hit which is associated to that extrapolated track is searched for. This allows us to determine the chamber efficiency, an example of which can be seen in Figure 6. Here, all sectors except for VFAT16 have an efficiency above the required 95%. However, this does not disqualify the chamber, as this lower value is due to the geometrical acceptance of the QC8 stand and is not a function of the detector itself.

Figure 6: QC8 Efficiency of GE1/1-X-S-PAK-0001

4. Conclusion

Many changes were made to the GEM

front-end electronics to allow for the required performance of GE1/1. The slice test proved invaluable in this regard, allowing us to identify problems such as channel loss and track length mismatches before the full production began.

References

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