

Vertex and Tracking Detectors for the Circular Electron Positron Collider (CEPC)

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The Circular Electron Positron Collider (CEPC) has been proposed as a Higgs factory to measure the properties of the Higgs boson with high precision and to enable the possibility to explore new physics. To meet the stringent physics requirements, it is necessary to design and construct both vertex and tracking detectors with the state-of-the-art silicon detector technologies. Initial R&D has been focused on CMOS pixel sensors to achieve both high position resolution and low power consumption. They are desirable for the vertex detector, which will sit closest to the interaction point and play a decisive role in precise determination of the primary and secondary vertices that are crucial for heavy flavor tagging. Recently, efforts have been also made to explore the possibility to design the large area silicon tracker with pixel sensors developed with high voltage CMOS technology, which promises both high position resolution and timing resolution. A short stave populated with the latest development of ATLASPix has been proposed for the demonstrator and sensor design tailored toward the CEPC tracker requirements are being pursued.

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1. Introduction

The Circular Electron Positron Collider (CEPC) [1,2] has been proposed to measure the Higgs boson properties with precision beyond the Large Hadron Collider (LHC) [3] and its successor, the High Luminosity LHC (HL-LHC) [4,5]. Precision measurements of the Higgs boson, as well as the W and Z bosons, will provide critical tests of the underlying fundamental physics principles of the Standard Model (SM) and are vital in the exploration of new physics beyond the SM (BSM). The CEPC, located in a circular underground tunnel of approximately 100 km in circumference, is designed to operate primarily at the center-of-mass energy of $\sqrt{s} = 240$ GeV as a Higgs factory, but also at around $\sqrt{s} = 91.2$ GeV at the Z -pole and $\sqrt{s} = 160$ GeV at the WW production threshold. To meet the stringent physics requirements, it is highly demanding to design a charged-particle tracking system of high performance and with a sufficiently large solid angle coverage. In this article, the baseline design of the CEPC tracking system will be described and several selected detector R&D activities will be reported.

2. Tracking System

The CEPC baseline tracking system is illustrated in Figure 1. The basic concept has been adopted from the International Large Detector (ILD) design [6] and composes two major components, with the vertex detector located close to the interaction point, and the outer tracker formed by the Time Projection Chamber (TPC) and multiple silicon sub-detectors. Details of the vertex detector and the outer tracker are described below.

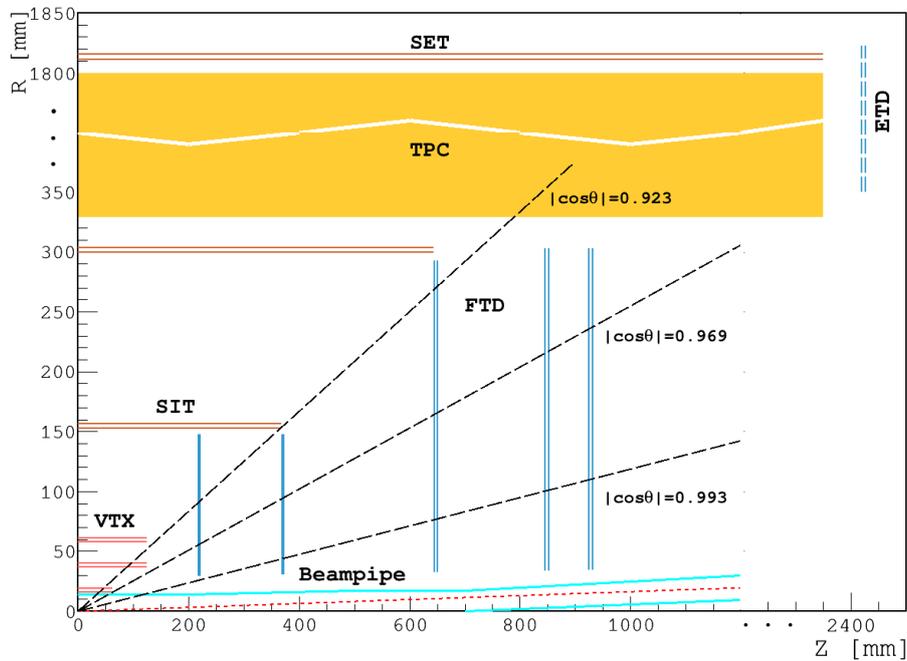


Figure 1: The layout of the CEPC baseline tracking system.

3. Vertex Detector Design and R&D

The CEPC vertex detector will play a critical role in heavy flavor tagging and τ -lepton tagging that are essential for the success of the precision physics program. It is desirable to achieve an excellent impact parameter resolution in the $r - \phi$ plane that can be parameterized as follows:

$$\sigma_{r\phi} = a \oplus \frac{b}{p \cdot \sin^{3/2} \theta} \quad (3.1)$$

where $\sigma_{r\phi}$ denotes the impact parameter resolution in the $r - \phi$ plane, p the charged particle momentum in the unit of GeV, and θ the polar angle of the charged particle. The first term a describes the intrinsic resolution of the vertex detector in the absence of multiple scattering, while the second term b represents the effects of multiple scattering. The required $a = 5$ and $b = 10$ for the CEPC vertex detector will deliver significantly improved performance over the legacy ones built for the Large Electron-Positron Collider (LEP) [7–10]. The baseline layout consists of six concentric cylindrical layers of high resolution pixel sensors, spacing between 16 mm and 60 mm in radii from the beam line. It must provide a high spatial resolution, close to the interaction point, better than $3 \mu\text{m}$, a low power consumption below $50 \text{ mW}/\text{cm}^2$ to allow forced air cooling, and a low material budget below $0.15\% X/X_0$ for each detector layer to minimize the multiple scattering effects. In addition, the vertex detector must survive a Total Ionizing Dose (TID) of 10 MRad and a Non-Ionizing Energy Loss (NIEL) of $2 \times 10^{13} \text{ 1 MeV } n_{eq}/\text{cm}^2$ over 10 years of operation. Along with the tracker concept design and tracker layout optimization, R&D efforts have also been conducted to develop silicon pixel sensors toward the required performance. In particular, several prototype pixel sensors have been developed with a $0.18 \mu\text{m}$ novel CMOS imaging sensor process, namely JadePix-1/2-3 and TaichuPix-1. Their design and characterization results are described below.

3.1 JadePix-1

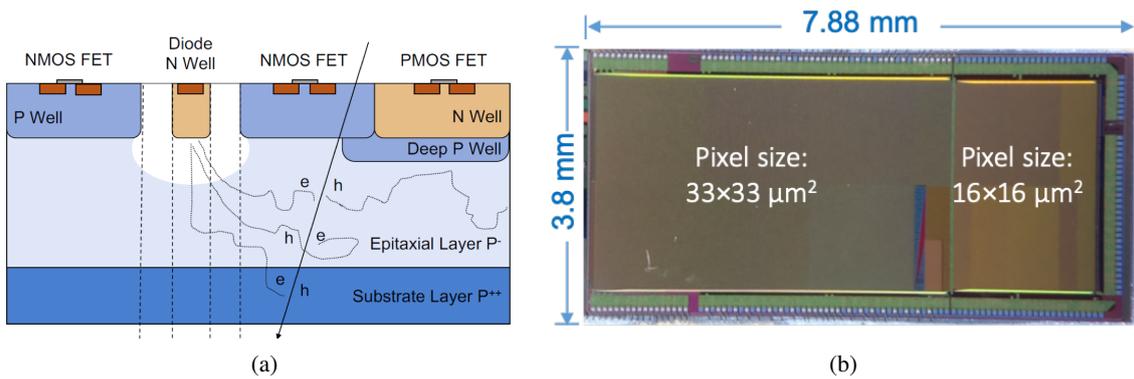


Figure 2: (a) Cross-sectional view of the JadePix-1 pixel structure with a small collection electrode implemented; (b) picture of a JadePix-1 prototype sensor.

JadePix-1 was the first prototype pixel sensor developed for the CEPC vertex detector [11]. It was designed to optimize sensor diode geometries to achieve high charge-over-capacitance (Q/C) ratio, which would be vital to reduce analogue power consumption [12]. Q and C represent the

effective signal charge collected by the electrode and the equivalent input diode capacitance, respectively. Prototype pixel sensors were fabricated on wafers with an $18\ \mu\text{m}$ thick epitaxial layer and a high resistivity of $\rho > 1\ \text{k}\Omega\cdot\text{cm}$. Figure 2a shows the cross-sectional view of the diode structure. Due to the lack of electric field in the active sensor volume, charge collection was primarily achieved through thermal diffusion. The prototype sensor was $7.88 \times 3.8\ \text{mm}^2$ in size, as shown in Figure 2b, and consisted of two matrices. The upper part of the left matrix contained 10 sectors of $33 \times 33\ \mu\text{m}^2$ pixels that were implemented with different electrode size and surrounding isolation area. The lower part contained 9 sectors of $33 \times 33\ \mu\text{m}^2$ pixels with test structures, and one sector of $16 \times 16\ \mu\text{m}^2$ pixels with biased voltage up to 10 V. In each sector, pixels were arranged in 48 columns and 16 rows. The right matrix contained 16 sectors of $16 \times 16\ \mu\text{m}^2$ pixels that were arranged in 96 columns and 16 rows in each sector.

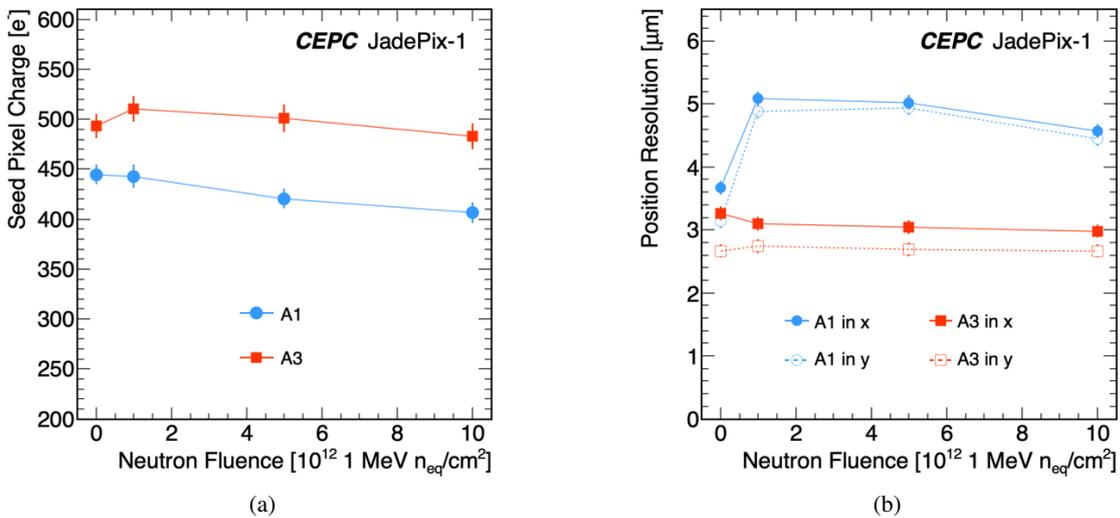


Figure 3: (a) Seed pixel charge for pixels with small electrode (in blue bullet) and large electrode (in orange square) before and after neutron irradiation; (b) position resolution for pixels with small electrode (A1 in x and y with blue open and closed bullets) and large electrode (A3 in x and y with orange open and closed squares) before and after neutron irradiation.

For the sectors with $33 \times 33\ \mu\text{m}^2$ pixels, their charge collection performance was characterized with radioactive sources [13]. Test results, including noise level, charge collection efficiency, charge-over-capacitance and signal-to-noise ratios, were measured. Equivalent noise charge and signal-to-noise ratio were measured to be below $10\ e^-$ and higher than 55, respectively. The highest Q/C ratio of 0.021 V was obtained for the pixel sector with a small electrode size of $4\ \mu\text{m}^2$ and a large isolation area of $30\ \mu\text{m}^2$. JadePix-1 prototype sensors were irradiated up to the fluence level of $10^{13}\ 1\ \text{MeV}\ n_{eq}/\text{cm}^2$ at a neutron irradiation facility in China. Prototype sensor performance was further characterized with the DESY electron test beam before and after neutron irradiation. Figure 3a shows the decreased amount of collected charge by the seed pixel as the radiation fluence increases. This could be explained with the charge trapping effect caused by the irradiation induced defects. Figure 3b shows the position resolution of the pixels with small electrode ($4\ \mu\text{m}^2$) degraded after neutron irradiation, but remained nearly unchanged for the pixels with large elec-

trode ($15 \mu\text{m}^2$). In general, pixels with larger electrode showed higher radiation tolerance thanks to the lower trapping probability due to the shorter charge collection distance.

3.2 JadePix-2/3

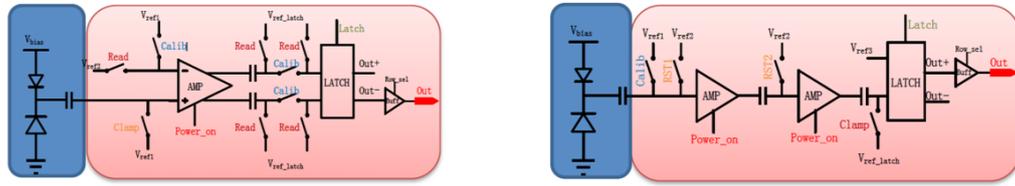


Figure 4: Schematics of the single stage differential amplifier and the two-stage single-ended amplifier used in JadePix-2.

JadePix-2 was aimed for compact pixel design (pitch size of $22 \mu\text{m}$) with high signal-to-noise ratio. The prototype sensor was $3 \times 3.3 \text{ mm}^2$ in size, and contained in total 96×112 pixels segmented into 8 matrices that were read out in the rolling shutter mode. It utilized a high voltage biased charge collection diode (V_{bias} up to 10 V) to minimize the input capacitance and a comparator with the Output Offset Storage (OOS) technique to mitigate the pixel-to-pixel threshold dispersion. As shown in Figure 4, signal amplification was achieved either with a differential amplifier or a two-stage single-ended amplifier. The equivalent noise charge (ENC) of the readout electronics was measured to be around $31 e^-$, with around $11 e^-$ from the Temporal Noise (TN) and around $29 e^-$ from the Fix Pattern Noise (FPN).

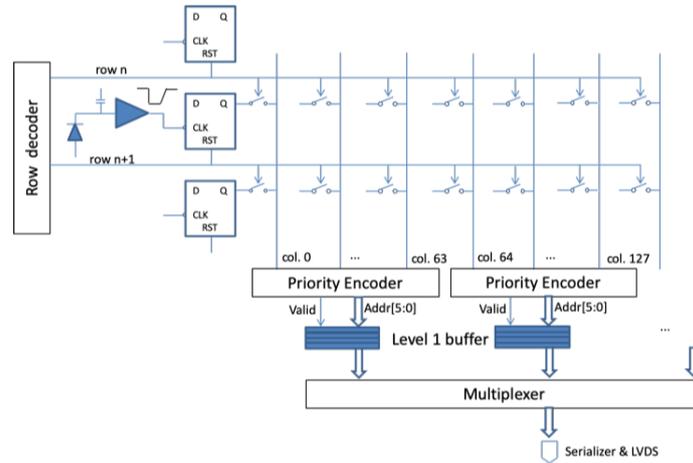


Figure 5: Readout architecture of JadePix-3.

An improved version, named JadePix-3, was designed to reduce the FPN noise and enhance the readout capability. As illustrated in Figure 5, D flip-flops, shared between column lines, were introduced to register hits, which were read out with the end of column priority encoder. 64 columns could be processed during each row readout circle. Zero suppression was implemented in the periphery to further optimize the data output. The design was submitted for fabrication in September 2019 and characterization will be performed after the chips are back from the foundry.

3.3 TaichuPix-1

TaichuPix-1 was initiated toward a full functionality pixel sensor that could cope with the high data event rate at the Z-pole. The prototype sensor was $5 \times 5 \text{ mm}^2$ in size, with $25 \times 25 \mu\text{m}^2$ pixels arranged in 192 rows and 64 columns as its floor plan depicted in Figure 6a. In the in-pixel circuit, it adopted the analog design from the ALICE ALPIDE sensor but with an increased biasing current to shorten the peaking time to about 25 ns. Two variants of in-pixel readout electronics were implemented, as shown in Figure 6b. One was based on a common “column-drain” readout architecture derived from the ATLAS FE-I3 readout chip, and the other derived from the ALICE ALPIDE. The former design utilized a priority based data driven readout. In addition, a time stamp could be registered at the End of Column (EOC). Based on a two-FIFO readout architecture, the L1 buffer was introduced at the column level to de-randomize the hit information, and the L2 buffer at the chip level to match properly the input and output data rates. TaichuPix-1 prototype chips were just back from the foundry and being tested in laboratory.

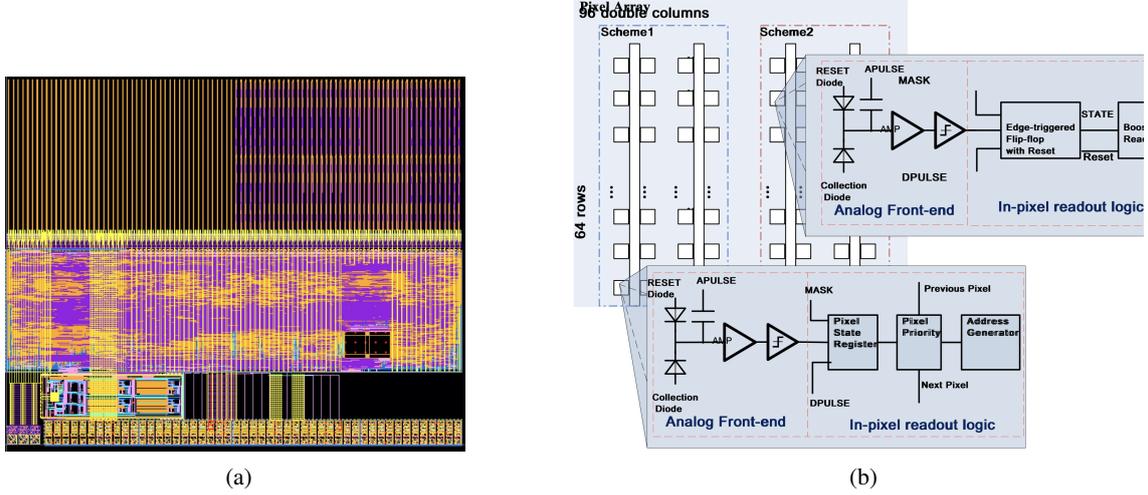


Figure 6: (a) Floor plan of TaichuPix-1; (b) schematic of the two in-pixel readout electronics implemented in TaichuPix-1.

4. Silicon Tracker Design and R&D

The baseline outer tracker features the large TPC as the main tracker that is wrapped up with the “Silicon Envelope” [14]. The TPC provides a high density of space points that will allow continuous tracking with low cost and additional energy loss (dE/dx) measurement to be used for the particle identification (PID). The silicon tracker, with low material budget controlled to be below $0.65\% X/X_0$ per detector layer, provides several additional high precision points along the charged particle trajectories and can improve the overall tracking efficiency and precision. The required track momentum resolution can be parameterized as follows:

$$\sigma_{1/p_T} = a \oplus \frac{b}{p \cdot \sin^{3/2} \theta} \quad [\text{GeV}^{-1}] \quad (4.1)$$

where $p(p_T)$ is the (transverse) momentum of the charged particle and θ the polar angle. The constant term a represents the intrinsic resolution of the tracker and the second term b parametrizes the multiple scattering effects. The CEPC tracker is expected to achieve $a \sim 2 \times 10^{-5} \text{ GeV}^{-1}$ and $b \sim 1 \times 10^{-3}$.

The silicon tracker is further composed of the Silicon Inner Tracker (SIT), the Silicon External Tracker (SET), the Forward Tracking Detector (FTD) and the Endcap Tracking Detector (ETD). In particular, the SIT and the SET provide precise measurement points on tracks before and after the TPC and improve the overall tracking performance in the central region. The FTD disks are installed in the forward region and essential for precise and efficient tracking down to a small polar angle. The ETD, not in the baseline layout, can be positioned in the gap between the endplate of the TPC and the endcap electromagnetic calorimeter. It shall improve the track extrapolation to the electromagnetic calorimeter. In addition to the precise space point measurements, the silicon tracker should also provide decent timing resolution of $O(10 \text{ ns})$ to separate bunch crossings, even for the most challenging operation at Z-pole with a short bunch spacing of 25 ns.

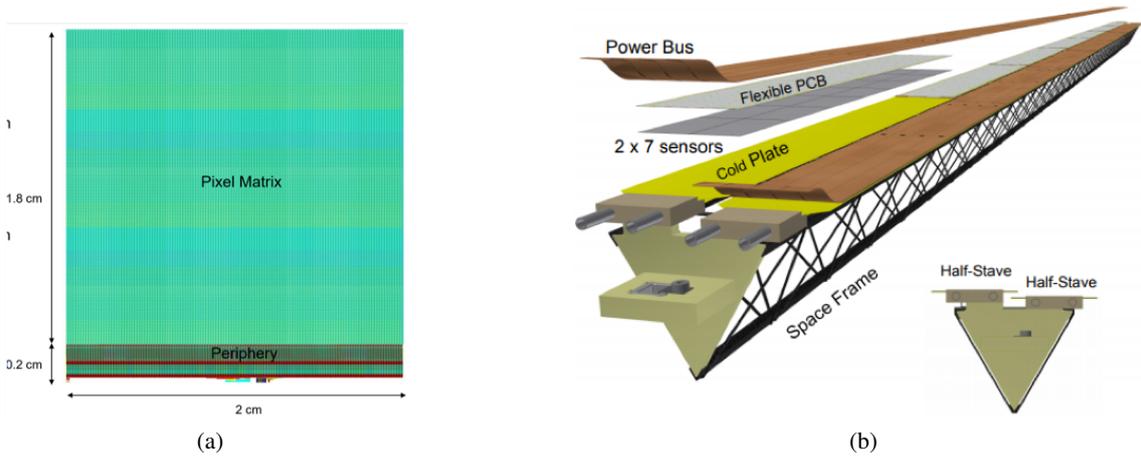


Figure 7: (a) Floor plan of ATLASPix-3; (b) sketch of the carbon fibre supporting structure with cooling pipes under the cold plate for the ALICE ITS outer tracker, taken from [17].

The total tracker area to be covered by silicon will exceed 50 m^2 . Although conventional but thinned silicon micro-strip sensors have been considered as the baseline design in the Conceptual Design Report, pixelated CMOS sensors are promising higher performance with reduced costs. They have already achieved certain level of maturity after years of R&D for the LHC experiments. Given the short R&D time allowed for the CEPC large-area silicon tracker, it would be appropriate to start with available components developed for other applications. In particular, to demonstrate the technology feasibility, it has been proposed to build a short stave with the ATLASPix-3 pixel sensors [15] developed for the ATLAS ITk-Pixel project, and the carbon fibre supporting structure with embedded cooling pipes designed for the ALICE ITS upgrade [17]. These two critical components are shown in Figure 7. With the predecessor of ATLASPix-1 [16], the measured position resolution of $\sigma_x = 11.3 \mu\text{m}$, the time resolution of 6.8 ns after the time walk and row delay corrections, and the power consumption below 300 mW/cm^2 are already close to the expected CEPC tracker requirements. ATLASPix-3 should provide improved performance and enriched functional-

ities. For future sensor developments, it should be feasible to deliver pixelated CMOS sensors with a smaller pitch size below $40\ \mu\text{m}$ and reduced power consumption that can fulfill all the CEPC requirements. Based on similar technologies, the LHCb collaboration is investigating the "Mighty Tracker" concept [18] for their main tracker toward the Upgrade II. It will be thus extremely important to explore the synergies between CEPC and LHCb.

5. Summary and Outlook

The Circular Electron Positron Collider (CEPC) has been proposed for Higgs and electroweak precision measurements, which would significantly deepen our understanding of the Standard Model and guide the search for new physics beyond the Standard Model. To meet the stringent physics requirements, the CEPC tracking system shall provide high efficiency and precision of charged particle tracking and vertex reconstruction. Along with the concept design and continuous layout optimization, R&D have started to develop silicon pixel sensors toward the stringent requirements. Prototype sensors, namely JadePix-1/2/3 and TaichuPix-1, have been developed for the vertex detectors and their performance has been characterized or is being characterized. For the outer silicon tracker, it has been proposed to build a demonstrator with available components and develop improved pixelated CMOS sensors to fulfill the tracker requirements.

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