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The SPi chip as an integrated power management device for serial powering of future HEP experiments

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Serial powering is one viable and very efficient way to distribute power to future high energy physics (HEP) experiments. One promising way to realize serial powering is to have a power management device on the module level that provides the necessary voltage levels and features monitoring functionality. The SPi (Serial Powering Interface) chip is such a power manager and is designed to meet the requirements imposed by current sLHC upgrade plans. It incorporates a programmable shunt regulator, two linear regulators, current mode ADCs to monitor the current distribution on the module, over-current detection, and also provides module power-down capabilities. Compared to serially powered setups that use discrete components, the SPi offers a higher level of functionality in much less real estate and is designed to be radiation tolerant. Bump bonding techniques are used for chip on board assembly providing the most reliable connection at lowest impedance. This paper gives an overview of the SPi and outlines the main building blocks of the chip. First stand alone tests are presented showing that the chip is ready for operation in serially powered setups.

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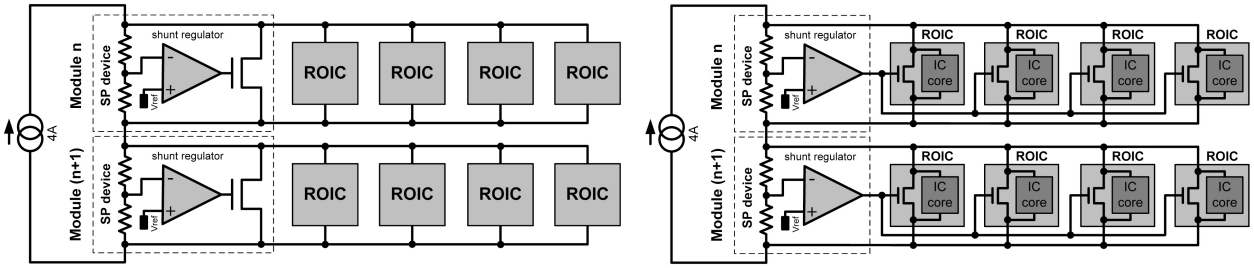

Figure 1: Illustration of the serial powering approach using two different schemes. One option (shown left) uses a shunt regulator and transistor on each module to generate the supply voltage for the readout chips. Another option (shown right) is to use a single shunt regulator per module but to distribute shunt transistors among all readout chip on the module.

1. Introduction to Serial Powering

The present LHC experiments use a conventional, parallel powering scheme where each individual detector subsystem is provided with power by a separate cable. This imposes a significant contribution to the mass of the detector. Also the resistive power loss in the cables (I^2R) is tremendous and results in a highly inefficient setup (for the current ATLAS strip detector the efficiency is as low as 50 %). The scheduled upgrade of the LHC experiments involves an increase of readout channels by up to a factor of ten. The additionally required cables when pursuing parallel powering are intolerable in terms of required mass and electrical efficiency. Serial powering is an alternative and more efficient powering scheme where a current is used to power modules in series and a appropriate supply voltage is generated locally at each module (see Figure 1).

Within the serial powering approach various different options are possible, which will be briefly outlined in the following. One option (Figure 1, left) requires a power management device on each module that generates the supply voltage locally. Such a power manager could also provide communication and module diagnostics, so that in case of a module failure a controlled shut-down of this particular module can be initiated while the remaining detector system still maintains operation. Many setups using discrete components explored this scheme ([1],[2]). The SPi (Serial Powering Interface) was designed to offer an integrated solution for power management that outperforms discrete setups in terms of functionality, performance and required area.

The second option is to use one shunt regulator per module but to distribute shunt transistors among all readout chips on the module (Figure 1, right). This approach, known as the distributed shunt concept developed by M. Newcomer, is also possible with the current SPi chip. However, this paper will not cover any details on the distributed shunt approach (see [3],[4]).

A third option where every readout chip is standalone and contains independent shunt circuitry is not shown in Figure 1. The current ABCn [5] (ATLAS strip) and FE-I4 [6] (ATLAS pixel) read out chip incorporate specific powering blocks to explore this approach.

Besides serial powering, DC-DC conversion [7] is considered as an alternative powering scheme for the LHC upgrade. All approaches have specific benefits and downsides and the optimal choice will strongly depend on the detector characteristic, meaning whether strips or pixels are powered and which specific experiment is equipped (CMS, ATLAS, etc.).

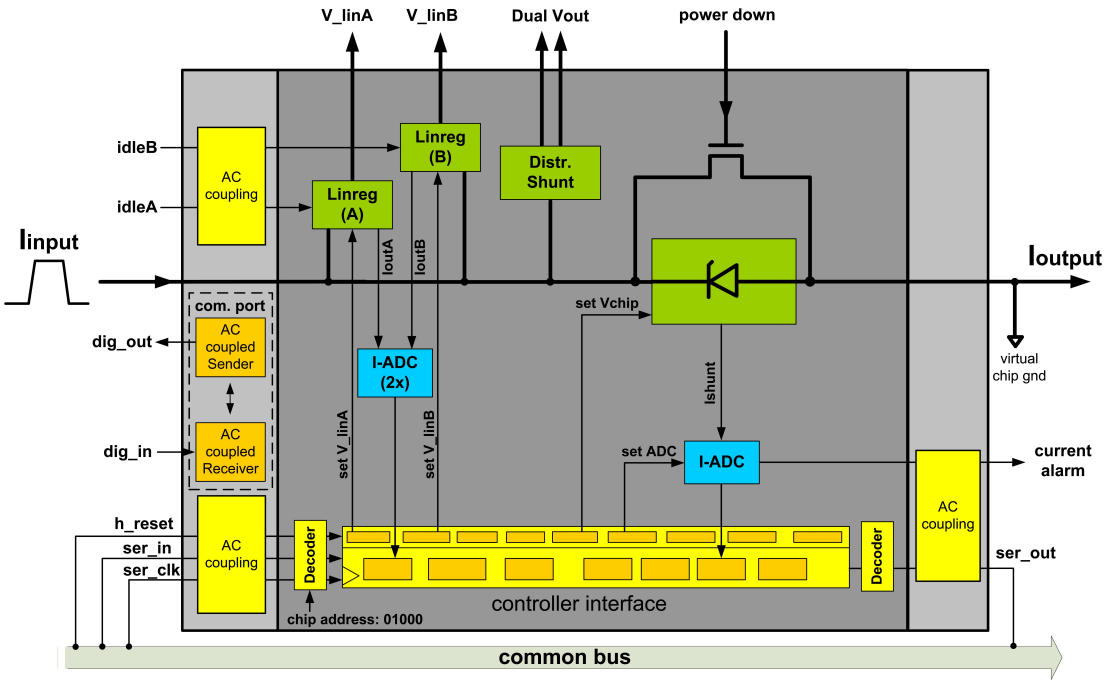

Figure 2: Schematic overview illustrating the main building blocks of the SPi chip.

2. Overview and features of the SPi chip

The main building blocks of the SPi are illustrated in Figure 2. The chip incorporates a shunt regulator (here shown symbolically as a shunt diode) that converts the supplied current into a programmable voltage that powers the chip as well as the remaining components on the module. Moreover, two programmable linear regulators create a subset of the shunt voltage. This enables the use of multiple voltages on a module, e.g. to supply digital and analog components at different levels. The voltage of the linear and shunt regulators is programmable in 100 mV steps and covers a wide range from 1.2 to 3 V.

A digital control interface provides communication with the chip. Upon wake-up the chip sets itself in a determined default configuration for all control registers, most importantly with 1.5 V as the shunt voltage, and can be reconfigured afterwards. Only two control lines (ser_in and ser_clk) are needed to program the chip. An optional ser_out line can be used to read back data from the chip. All SPi chips are foreseen to be connected to a common bus in a multi-drop configuration. The address of each chip is hardwired by connecting each of 5 address pads to the upper or lower supply rail. The 32 bit command word to communicate with the chip includes the 5 bit chip address. It also contains an instruction part (such as set, read back, or default), the register address, and an 8-bit data word. A chip wildcard (address: b10101) can be used to talk to all SPi chips attached to the bus at the same time, e.g. to set the shunt voltage on all modules at once.

6-bit current mode ADCs are attached to the shunt and linear regulators to measure the current passing through the devices. The ADCs are read back via the digital control interface. The LSB of each ADC is adjustable with 4 bits offering a dynamic range between 100 mA and 2 A. Each ADC has a programmable threshold and reports an over-current situation once this threshold is exceeded

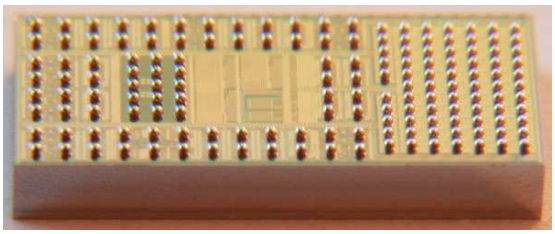

Figure 3: Photograph of the $5.7 \times 2.8\,\mathrm{mm}^2$ large SPi 001 chip with SnPb bumps before flip chip assembly.

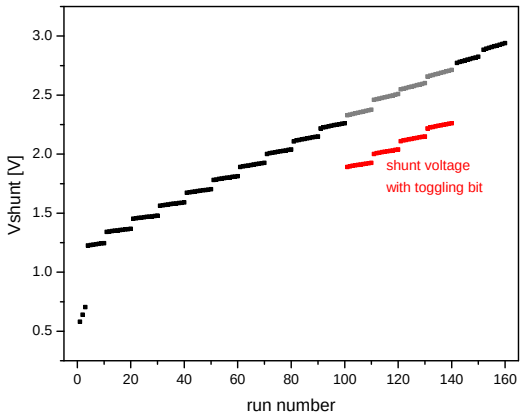

Figure 4: Output voltages of the SPi shunt regulator. Each line segment shows a current sweep between 50 mA and 500 mA.

for a selectable time period (between 150 μs and 2 ms). For the shunt ADC in particular, this logic level is provided outside the chip (current alarm flag) and can be used immediately to initiate proper power down procedures.

Powering down a module can be done using a separate power FET ($\mathrm{W} \sim 680\,\mathrm{mm},\ \mathrm{L} = 300\,\mathrm{nm}$) that is integrated in the chip. The power FET is completely self-contained and is able to bypass the full module current of 4 A and more (see section 4).

In addition, a standalone amplifier unit is placed within the SPi to explore the previously mentioned distributed shunt concept.

All communication with the chip is done using AC coupled LVDS drivers and receivers. AC coupling (with the use of external capacitors) is necessary as the DC potential of each individual module is different from the common ground at the DAQ system due to the staggered module architecture in the serial powering scheme. Additional bidirectional communication ports that contain AC LVDS driver and receiver pairs are implemented as well. They are integrated to act as level adapters between standard electronics on the module and the DAQ system. Details on the data protocol and the use of the SPi in a master and slave communication configuration can be found in [8].

3. First Results with SPi 001

A prototype of the SPi has been fabricated using TSMC 250nm technology. To provide the lowest possible connection impedance, bump bond technology is used for assembly. A photograph of the $5.7 \times 2.8\,\mathrm{mm}^2$ large SPi 001 chip is shown in Figure 3. The chip contains all elements that are outlined in section 2 and shown in Figure 2. First standalone tests have been conducted with the chip after successful assembly onto a PCB using flip chip on board technology. Details on the assembly method can be found in [9].

Figure 4 shows the different chip voltages obtained by using the programmable shunt regulator. The voltage range encompasses approximately 1.2 V to 3 V. Due to a variety of configuration

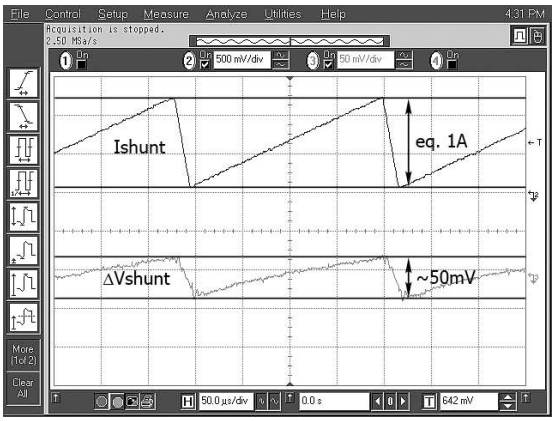

Figure 5: Large signal behavior of the shunt regulator. The shunt current is modulated from 50 mA to 1 A (time scale: 50 μs per div) using a voltage controlled current source (upper trace). Shunt voltage response is shown below indicating an impedance of about 50 mΩ for this frequency range.

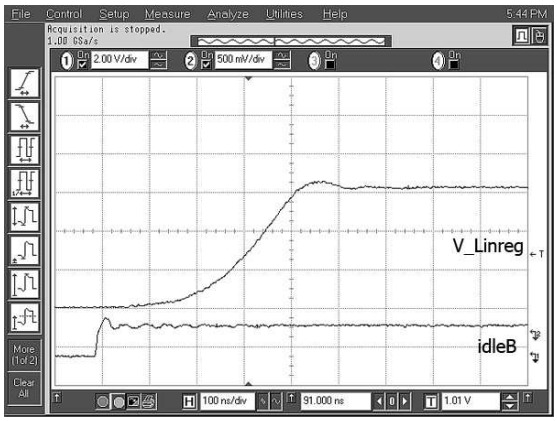

Figure 6: Output voltage of one linear regulator (upper trace) using the idle control feature (lower trace). The time scale is 100 ns per division.

options in the chip, voltages even below 1.2V and above 3V can be selected. However, for voltages below 1.2 V the functionality of the digital controller cannot be ensured, and it is likely that further communication with the chip is not possible once such a low voltage is set[1]. Since the nominal supply voltage of the process is 2.5 V, voltages in excess of 3 V are avoided in the tests.

Within each selected voltage in Figure 4 the shunt current is swept from 50 mA to 500 mA in order to illustrate the DC output characteristic of the shunt regulator. A linear fit to the segments reveals an output resistance of about 50 mΩ. The plot also indicates a minor design flaw in the digital controller. A timing hazard can cause an unwanted toggling of some bits when the data word is loaded into the chip. This timing issue is supply voltage dependent and only appears for supply voltages above 2.2 V. For lower supply voltages any data word can be successfully latched. That means that right after the chip is reset for example (Vchip at 1.5 V), any shunt voltage can be programmed and will be established (black data points). However, if a successive voltage sweep is performed, the bit toggling occurs for certain voltage levels (indicated by red segments).

Figure 5 illustrates the large signal behavior of the shunt. Shown is the AC voltage response of the shunt (lower trace) when the current is swept from 50 mA to 1 A (upper trace). The response yields a dynamic impedance of about 50 mΩ, in perfect agreement with the DC performance. This very low impedance is due to the fact that bump bond techniques have been used to mount the chip. Note that the maximum bandwidth of the voltage controlled current source that is used to modulate the current is about 10 kHz. However, detailed frequency measurements [10] confirm a shunt impedance on the order of 50 mΩ for the full dynamic range up to about 10 MHz. This frequency range is in agreement with simulations of the bandwidth of the shunt regulator.

The output of one linear regulator using the idle feature is shown in Figure 6. The idle feature is particularly interesting for pulsed powered operation schemes, such as anticipated at the ILC.

[1]Note that an optional hard reset (h_reset) can always set the chip back to the default configuration.

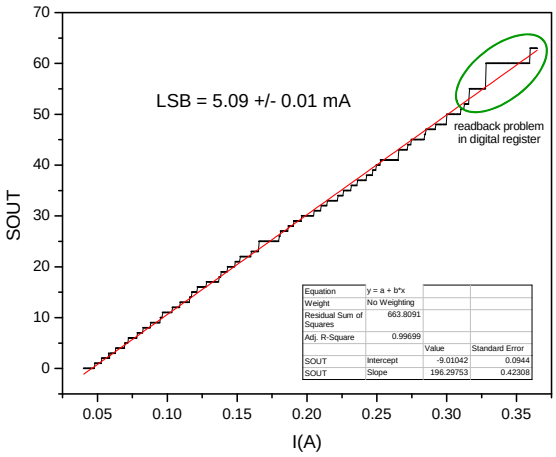

Figure 7: Digital response of shunt ADC as a function of shunt current.

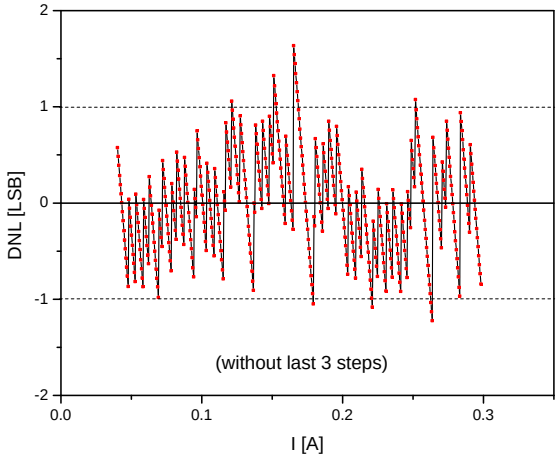

Figure 8: Differential-Non-Linearity of the ADC response excluding the last 3 steps.

In idle mode the output pad is decoupled from the linear regulator, and hence put into a high impedance mode. Since the falling edge of the voltage is mainly given by the output load it is not shown. The rising edge (upper trace in Figure 6) re-establishes the proper output voltage after about 500 ns. More detailed studies on the linear regulators have not been performed yet. However, the programmability of the voltage and the functionality of the idle feature have been fully tested.

The 6-bit shunt ADC has been tested as well. Figure 7 shows the digital read back of the ADC as a function of the shunt current. The response shows a few non-monotonic artifacts, most significantly at the end of the dynamic range. Most likely these artifacts are due to the same timing hazard in the digital controller that causes the toggling bits when setting the shunt voltage, and are not due to limitations in the ADC design itself. A correction of the digital control block is expected to straighten the ADC response at the same time. Figure 8 illustrates the differential-non-linearity (DNL) obtained from Figure 7, excluding the last three steps. The analog noise of the circuitry, derived by observing the step response between two adjacent digital values, is about 65 μA and hence negligible compared to the LSB setting of about 5 mA. The most important feature of the shunt ADC is to coarsely monitor the dissipated current and to report over-current conditions rather than to perform highly spectroscopic purposes. The design specifications determined 4-5 effective bit resolution as being sufficient for this task. Hence, the present implementation is certainly usable for this purpose. The current alarm flag using the programmable threshold has been tested as well, and can be used to indicate over-current conditions.

4. Protection schemes using the SPi

If a module that is serially powered by SPi fails, it is desirable to shut down the module. The most efficient way to do this, is to use the power FET of the SPi to bypass the full module current. This will collapse the module voltage, shut down the module components, and reduce the SPi functionality to a mere switch.

The static bypassing capabilities of the power FET are illustrated in Figure 9. A voltage source

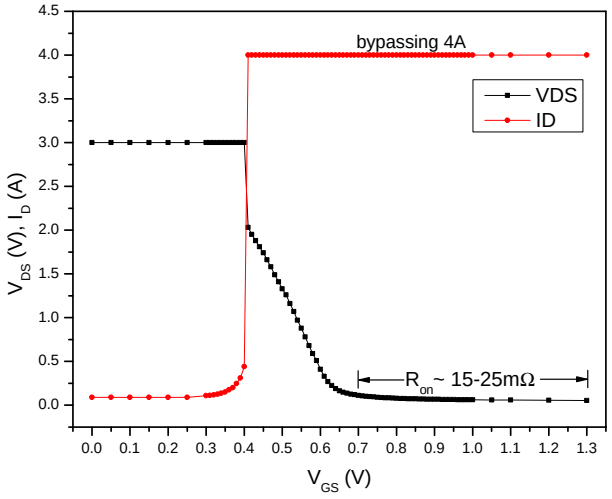

Figure 9: Static bypassing characteristic of the power-FET. The gate voltage is swept and the current (red) and voltage (black) across source and drain of the FET are shown.

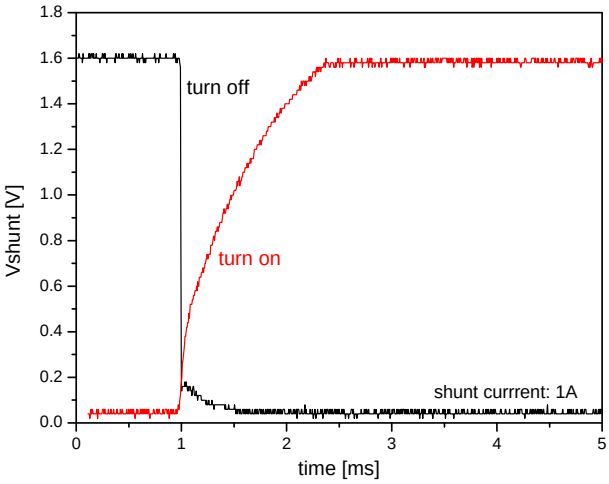

Figure 10: Dynamic switching characteristic of the power-FET bypassing a shunt current of 1 A.

of 3 V, current limited to 4 A is attached to the transistor's source and drain. To characterize the FET only, the SPi shunt regulator is disabled. The voltage (black) and the current (red) are shown as a function of the gate-source voltage. Below the NMOS threshold voltage of about 400 mV the voltage across the transistor is given by the voltage source, and only a small SPi bias current is drawn. Above the NMOS threshold voltage the full 4 A current is conducted through the chip and the voltage collapses. The chip voltage, and hence the module voltage is then determined by the magnitude of the bypassed current and the on-resistance of the power FET. For gate-source voltages of 700 mV and higher the on-resistance is about 20 mΩ, which means that the module voltage collapses down to about 80 mV (at 4 A). This leads to a total power consumption of 320 mW, which is comparable to or smaller than that of a typical read out chip. Special design techniques have been carefully applied to avoid electro-migration issues on the chip, so that high currents of 4 A should be able to be conducted for long periods of time. However, long time studies are still needed to confirm this capability.

To characterize the SPi bypass behavior dynamically, the power FET's gate was driven by a protection circuit that has been successfully exercised with discrete components in the past [11]. A 1 A current source is used to power the SPi regulator in parallel with a 2 Ω load. Figure 10 shows the chip voltage when triggering the power FET, turning the chip off (bypassing) and turning it back on. In the normal operation mode, the default voltage of about 1.5 V as anticipated is established. In bypass mode, the power FET shorts the module to less than 50 mV. The asymmetry in the switching times is primarily given by the driving circuitry, and in both cases the response time is sufficient for a slow-controlled disabling/enabling of a module.

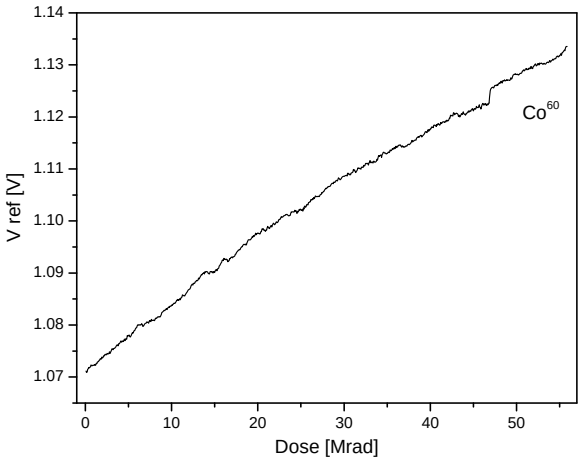

Figure 11: Reference voltage of the chip as a function of radiation dose.

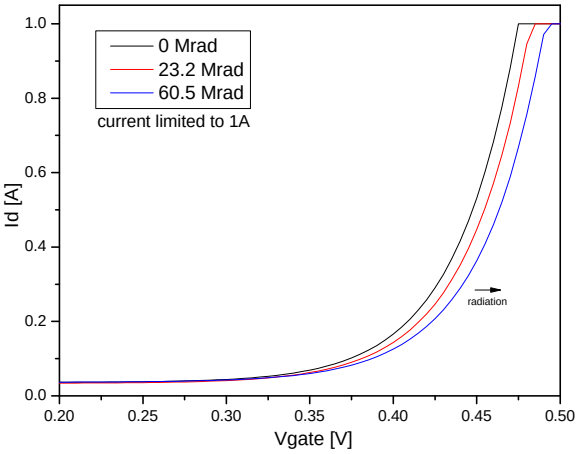

Figure 12: Transistor characteristic of the bypass power-FET on the SPi chip before radiation and after 23.2 and 60.5 MRad dose showing minor threshold shift.

5. Radiation Studies

The radiation hardness of the SPi chip against ionizing radiation has been tested using Cobalt 60 gamma rays. Well known layout techniques such as annular NMOS have been used in the SPi design to make the design as radiation tolerant as possible. However, the current version of the chip does not feature SEU tolerance. Triple redundant logic and similar measures could be implemented easily in a future iteration, if necessary.

Two aspects of the chip have been studied concerning radiation. First, shifts in voltages that are generated on the chip and second, the properties of the power FET. The chip uses an internal voltage reference of 1 V to derive the shunt voltage as well as the voltages provided by the linear regulators. The dependence of this reference voltage as a function of ionizing radiation is shown in Figure 11, up to a dose of about 60 MRad. During irradiation the chip was biased with about 100 mA shunt current while the voltage was monitored. The total shift in voltage is about 60 mV, equivalent to 6 %.

Figure 12 shows the transfer characteristic of the power FET before irradiation and at a dose of 23.2 MRad and 60.5 MRad. The power FET has not been operated during irradiation since this is the default case in real operation. The set of curves in Figure 12 show a minor shift in threshold compared to the expected voltage swing of at least 500 mV to trigger the bypass switch. Hence, the power FET is still fully capable of bypassing the module current after being exposed to 60 MRad.

6. Conclusion and Outlook

The SPi 001 chip has been fabricated to serve as a versatile power manager on the module level in order to explore serial powering schemes for the upcoming sLHC experiments. The chip uses advanced assembly methods based on bump bond technology and provides highly integrated functionality. Standalone tests have confirmed the functionality of the chip. A minor flaw in

the digital part has been identified which, most importantly, does not prevent the general use of the chip. Highlighting the most interesting features, SPi 001 offers a voltage range from 1.2 to 3 V and shows an outstandingly low dynamic impedance of 50 mΩ. Module failure detection can be provided by monitoring the current consumption and distribution on a module. Power down scenarios were investigated showing the capability to handle module currents of 4 A and more. Radiation tolerance against ionizing radiation was studied up to 60 MRad. Next steps are field tests using the SPi to serial power modules equipped with present readout electronics and sensors to demonstrate the full potential of the chip.

7. Acknowledgements

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