PROCEEDINGS OF SCIENCE

The Belle II Pixel Detector for the SuperKEKB Flavour Factory

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The upgrade of the KEKB e^+e^- asymmetric energy collider in Tsukuba, Japan to SuperKEKB will increase the instantaneous luminosity by a factor of 40. A significant increase in background and data rate of the vertex detector is expected, which cannot be handled by the current Belle design. To cope with these demands a new inner detector is under development and it is currently being extensively tested. This paper describes the DEPFET technology used for the pixel detector with its key features which proved to be a suitable solution for the Belle II detector. In addition, all involved readout electronics as well as the DAQ system are presented. The latest test beam campaign and its results are also described.

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1. Overview of SuperKEKB and the Belle II detector

In order to observe rare meson decays, high statistics and a large number of events are required which as their side product induce a harsh radiation environment in the interaction and surrounding regions. Especially the vertex detector needs to be able to resolve single tracks with high precision to reconstruct accurate vertex points in this environment. Large data samples and excellent decay vertex resolution are crucial to search for deviations in the Standard Model.
The asymmetric e^+e^- (4 GeV, 7 GeV) energy collider SuperKEKB located in Tsukuba, Japan is an upgrade of KEKB and will provide a 40 times higher instantaneous luminosity. This is achieved by a new beamline and a magnetic design using the so-called "nanobeam"-scheme to create denser bunches with a beam spot size of 10 μm $\times$ 60 nm at the interaction point and two times higher current. The center-of-mass energy of the collider is designed to be at 10.58 GeV, the mass of the $\Upsilon(4S)$ resonance, which decays into $B\bar{B}$ mesons. An upgrade of the former Belle detector, called Belle II is required to fully exploit the increased luminosity. For fast and precise track reconstruction the vertex detector, consisting of two layers of a highly segmented DEPFET based Pixel Detector (PXD) and four layers of a double-sided Silicon strip Vertex Detector (SVD) [1] are inserted near the interaction region, complemented by a drift chamber. For particle identification a T.o.F. Cherenkov detector, calorimeter and muon detector are installed. [2]
The beam pipe at the collision point is made of an Beryllium alloy and has an radius of 10 mm with a thickness of 1 mm. Therefore, the first detector layer can be placed very close to the interaction point at 14 mm. This requires compact, possibly self-sustaining modules in the inner layer to fit the mechanical constraints. To still benefit from the close location and with it the high resolution, a low material budget of 0.2 X_0 per layer is required to comply with a 10 μm vertex resolution, which is limited by multiple scattering. A pixel size of 50×50 μm and a thickness of 75 μm is sufficient to fulfill the requirements and keeping a high signal-to-noise ratio. The thickness was also chosen as a compromise between space for charge distribution within the detector to create an average cluster size of two pixels and keep the material budget low. Another layer is located 22 mm from the interaction point. Both layers need to cover an angular acceptance range between 17° and 150°. Simulations suggest a radiation dose from background at the full luminosity of around 2 Mrad per year. [3]
To keep the occupancy of the detector below 3 %, a continuous readout of the pixel detector with one complete read cycle within 20 μs is required. Since the data rate is dominated mostly by non-physics-relevant background hits and the storage cannot handle the full data bandwidth, a reduction of a factor of 10 is required in the DAQ chain.

A technology satisfying all these demands (fast, precise, radiation hard with low material budget) was found in the DEPFET sensors, which are described in the next section.

2. The DEPFET Sensor

A DEpleted P-channel Field Effect Transistor (DEPFET) [4] pixel cell consists of a MOSFET structure on a fully depleted high-resistivity n-type substrate bulk as depicted in Figure 1a. At a distance of 1 μm below the transistor channel an additional n-implant causes a potential minimum for traversing electrons. Stored electrons in this so-called internal gate induce mirror charges in the gate, which in turn modulates the p-channel current. The change in this current is measured over the drain contact. A particle crossing through the active area creates, according to the Bethe-Bloch equation, a average number of electron-hole pairs, depending on its energy. The momentum of the particle can be estimated by the number of electrons, stored in the internal gate, determined by the modulated drain current. Because a transistor is already included in the pixel cells, the sensor has an internal amplification g_q, which was measured in a prototype structure of to be around 500 pA/e^-. [5]

The capacity of the internal gate and its parasitic coupling to the gate can be controlled by the doping concentration. To achieve a low noise the parasitic capacity to the gate should be low, while the internal capacity should be sufficiently high to store all electrons. A compromise between storage and parasitic capacity was accomplished with a noise level of $\sim$ 50 nA, mostly dominated by the readout electronics.

With higher occupancy of the internal gate the potential minimum starts to decrease. To prevent a saturated internal gate a clear process is required as depicted in Figure 1b. In an equivalent circuit the clear process is realized over a second transistor turned by 90° forming an n-channel between internal gate and clear contact, once the clear-gate is activated. The electrons are then removed over this n-channel. During charge collection in the internal gate (clear-gate off), the clear contact is protected from accidentally removing electrons by a deep p-well implant.

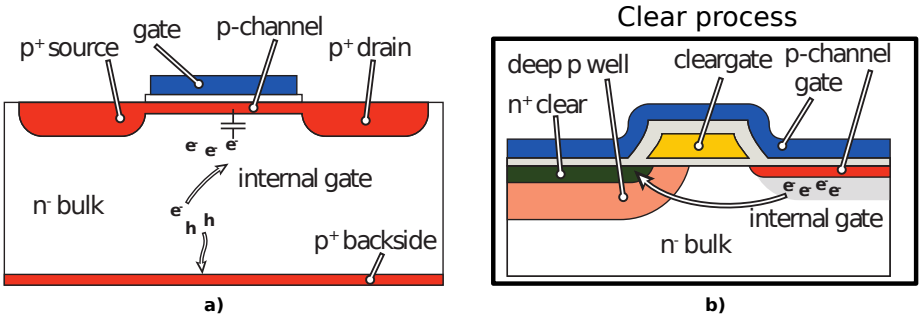

Figure 1: Simplified illustration of one DEPFET pixel cell (a) and its clear process (b).

2.1 DEPFET Half-Module

The DEPFET pixel cells are arranged in a matrix containing 250×768 pixels, which is called a half-module. All clear and gate lines of each row and all drain lines of one column are connected. In order to speed up the readout of the entire sensor, in the Belle II design four gate and clear lines are steered at a given time, while the drain current is read out. This method is called "rolling shutter"-mode. Only active rows consume power, while the other pixels are still sensitive to charge.

One sensor contributes only 1 W to the total 9 W power dissipated by one half-module. In order to place the required steering and readout ASICs outside of the sensitive area, long drain, gate and clear lines are used as depicted in Figure 2.

Three different types of ASICs are required to operate a DEPFET half-module. The Switchers are responsible for driving the gate and clear lines and are placed on a balcony on the side of the module. Each Switcher has 32 channels and steers four gate and clear lines simultaneously, thus 6 of them are needed for one half-module. The Drain Current Digitizer (DCD) digitize the incoming drain current in 256 channels with an upstream connected transimpedance amplifier. To read all 1000 channels ($4 \cdot 250$) four DCDs are required, placed at the bottom of the module. For further signal processing each DCD has a corresponding Data Handling Processor (DHP) to perform pedestal subtraction, zero suppression and data transmission over a 50 cm long and thin kapton flex cable with four 1.6 Gbps high speed serial LVDS lines. This kapton cable also provides all power lines and slow control signals.

A four-row readout cycle was measured to take at minimum 92 ns. Using a 100 ns cycle a full frame readout would take 19.2 μs, which fulfills the Belle II requirements of equal or less than 20 μs.

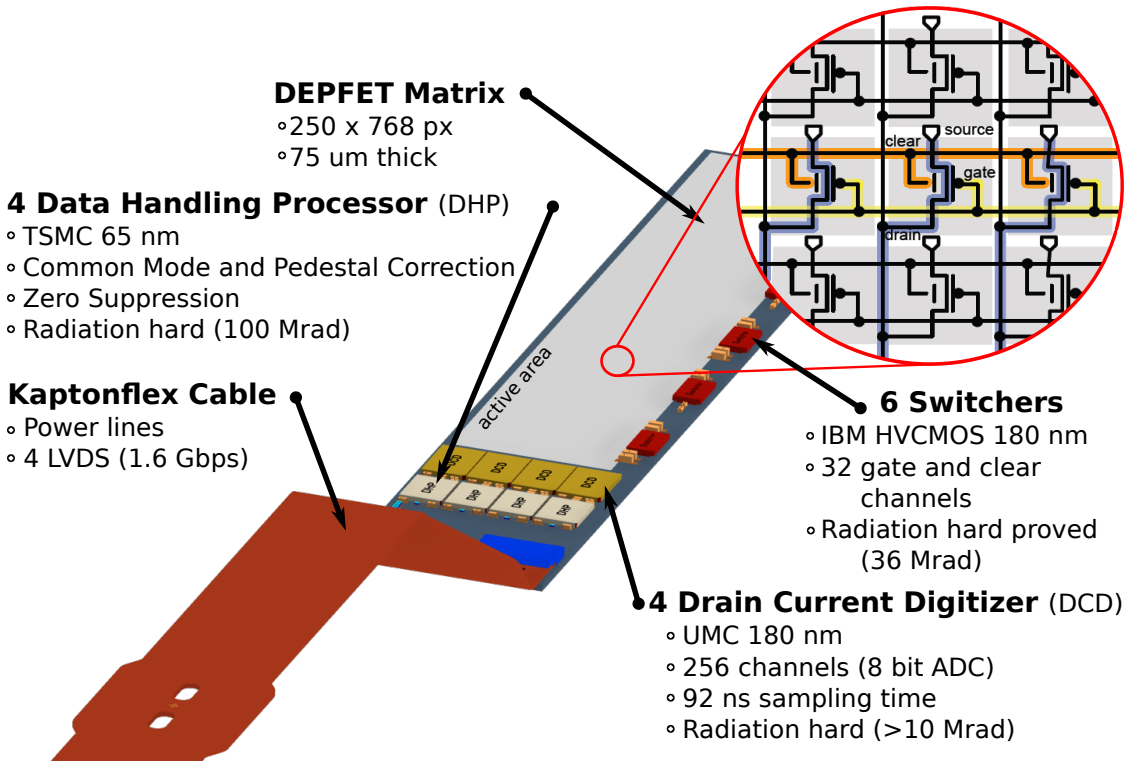

Figure 2: DEPFET half module for the Belle II Pixel Detector with all readout ASICs, transmission and power cabling.

	Layer 1	Layer 2
# Ladders	8	12
Radius	14 *mm*	22 *mm*
Ladder Size	15×136 *mm*	15×170 *mm*
Pixel size	50×55 μm 50×60 μm	50×70 μm 50×85 μm
# Pixels	250×1536	250×1536
Thickness	75 μm	75 μm

Table 1: Properties of the pixel detector and key features of the sensors.

3. The Belle II Pixel Detector

Two half-modules combined, glued together at their transition, and further reinforced with ceramic rods, form one full ladder. To build the pixel detector for Belle II 8 ladders for layer 1 and 12 for layer 2 are needed. The ladders are arranged in a so-called windmill structure to create an overlap between sensitive areas and avoid gaps. Table 1 summarizes the properties of each layer and its sensors. The pixel sizes of the PXD sensors are divided into two groups between the central and outer regions. Pixels with smaller sizes are located at the central region to improve the resolution with perpendicular traversing tracks, while in the forward region the incident angle is smaller, so the probability of creating clusters with two pixels increases. The larger size also prevents the charge cloud from spreading over too many pixels, which would decrease the resolution.

The occupancy of the PXD sensors is crucial for the optimal operation and design of the readout ASICs, thus extensive simulations were done and are still ongoing to get an idea of the expected background levels. Figure 3 shows the latest simulation results of the different contribution and distribution of the major background sources. The inner layers has the highest background level, causing an occupancy of ~ 1 percent, the one for the second layer is a factor of two lower. Synchroton radiation is one of the major background sources, which are still under investigations. First estimation shows that this background adds an additional 0.2 percent. The asymmetry in the occupancy of the different ladders is exploited to load balance the data. In an average $B\bar{B}$ event about 10 tracks are created; compared with the current background level, the occupancy of the PXD is completely dominated by background hits. The outgoing detector bandwidth can be significantly reduced by removing part of the background hits.

3.1 DAQ System

The kapton flex cable of each half-module is connected to a patch panel, which splits up high-speed serial data links, slow control JTAG signals and power lines. Several different voltages are required to power the DEPFET module and its mounted ASICs.

For data transmission the patch panel is connected over two high quality 15 *m* long Infiniband cables to the Data Handling Hybrid (DHH), which receives the four high speed links from four DHPs. To ensure a correct transmission a link driver with pre-emphasis was implemented in the DHP. It was tested up to a bandwidth of 1.6 Gbps. [6] An eye-diagram to check the link stability is shown in Figure 4. The opening of the eye determines the quality of the data transmission, in this case it

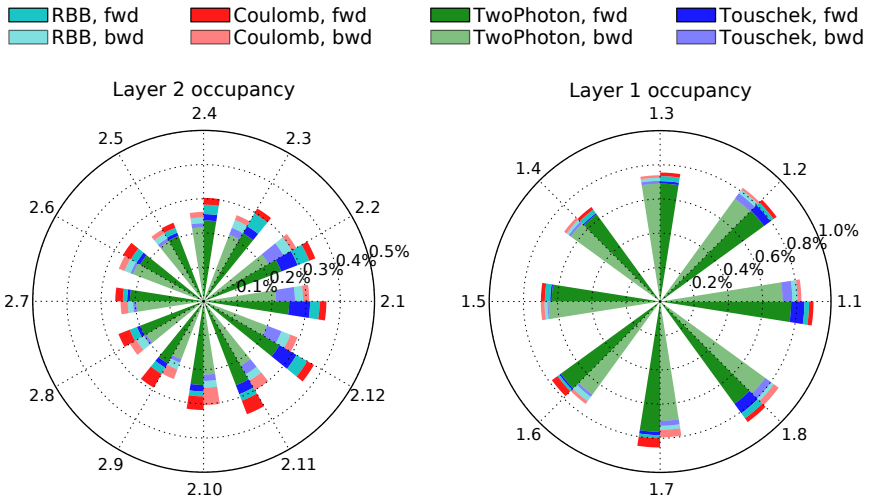

Figure 3: Simulation results on the expected background level, split up by their different sources.

is still sufficiently open to ensure a stable connection.

The DHH system is build on the ATCA standard with Xilinx Virtex 6 FPGAs performing a data load balancing. As seen in Section 3 the asymmetry in the background can be exploited to combine sensors with low occupancy with sensors suffering from high background. 5 DHH (two half-modules from layer 1 and three from layer 2 on the opposite side) are connected to one DHH Controller (DHHC). The DHHC aggregates the incoming data stream and converts from LVDS lines to optical signals. Further, the DHH provides the slow control to the DHPs, which in turn control all the other ASICs, e.g. the sequence for the Switchers, or offset settings for the DCD.
A further data load balancing is achieved in the four 6.25 Gbps optical link connections between each DHHC and the ONline SElector Node (ONSEN), over a programmable write sequence. The ONSEN system is based on the xTCA standard using Advanced Mezzanine Cards (AMC) to receive on one AMC two optical links from DHHCs. The pixel data are written out over one Gbit Ethernet link per AMC to the storage farm. In order to fit the data bandwidth on this link a reduction is needed as described in the next section.

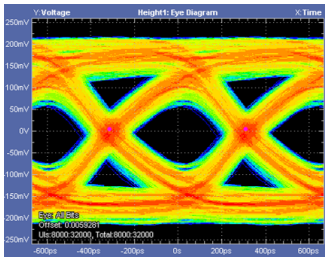

Figure 4: Eye diagram of the transmission line between DHP and DHH with an 15 *m* long cable. The DHP was irradiated with 100 *MRad*. [7]

3.2 Data Reduction

For the data reduction the hit information of the surrounding Silicon strip Vertex Detector is utilized to define so-called Regions of Interest (ROI) in the PXD. Only hit information of the pixels located inside these ROIs are saved. The ROIs are computed by reconstructing track segments from strip data and extrapolating them to the pixel detector layer. The goal is to achieve a data reduction of up to a factor of 10 with this ROI selection. When the pixel raw data are not saved in ONSEN and

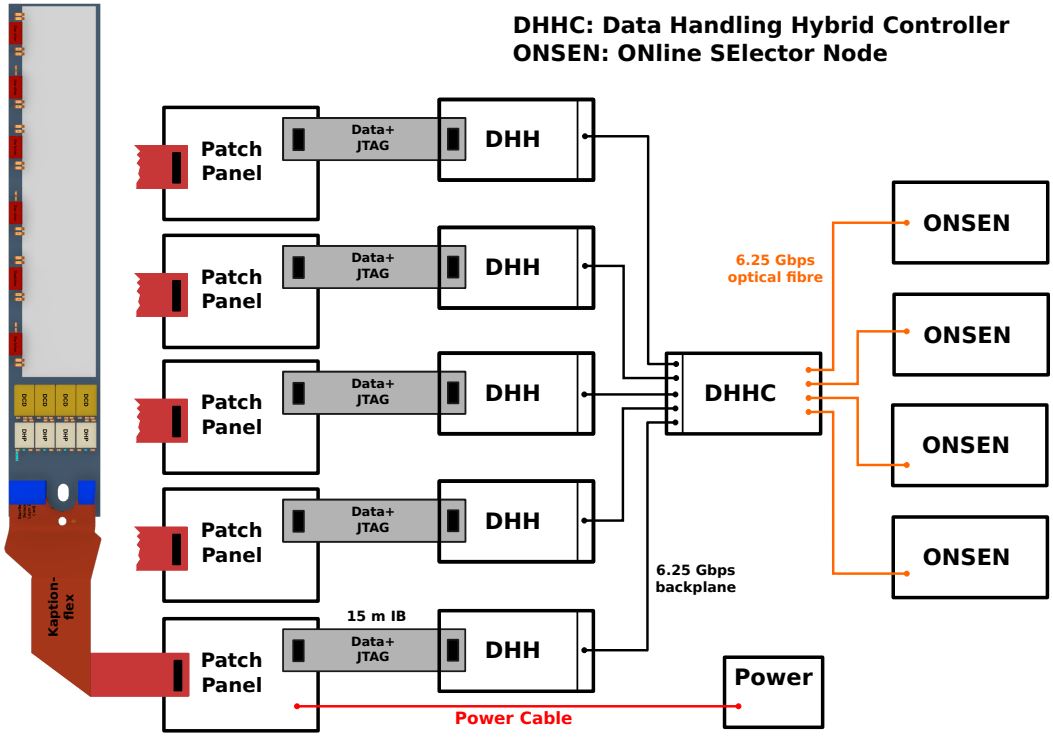

Figure 5: Overview of the Belle II PXD DAQ system.

written to disk, they are lost. Thus, a complementary approach was defined using three different systems with a different algorithm to ensure that as much physic relevant information are saved as possible:

- High Level Trigger (HLT): A compute farm using a sector-neighbour finding algorithm with an Hopfield network and the Genfit library to create ROIs. [8]
- Data Acquisition Tracking and Concentrator Online Node (DATCON): FPGA-based system using the Fast Hough Transformation and pre-calculated lookup-tables to provide the ROI.
- Cluster Rescue: A neural network analyzing the PXD cluster charge and distribution to identify possible low-momentum particles, implemented in the FPGA of the DHH.

4. Latest Test Beam Campaign

The performance and characteristics of the DEPFET sensor were demonstrated at several lab tests and test beams over the past years. The test beam described in this paper aimed not only at testing the sensors but also the cooling and the whole DAQ system, including the data reduction scheme and the software developed for slow control, alignment and data quality monitoring.

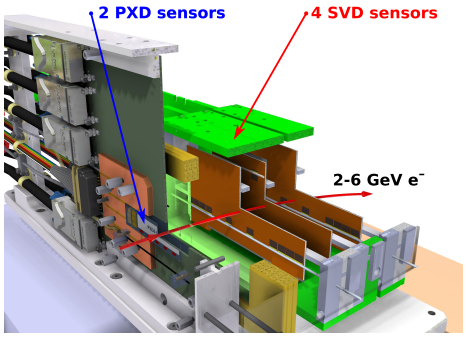

Figure 6: Vertex Detector test beam setup at DESY.

The test setup consisted of four SVD and two PXD sensors, one sensor representing one layer of the detector placed at a distance corresponding to the final geometry. Figure 6 shows the layout with the mechanical support structures and the trajectory of an electron traversing the setup. DESY provides a directed electron beam with flexible energies between 2 and 6 GeV. In addition, a solenoidal magnet field of up to 1 T was used in several steps. One of the PXD sensors were damaged, so only one sensor was installed during the test beam to prove the working principle.

The former with a smaller matrix and the current setup are compared in Figure 7. The sensor on the left consists of 32×64 pixels with one Switcher, DCD and DHP mounted on separated pieces of silicon connected to the sensor with wire bonds. The new all-silicon module (Figure 7b) has a sensor with 192×480 pixels and four Switchers, three DCDs and DHPs, which is close to the final design, and was operated for the first time.

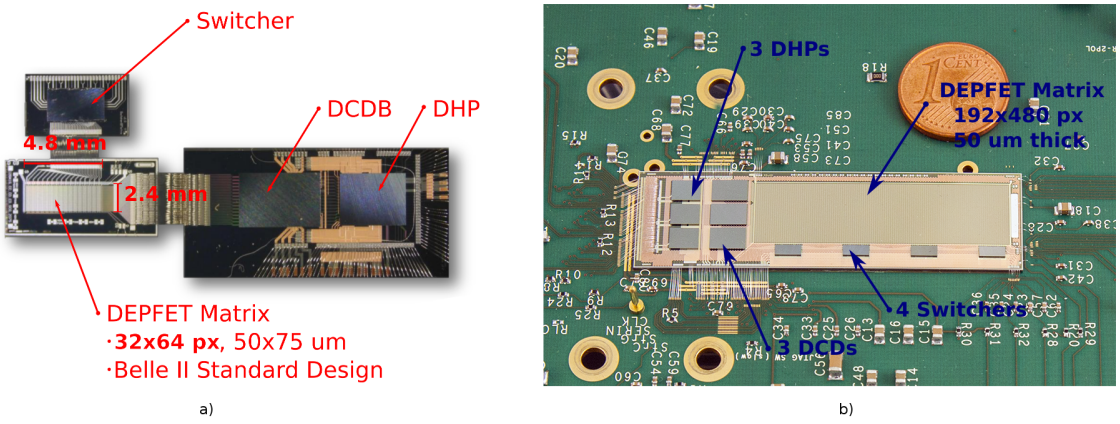

Figure 7: Comparison of the a) former (32×64 pixel matrix) and b) current test beam setup (192×480 pixel). For the first time a thin, multichip DEPFET module was produced and operated with the DAQ system.

4.1 Results

In several days long runs, the long-term stability of the system was successfully tested up to a trigger rate of 1.5 *kHz*. Figure 8 shows a visualization of one event, taken with the full DAQ and

software chain. It shows the successful operation of the ROI data reduction scheme (one hit inside the PXD sensor was saved in this figure), the correct decoding and merging of SVD and PXD data with a common trigger source and the required software tools for analysis. The beamspot was also clearly visible in the accumulated ROI and PXD hit map. For further optimization and development the 10 million recorded events can be used to test and tune certain aspects of the system, e.g. for adding the correct alignment for the online track reconstruction systems. In addition, service structures such as the CO_2 cooling system [10] and the power supply [11] for the PXD sensor were tested.

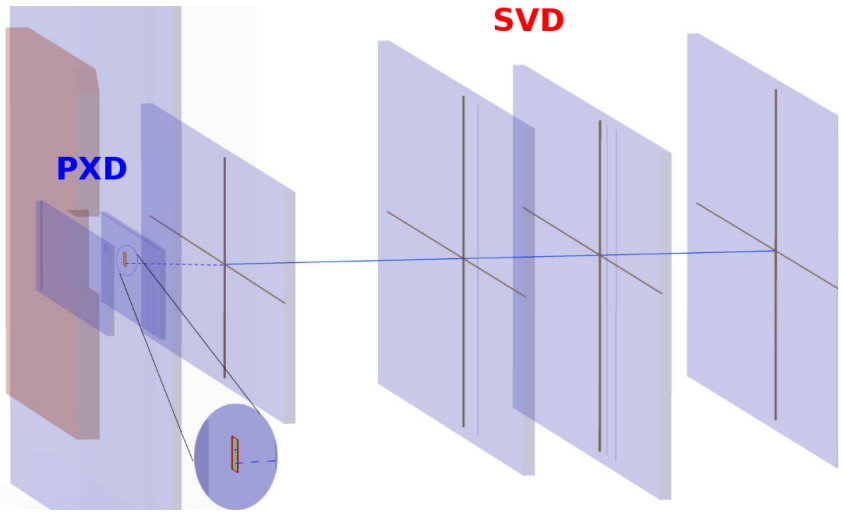

Figure 8: Visualization of one event from the test beam. One track is traversing through the SVD, firing strips. From the strips the track parameters are reconstructed and extrapolated on the one PXD layer, where a ROI is created. [8]

5. Conclusion

The DEPFET technology proved to be a suitable solution for the Belle II pixel detector to cope with the high occupancy in the inner layers at the required readout speed and the dense space constraints with low material budget. A first almost full-size self-sustaining DEPFET module was operated in the DESY test beam, not only showing the working conditions of the sensor, but also of the entire readout DAQ chain. The gathered experience in the long-term operation influenced new developments for the final Vertex detector, e.g. a common grounding scheme. The production of the sensors are ongoing and a first full Belle II half-module is expected to be tested in the next test beam campaign towards the end of 2015.

6. Acknowledgment

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