

Status and Performance of the CDF Run II Silicon Detector

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The CDF Run II silicon detector with its 8 layers of double- and single-sided silicon micro strip sensors and a total 722,432 readout channels is one of the largest silicon detector devices currently in use by a HEP experiment. We report our experience commissioning and operating this complex device during the first 4 years of Run II. As the luminosity delivered by the Tevatron collider increases, we have observed measurable effects of radiation damage in studies of charge collection and noise versus applied bias voltage at many different integrated luminosities. We discuss these studies and their impact on the expected lifetime of the detector.

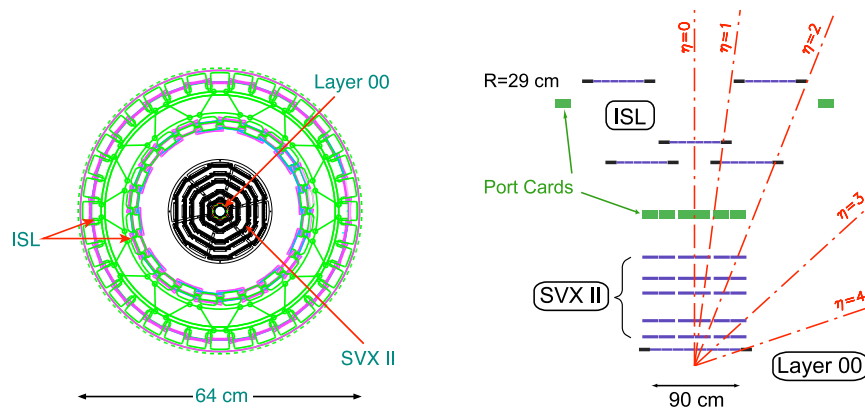
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Figure 1: Axial and r - z views of the CDF silicon detector.

1. Introduction

The CDF experiment completely replaced its silicon vertex detector for the Tevatron Run II physics program, which requires improved acceptance, impact parameter resolution, and heavy flavor tagging efficiency over the Run I silicon detectors. The resulting detector, shown in Figure 1, incorporates 8 layers of double- and single-sided silicon read out through 722,432 channels. It is one of the largest silicon detectors currently in use by a HEP experiment.

The core of the new detector, SVX II, consists of 12 identical wedges in ϕ , tightly aligned and quickly read out in parallel for use in an innovative hardware displaced track trigger, SVT. Each wedge contains 5 layers of double-sided silicon, oriented parallel to the beam pipe at radii from 2.5 to 10.6 cm, with axial strips along the p - n junction side. The other side has 90° stereo strips for 3 of the layers, and 1.2° stereo strips for the remaining 2 layers. Between SVX II and the CDF wire tracking chamber, ISL provides 1.2° stereo double-sided silicon with a single layer for an intermediate radius measurement of central tracks ($|\eta| < 1$) and two double-sided layers for tracking in regions without full fiducial wire tracker coverage ($1 < |\eta| < 2$). Inside SVX II lies Layer 00, a single layer of silicon built directly onto the beam pipe at a radius of 1.5 cm. Because of its proximity to the interaction region, Layer 00 uses actively cooled silicon, read out with axial strips on one side only and capable of much higher bias voltage to outlive the innermost layers of SVX II. Layer 00 provides precision position measurement before any multiple scattering occurs in portions of the extensive DAQ and cooling infrastructure that lie within the tracking volume.

2. Operational Experience and Performance

Commissioning and maintaining the CDF silicon detector has been a challenge. It is a large and complex system rendered virtually inaccessible by installation in which several unanticipated problems developed. Epoxy blockages found after installation in 12 of the 34 ISL cooling lines made a significant portion of ISL sensors uncoolable and thus inoperable during early data taking. All but one of the blockages were successfully removed with a laser [1]. Problems with noise pickup in cables connecting Layer 00 to its readout electronics developed. Offline noise pedestal

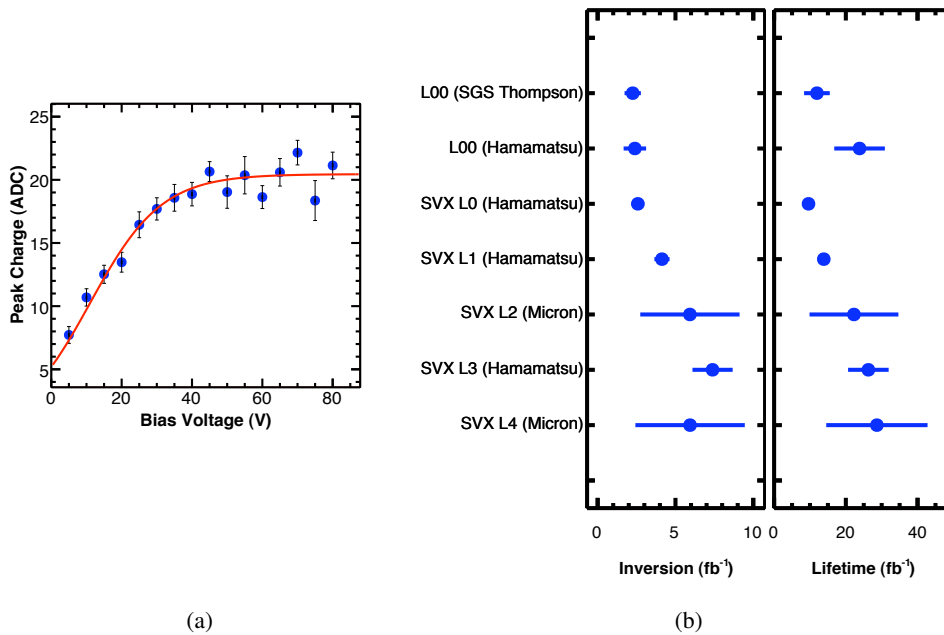


Figure 2: (a) Collected charge for a single Layer 00 DAQ unit, combining two sensors, versus applied bias voltage. (b) Mean and RMS of individual sensor predictions, based on scans taken between 0.2 and 1.3 fb⁻¹ of integrated luminosity, for type inversion and for a lifetime limit due to charge collection inefficiency obtained by assuming the same rate after inversion.

subtraction solved these problems but required removal of Layer 00 from SVT [2]. During DAQ testing, readout chips on the stereo side of SVX II ladders began to fail consistent with the loss of 2-mm-long wirebonds providing these chips with power. Vibration and subsequent breaking of the wirebonds, which for certain readout frequencies resonate due to Lorentz forces in the CDF 1.4 T solenoidal magnetic field, caused these failures [3]. DAQ reprogramming to minimize wirebond current and avoid resonance conditions, and a hardware board that recognizes resonance conditions and halts the DAQ when they arise, has avoided additional failures.

Approximately 84% of SVX II, 82% of ISL, and 96% of Layer 00 produce data with a digital error rate of less than 1%, numbers which have held constant since mitigation of the wirebond resonance problem. The small number of failures incurred since commissioning has coincided with thermal cycles and beam incidents. Beam incidents have the potential for significant damage, with the first major incident damaging 31 out of a total 3168 SVX II readout chips. An additional beam collimator and other protection developed in response to this incident has greatly reduced the number of subsequent beam-induced failures, but beam incidents continue to be a concern.

Accessing the silicon sensors is impossible, and thus maintaining this high level of performance for the next 4 years is a significant challenge. Daily silicon operations require 5 to 10 FTE for a vigilant group of monitoring experts with dedicated shifts to rapidly spot problems and for aggressive reaction to new problems by a hierarchy of on-call postdocs and graduate students. Most problems must be solved either by repairing power supply and DAQ infrastructure in the collision hall or by reprogramming inaccessible readout electronics to minimize the effects of damage.

3. Detector Lifetime

Aging effects due to long term irradiation are the primary concern for the lifetime of the detector. CDF expects 5 to 8 fb⁻¹ of integrated luminosity by 2009 and has made a broad effort to study the effects of beam- and collision-induced radiation on the silicon sensors and readout electronics, including measurements of the radiation environment in and around the tracking volume [4]. These studies suggest that the strongest constraint on lifetime is charge collection efficiency, which for the innermost layers of SVX II may degrade beyond usefulness in the final year or two of running [5].

Sufficient charge collection requires application of a bias voltage between the two sides of each silicon sensor so that a region depleted of charge extends throughout the sensor bulk. The required voltage evolves as the sensor bulk gradually changes from net *n*-type to *p*-type under irradiation and annealing, first decreasing until type inversion occurs, then increasing, eventually surpassing the maximum voltage that can be applied. In SVX II, the capacitively coupled readout design and concerns about micro discharge limit the maximum safe bias voltage to 160 V for the three 90° Hamamatsu silicon layers and 60 V for the two small angle stereo Micron silicon layers. In Layer 00, the limit is currently 500 V, the maximum capability of its power supplies.

In part because of the large uncertainties on available predictions, we monitor the depletion voltage using two methods. For Layer 00, we study the charge collected for hits on well-measured tracks for many applied bias voltages, as shown in Figure 2a. This method requires a substantial amount of dedicated beam time. For SVX II, which has readout strips on both sides of the sensor, the depleted region begins on the *p* side of the sensor and extends to the opposite side as larger bias voltage is applied, driving the inter-strip noise down and providing a way to estimate the depletion voltage without intruding on beam time. The two methods give similar results, and both types of bias voltage scans are taken regularly as luminosity accumulates.

Preliminary results are consistent with the predictions in [5]. Type inversion, as shown in Figure 2b, should occur for the inner layers of the detector in the next 1 fb⁻¹ of integrated luminosity. Measurement of the rate after inversion is crucial to any conclusions about detector lifetime; however, if one assumes the same rate after inversion, one obtains estimates shown in Figure 2b. As suggested in [5], this number should be regarded as an upper limit on the lifetime of the detector.

References

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