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Integrated electronic for SiPM and MPPCs

Pierre Barrillon
OMEGA/LAL/IN2P3
Université Paris Sud - Bâtiment 200 - 91400 Orsay, France
E-mail: barrillo@lal.in2p3.fr

Sylvie Blin
OMEGA/LAL/IN2P3
Université Paris Sud - Bâtiment 200 - 91400 Orsay, France
E-mail: blin@lal.in2p3.fr

Frederic Dulucq
OMEGA/LAL/IN2P3
Université Paris Sud - Bâtiment 200 - 91400 Orsay, France
E-mail: dulucq@lal.in2p3.fr

Julien Fleury[1]
OMEGA/LAL/IN2P3
Université Paris Sud - Bâtiment 200 - 91400 Orsay, France
E-mail: fleury@lal.in2p3.fr

Gisèle Martin
OMEGA/LAL/IN2P3
Université Paris Sud - Bâtiment 200 - 91400 Orsay, France
E-mail: martin@lal.in2p3.fr

Ludovic Raux
OMEGA/LAL/IN2P3
Université Paris Sud - Bâtiment 200 - 91400 Orsay, France
E-mail: raux@lal.in2p3.fr

Nathalie Seguin
OMEGA/LAL/IN2P3
Université Paris Sud - Bâtiment 200 - 91400 Orsay, France
E-mail: seguin@lal.in2p3.fr

Christophe de La Taille
OMEGA/LAL/IN2P3
Université Paris Sud - Bâtiment 200 - 91400 Orsay, France
E-mail: taille@lal.in2p3.fr

[1] Speaker

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Expectations on front-end electronics have deeply changed with the strong increase of channels in physics experiments and medical imaging. Integration has become a key issue to achieve low-cost and efficient readout of new photo-detectors generation.

The Orsay Microelectronic group (OMEGA) has developed an expertise in front-end chip to read out such photodetectors with a high level of integration.

A first version of SiPM readout chip has been designed and produced to read out the 8,000-channel Iron-Scintillator hadronic calorimeter prototype currently in test beam at CERN. An input DAC allows a channel by channel 5V adjustment on the SiPM bias ensuring a trimless tuning of the signal to noise ratio of every channel. The read-out chain embeds an AC-coupled charge preamplifier followed by a CRRC² shaper and a track and hold.

A new generation of System-on-Chip ASICs called SPIROC (standing for SiPM Integrated Read-Out Chip) is being designed embedding high-voltage fine adjustment, gain correction, amplification, filtering, analogue memory, analogue to digital conversion, digital memory, time measurement, self-triggering capability. This new stand-alone device will allow going further in the integration of high numbers of channels at low cost.

Several chip designed by the omega team will be presented and some example of integration will be developed.

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1. Introduction

The point of this paper is to describe features and performances of the most SiPM-suitable ASIC designed by the OMEGA group. Four ASICs are presented:

- FLC_SiPM: That chip designed in 2004 is currently operated to read out the 8000 SiPM of a tile Hadronic calorimeter prototype for the international linear collider.
- MAROC: Originally designed to read out MA-PMT for luminometry application, that chip is perfectly suitable for SiPM or MPPC readout.
- HARDROC: A new mixed signal front-end chip integrating analogue front-end and digital memory. Designed to read out RPCs, Hardroc features Maroc front-end therefore it can trig on SiPM single photoelectron.
- SPIROC : The very last chip from OMEGA, designed for SiPM readout. It features time measurement, self trigger, charge measurement, internal memory and many other capabilities useful for SiPM or MPPC readout.

2. FLC_SIPM presentation [1]

2.1 ASIC Chip description

An 18-channel ASIC chip dedicated to SiPM readout has been developed starting from the design, in AMS 0.8 µm CMOS technology, already in use for the Si-W ECAL prototype readout. *Fig. 1* shows a schematic view of this FLC-SIPM ASIC chip.

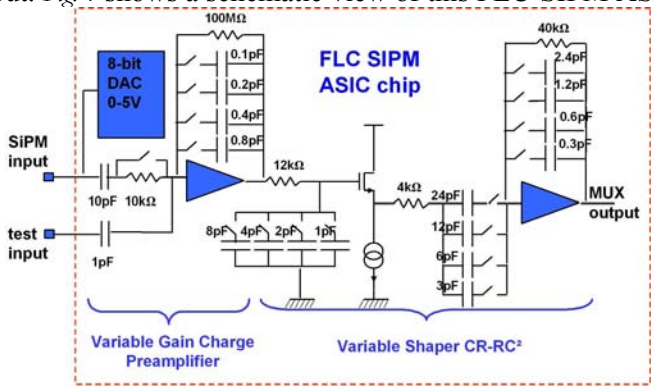

Fig. 1: Schematic view of ASIC chip components.

The integrated components allow the choice between 16 selectable preamplification gain factors from 1 to 100 mV/pC, and between 16 $CR(RC)^2$ shapers with shaping times from 40 to 180 ns. A 10 k resistor can be add at the input of the preamplifier to further delay the signal peaking time (at the expenses of a 40% noise increase). After shaping the signal is held at its maximum amplitude with a track and hold method and multiplexed by an 18-channel multiplexer to provide a single analog output to the ADC. An example of the signal path through the chip is given in *Fig. 2a-d*, where the stages of input, amplified and shaped, held and multiplexed signal are shown. The longest shaping time has been introduced in the ECAL design to match the long delay of the beam trigger in a test beam environment (~150 ns). For SiPM gain calibration using LED signal, pile-up from thermal noise-induced signals (dark rate) can be reduced by exploiting the fast SiPM response with a shorter shaping time. The large varaiety of operation modes offered by the ASIC chip gives the opportunity to amplify moe that only the SiPM signals with the same chip design. This is a big advantage as signals from monitoring devices like PIN-diodes or photomultipliers can be read out over the same chain. A

5V rail-to-rail 8-bit Digital to Analog Converter (DAC), integrated on each of the 18 input lines of the ASIC chip, allows individual adjustment of the SiPM bias voltage for each channel. In addition to the 18 signal inputs the ASIC chip provides two test inputs (each one common to 9 channels) to check the preamplification line decoupled from the SiPM.

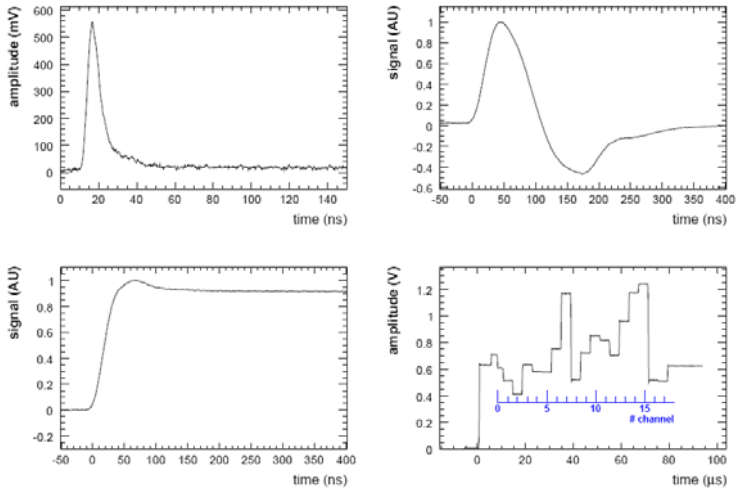

Fig. 2: Electrical signal processing in the ASIC.a) Input (×18), b) pre-amplified and shaped (×18), c) held (×18), d) multiplexed (×1) signal.

The properties of the ASIC chip relevant to the operation in conjunction with the SiPM have been tested using the test setup sketched in *Fig. 3*.

2.2 Linearity

The study of the linearity range of the ASIC chip for various combinations of gain and shaping time has been performed injecting current from an external capacitor (C1) to the ASIC chip input. By varying the value of the capacitor C1 it is possible to change the duration of the injected charge to mimic the real shape of a SiPM signal. *Fig. 4* demonstrates how the shape of the input signal is adjusted choosing a 68 pF capacitor. Each input channel of the ASIC chip is grounded via a 50 Ohm resistor and a 0.1 µF capacitor.

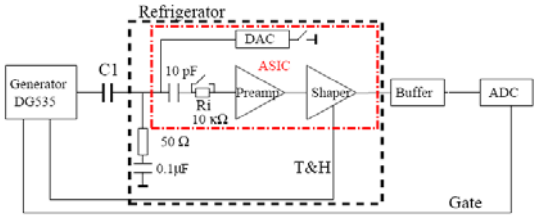

Fig. 3: Electronic set up for ASIC chip studies.

The output signal of each preamplifier and shaper stage is held at its maximum value by an external track & hold signal timed with the generator. The duration of the hold time is determined by the width of the hold signal, generally about 2-5 µs. A signal amplitude drop of 1 mV per 500 ns is observed. During this time the signal is measured on a peak sensing 12-bit ADC with a gate of 100-400 ns. The linearity range of the ASIC chip operated with longest shaping time (180 ns) is presented in *Fig. 5a*. The saturation of the input charge is visible which depends on the shape of the injected signal (or the value of the input capacitor C1). In *Fig. 5b* the gain factors for the various choices of capacitors are shown, which are calculated from a fit to the linear (± 3 %) part of the curves in *Fig. 5a*

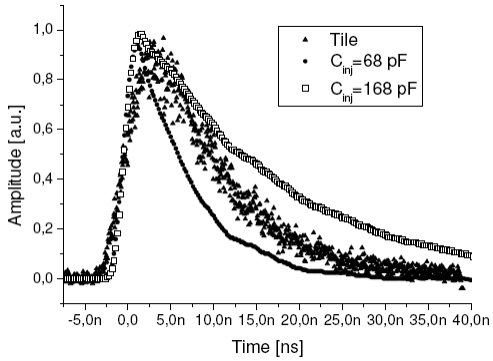

Fig. 4: Comparison of charge injected signal to real SiPM signal.

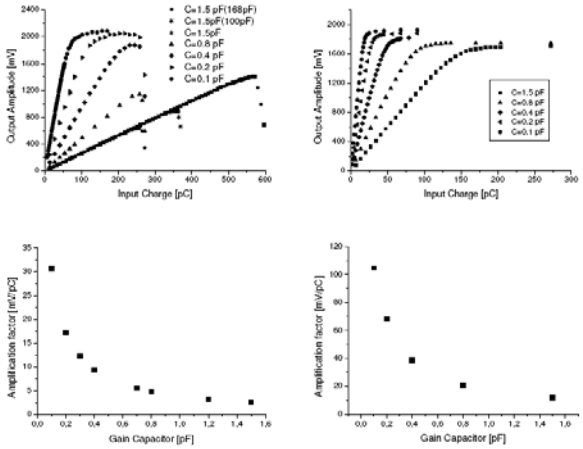

Fig. 5: Linearity of ASIC chip output signal for the longest (a) and shortest (c) shaping time and various gains. b-d) Relative gain factors as a function of the chosen capacitor.

The same values are evaluated from *Fig. 5c* and shown in *Fig. 5d* for the shortest shaping time (_40 ns). It can be observed that for low capacitors the increase of the gain value is not linear with the increase of the capacitor value. If the input is not saturated, the ASIC chip output saturates between 1.7 and 1.9 V depending on the gain. While the slopes of the curves in *Fig. 5a(c)*, as well as the absolute gain values reported in *Fig. 5b(d)*, are strongly changing depending on the value of the input capacitor C1, the output saturation level stays quite constant. We conclude that the ASIC chip can be used for SiPM-like signal readout in a linear range up to 1.3 V for all combinations of gains and shaping times.

2.3 Noise

In order to measure the noise contribution of the ASIC chip preamplifier the input line was grounded only via the 50 Ohm resistor in Fig. 3, removing the 0.1 μF capacitor. In this way, the noise of the DAC component is neglected. The noise is defined as the standard deviation (_) of the Gaussian fit to the noise spectrum of the ASIC chip for various combinations of gains and shaping times.

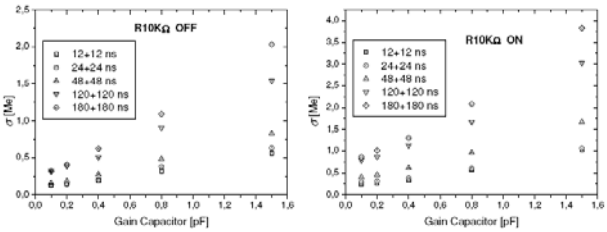

Fig. 6: Noise of the ASIC chip preamplifier, expressed in units of 106 electrons (Me), for various combinations of gains and shaping times. Bypassing (left) or using (right) the 10 k injection resistor Ri.

In *Fig. 6* the noise values are presented for the two operation modes in which the injection resistor (Ri) is used or bypassed. The noise is expressed in units of 10^6 electrons (Mega-electrons = Me). The amplitude of the SiPM signal for a single pixel firing (one photon signal) is approximately 1 Me, therefore the electronic noise should be smaller than this value to resolve single pixel structure. The best noise to gain ratio of 0.25 Me is obtained for the highest gain and the shortest shaping time, which is the mode adopted for single pixel calibration in the operation with SiPM.

2.4 Individual channel voltage adjustment (DAC)

As previously discussed, one of the requirements of the developed very front-end electronics is to operate a large number of SiPM, being able to individually steer their bias voltage. This is achieved by a voltage adjustment via a 8-bits DAC connected to the input of each ASIC chip preamplifier channel. The DAC covers effectively the range between 0.24 and 4.7 V, in steps of 20 mV. In Fig. 7 the linear range of the DAC output voltage is shown together with its noise. The voltage stability required for SiPM operation is on the order of 30 mV, corresponding to a change in gain for the SiPM of about 1%. The stability of the DAC is very well below this level.

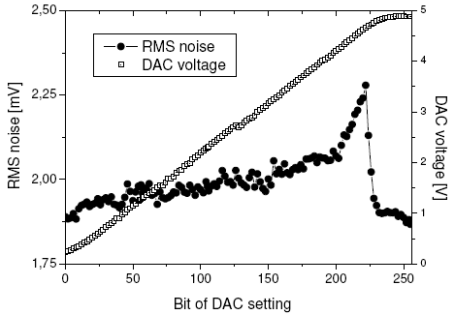

Fig. 7: DAC output voltage and noise as a function of DAC setting parameter.

A check was made to ensure the input of the DAC could tolerate the typical current from the coupling to the SiPM (5-0.3 μA). The maximum tolerable current at the DAC input was found to be 40-140μA depending on the DAC settings, compatible with the requirements. From this the dissipation power of the DAC has been calculated to be about 500 μW.

2.5 SiPM readout with the ASIC chip

Once established that all the ASIC chip characteristics are compatible with the type of signal and the requirements for which the chip was designed, one can proceed and integrate the SiPM to its very front-end electronics and study the property of the combined system. The studies presented in this section are performed for one single channel, to understand the effect of the readout electronics on the SiPM signal. The operation of a large number of SiPM with the same very front-end electronics will be discussed in a dedicated publication. The connection scheme of SiPM to the ASIC chip is shown in *Fig. 8*. The possibility to calibrate the SiPM gain is an important advantage of this type of photodetector. For this it is necessary to measure the separation of the single pixel peaks in the SiPM pulse hight spectrum. To achieve best separation with minimum noise contribution from the electronics and from the SiPM dark rate, the mode adopted to perform gain calibration is the combination of the highest gain (G=0.1pF) and the shortest shaping time (T=40ns).

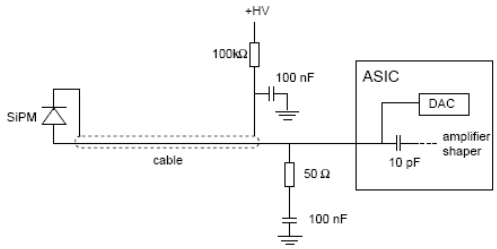

Fig. 8: Connection scheme of SiPM to ASIC chip.

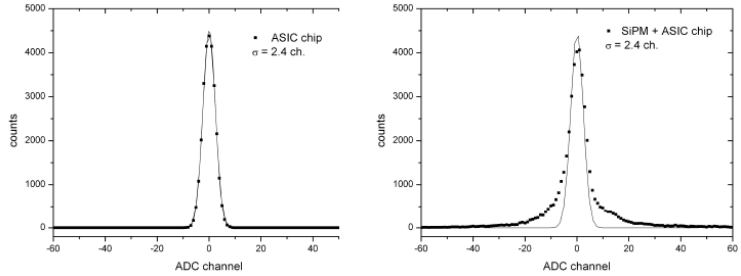

Fig. 9: Noise spectrum from the ASIC chip only (a) and SiPM connected to the ASIC chip (b).

The analog SiPM signal (not held) at the ASIC chip output is shown in *Fig. 5b*. The bipolar shape of the signal is obtained after the CR(RC)^2 shaper. Due to the SiPM dark rate the noise spectrum obtained with SiPM connected to the ASIC chip (*Fig. 9b*) deviates from the perfect Gaussian shape resulting only from electronic noise (*Fig. 9a*). The positive and negative tails in *Fig. 9b* are the result of thermal noise-induced signals hold at their positive or negative amplitudes. Given the equal widths of the two noise spectra in *Fig. 9a* and *9b* it can be stated that the SiPM noise is negligible with respect to the ASIC preamplifier noise. Using a low intensity light source it is possible to observe the single pixel structure in the SiPM pulse hight spectrum, as seen in *Fig: 10*. The separation of subsequent peaks is good and allows for a multi-Gaussian fit to determine the SiPM gain Δpeaks (here shown in QDC channels and not recalibrated to Me) and the peak widths. The signal to noise ratio obtained for single pixel signal is ~4, in agreement with the ratio extracted from the direct measurements of the ASIC chip.

During normal data taking the SiPM signal amplitude can vary up to the SiPM saturation which, for the 1024-pixel device used for the HCAL prototype, is at about 1250 effective pixels fired or 200 pC. It is possible to choose the preamplifier gain such that the amplified signal is contained in the linear range of the ASIC chip. The shaping time choosen for beam or cosmics data taking is fixed to the longest possible (T=180ns) by the requirement of the external trigger latency. It has been checked that choosing an intermediate gain (G=0.5pF).

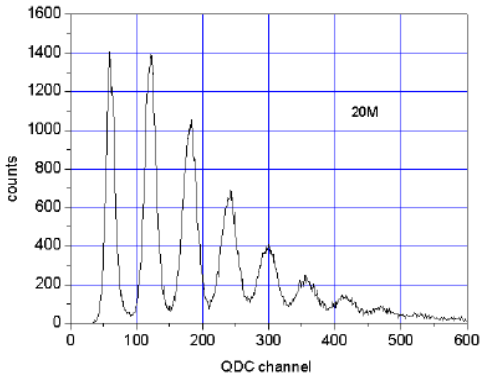

Fig. 10: Single photoelectron peak spectrum from SiPM with ASIC chip readout.

the SiPM signal saturates below the limit value of 1.3 V fixed to be in the ASIC linear range at the 3% level.

2.6 Conclusions

After this series of measurements we conclude that the ASIC chip FLC-SIPM developed by LAL, together with the very front-end electronics designed to steer it, can be used to readout and calibrate SiPM photodetectors. The dedicated very front-end electronics provides the possibility to control the bias voltage applied to the SiPM with a low noise DAC. It allows to perform SiPM gain calibration with a signal to noise ratio for single photon signal of ~4. Furthermore, it offers the required linear dynamic range to readout the signal from a 1024-pixel SiPM, of the type used in the hadronic calorimeter prototype for the ILC.

3. MAROC presentation [2]

3.1 Introduction

MAROC is the readout chip designed for the ATLAS luminometer made of Roman pots. This ASIC is an evolution of the OPERA_ROC ASIC developed and installed on the OPERA experiment to auto-trigger and readout 64 channels Hamamatsu multi anode PMTs.

Its main requirements are a 100% trigger rate for signal greater than 1/3 photoelectron, a charge measurement up to 30 photoelectrons with a linearity of 2% or better and a crosstalk less than 1%.

In order to check the functionalities of MAROC, laboratory tests have been performed and have showed a good global behaviour of the chip, which allows using it for beam tests at CERN in summer 2006.

3.2 Description of the asic

The MAROC chip is a 64-channel input front end circuit developed to read out PMTMA outputs. Its main characteristics are the following:

- AMS SiGe 0.35µm technology
- $12mm^2$ (3.5mm × 3.9mm) area
- 3.5V power supply
- 130mW power consumption
- Package: CQFP240

The block diagram of the ASIC is given in *Fig. 11*. For each one of the 64 channels, the PM signal is first amplified thanks to a variable gain preamplifier which has low noise and low input impedance to minimise crosstalk. It allows compensating for the PM gain dispersion up to a factor 4 to an accuracy of 6% with 6 bits.

The amplified current feeds then a slow shaper combined with a Sample and Hold buffer to store the charge in 2pF and provide a multiplexed charge output up to 30 pe^-.

In parallel, trigger outputs are obtained via fast channels made of a fast (15 ns) shaper followed by a discriminator.

The discriminator threshold is set by an internal 10 bit DAC, made of a 4 bits thermometer DAC for coarse tuning and a 6 bits mirror for fine tuning.

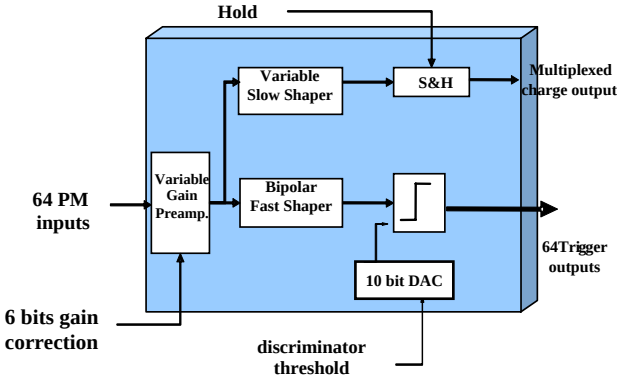

Fig. 11. Block diagram of the ASIC.

3.3 Laboratory tests

Since October 2005, date of the chip delivery, extensive tests have been performed. The first ones have showed substrate coupling between mirror output and preamplifier ground return leading to oscillations for ground inductance > 20 nH when all channels were used at high gain. By mounting the chip on board these effects are reduced and this allows the use of MAROC during beam tests.

The results showed here have been obtained with a chip mounted on the test board developed at LAL.

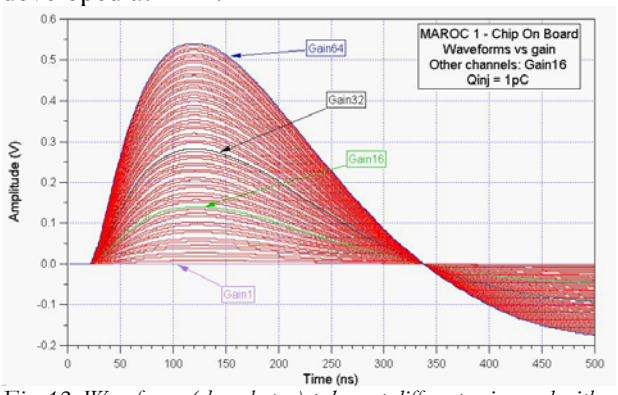

Fig. 12. Waveforms (slow shaper) taken at different gains and with a constant charge injected.

Fig.12 shows slow shaper waveforms obtained for preamplifier gain varying from 0 to 4 (6 bits)[1]. From the maximum of these waveforms a linearity of ± 1% is obtained, in agreement with the requirement.

The trigger functionality also behaves as expected. The *Fig. 13* shows the trigger efficiency as a function of the input charge for the 64 channels set at gain 1. In average the 50 % trigger efficiency is reached at 50 fC which corresponds to 1/3 pe- for a PMT functioning with a gain of 10^6. The noise is of the order of 1 fC.

[1] The gain amplification varies from 0 to 4. It is set via a 6 bits (1 to 64) gain correction level.

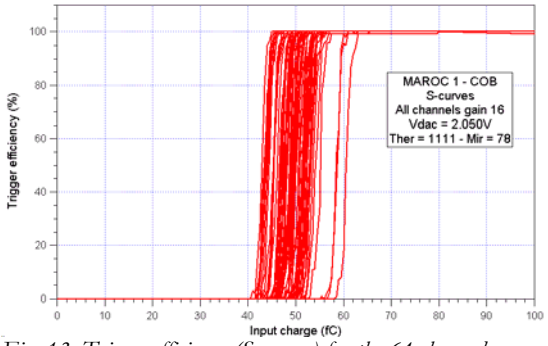

Fig. 13. Trigger efficiency (S-curves) for the 64 channels.

The *Fig.14*, which represents the evolution of the 50% trigger efficiency input charge as a function of the channel number, illustrates the reasonable spread (3.9 fC rms) between channels.

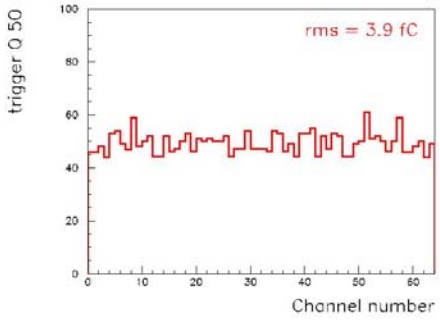

Fig. 14. 50% trigger efficiency input charge as a function of the channel number.

The linearity of the 50% trigger efficiency point with respect to the preamplifier gain has been found better than 5 ‰.

As can be seen in *Fig. 15*, which represents the S-curves for 3 neighbouring channels: the central one is fed with signal up to 10pC, while the neighbours do not trigger up to 8 pC, showing a crosstalk smaller than 1% as required.

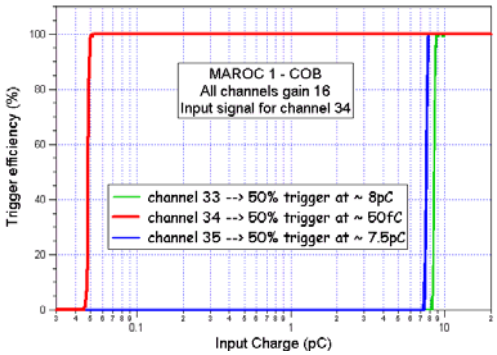

Fig. 15. S-curves for channel 34 and its two direct neighbours, up to an input charge of 10pC.

The pedestal for both fast and slow shapers has a spread of a few mV for the whole chip as illustrated in *Fig. 16*.

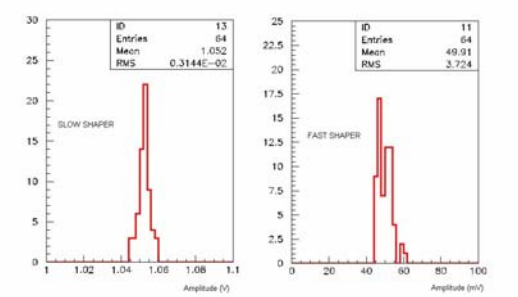

Fig. 16. Pedestal distribution for the 64 channels for the slow shaper (left) and fast shaper (right).

3.4 Conclusion

All the tests performed have showed a satisfying global behaviour of the chip. By using a chip on board, the substrate coupling problem is removed up to gain 2. This will allow the use of MAROC chip during summer and autumn 2006 beam tests, with a reasonably large choice of configurations.

Thanks to the results obtained from the tests of this first version of MAROC a new version (*Fig. 17*) has been developed at LAL and has been submitted in March 2006. The substrate separation applied should solve the coupling problem. Three discriminators are now implemented to have a 2 bit trigger output per channel, which is encoded at 80 MHz. In addition to the functionalities mentioned in the second section a 12 bits Wilkinson ADC has been added per channel on the charge readout path after the track and hold, to deliver directly digitized data.

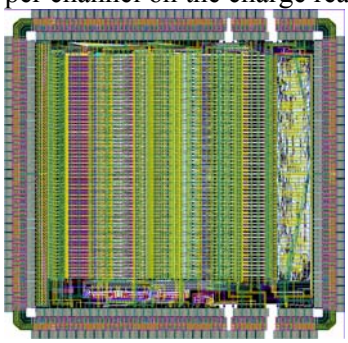

Fig. 17. MAROC 2 layout.

4. HARDROC presentation [3]

4.1 Introduction

HARDROC1 (HAdronic Rpc Detector ReadOut Chip) is the first prototype of the very front end chip designed for the readout of the RPC or GEM foreseen for the Digital HAdronic CALorimeter (DHCAL) of the future International Linear Collider.

The very fine granularity of the ILC hadronic calorimeters (1cm^2 pads) implies a huge number of electronics channels (4 10^5 /m^3) which is a new feature of "imaging" calorimetry.

Moreover, for compactness, the chips must be embedded inside the detector making crucial the reduction of the power consumption to 10 µWatt per channel. This is achieved using power pulsing, made possible by the ILC bunch pattern (1 ms of acquisition data for 199 ms of dead time).

HARDROC readout is a semi-digital readout with two thresholds (2 bits readout) which allows both good tracking and coarse energy measurement, and also integrates on chip data storage.

The 64 channels of the ASIC are made of:

- Fast low impedance preamplifier with 6bits variable gain (tuneable between 0 and 4)
- Variable shaper (50-150ns) and Track and Hold to provide a multiplexed analog charge output up to 10pC.
- Variable gain fast shaper (15ns) followed by two low offset discriminators to autotrig down to10 fC. The thresholds are loaded by two internal 10 bit- DACs.
- A 128 deep digital memory to store the 2*64 discriminator outputs and bunch crossing identification coded over 24 bits counter.

The design and measured performance of the chip will be presented.

4.2 ASIC description

HARDROC is a 64-channel input very front end circuit. Its main features are:

- AMS SiGe 0.35µm technology
- 16mm^2 area
- 3.5V power supply
- 10µW power consumption/channel
- Package: CQFP240

The block diagram of the ASIC is given in *Fig. 18*. Each input signal is first amplified thanks to a variable gain preamplifier which exhibits low noise and low input impedance to minimise crosstalk. It allows accommodating the gain depending of the detector choice, up to a factor 4 to an accuracy of 6% with 6 bits.

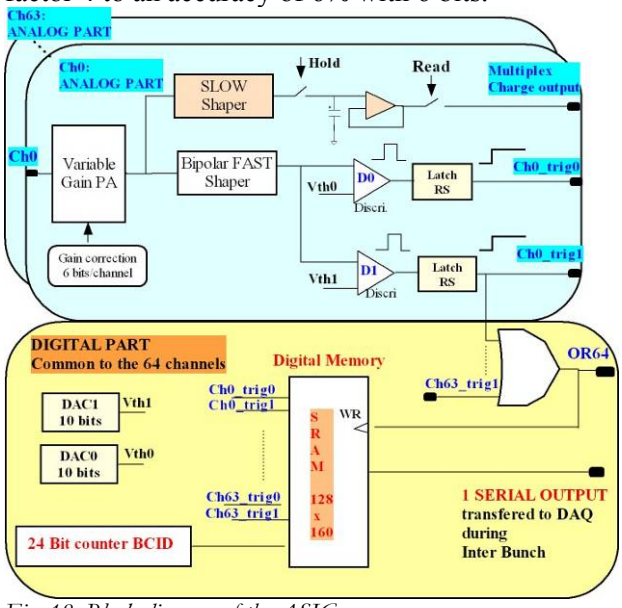

Fig. 18: Block diagram of the ASIC.

The amplified current feeds then a slow shaper combined with a Sample and Hold buffer to store the charge in 2pF and provide a multiplexed charge output (5MHz) up to 10pC.

In parallel, trigger outputs are obtained via fast channels made of a fast (15 ns) shaper followed by 2 low offset discriminators.

The discriminator thresholds are set by two internal 10 bit DACs.

Each trigger output is latched to hold the state of the response until the end of the clock cycle. The trigger1 outputs (corresponding to Vth1 <Vth0) are OR wired to generate an internal trigger used to start the memorization of the 128 trigger outputs as well as the Bunch Crossing Identification delivered by a 24 bit counter, needed to associate hits in the DAQ to bunch crossing ID. It is also possible to capture event data using an external trigger provided from outside the chip.

All the bias currents are programmed through the Slow Control

The chip is power pulsed to decrease the power consumption. 10µV/channel as targeted with a 1% beam duty cycle.

4.3 Testbench Measurements

4.3.1 Analog Part:

HARDROC has been submitted in September 2006 and received mid December 2006.

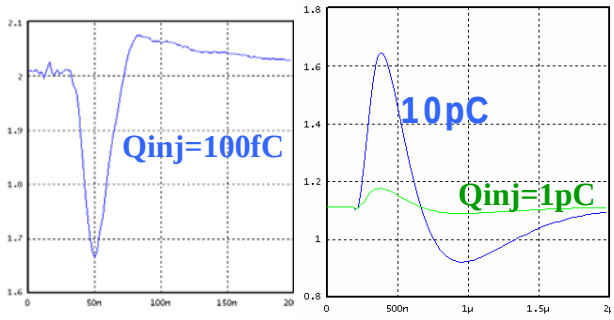

Fig. 19: Waveform of the fast shaper and the slow shaper.

Fig.19 shows slow shaper and fast shaper waveforms. The bipolar fast shaper gain is about 3.5mV/fC and its peaking time is equal to 15ns. The Slow Shaper gain is about 50 mV/pC and its peaking time can be tuned from 100ns to 150ns.

The input impedance of the preamp has been measured to be 50-70 ohms, depending on the (tuneable) current flowing in the preamp.

The crosstalk (*Fig.20*) has been measured by sending 100fC in one channel and looking to the direct neighbours. This 2% crosstalk is well differentiated and located on the input.

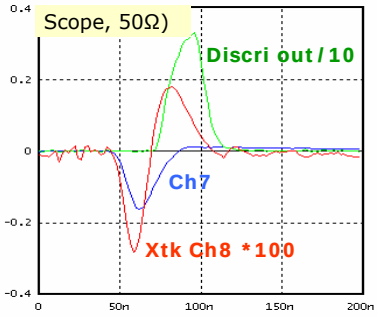

Fig. 20: Crosstalk measurement.

The linearity of the 2 10 bits integrated DACs used to generate the thresholds of the discriminatrors, has been measured: the residuals of the both DACs are within ±5 mV for a 2.6V dynamic range which corresponds to an Integral Non Linearity of 0.2% (2LSB). The slope is 2.5mV per DAC unit.

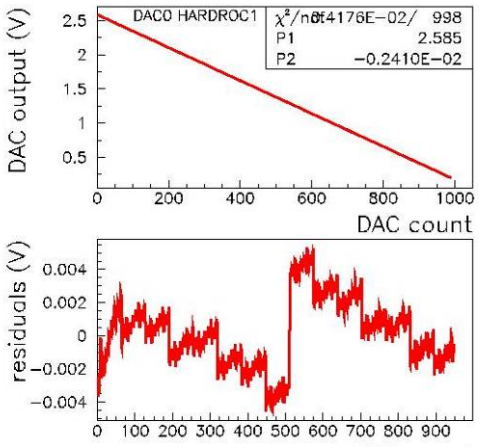

Fig. 21: DAC linearity

The *Fig. 22* represents the s-curve measurement performed on the 64 channels of the chip. The quite large non uniformity between channels (±25 %) is explained by current mirror mismatch (small size transistor to optimize speed) and can be corrected using the gain tuning of the input preamp.

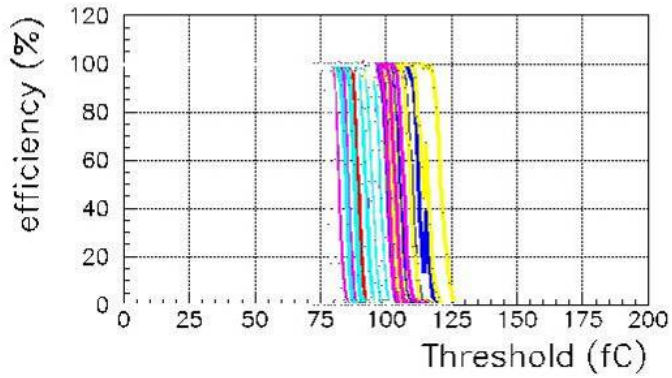

Fig. 22: Trigger efficiency input charge as a function of the channel number.

4.3.2 Digital part:

Because of the very high number of electronic channels foreseen in the final detector, chips will be embedded inside the detector and are designed to be daisy chained without any external circuitry, to limit to a bare minimum the number of output lines on the detector. A memory (*Fig. 23*) has been integrated in HARDROC to store during the bunch train the 2bits trigger outputs of each channel as well as the BCID, and this for every hit.

The data format is 128(depth)*[2 bits * 64 ch + 24 bits (BCID) +8 bits (header)] =20kbits. There is one serial output which is transferred to the DAQ during the interbunch.

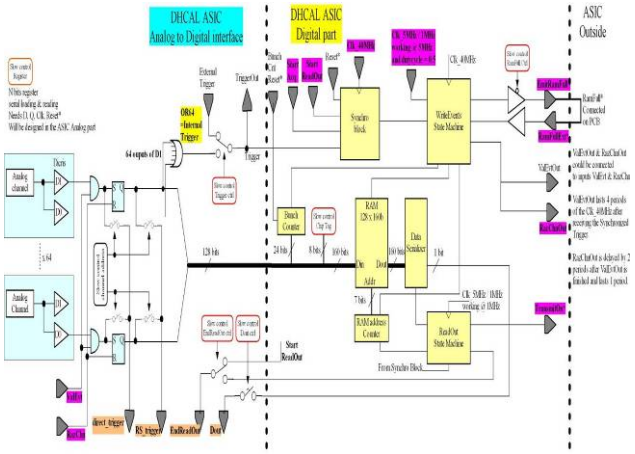

Fig. 23: Digital part of HARDROC

The *Fig. 24* displays a memory frame. The auto trigger mode which is crucial for the chip functionality has been checked successfully down to 10fC.

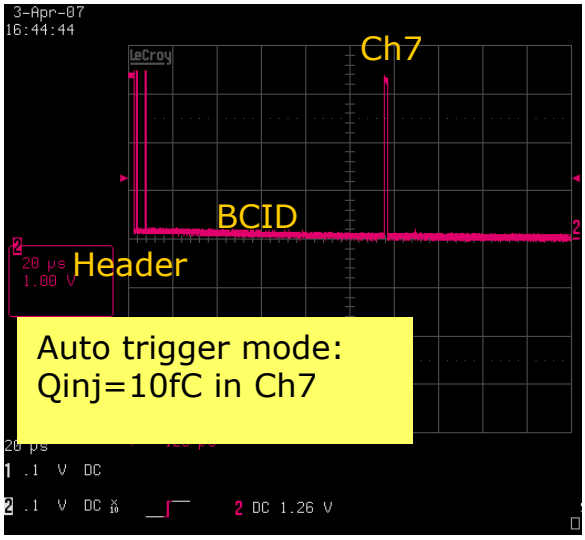

Fig. 24: Memory frame

The trigger crosstalk has been measured (*Fig. 25*) by injecting a charge in one channel (Ch7) and measuring the trigger efficiency on the direct neighbours. There is no crosstalk for injected charge lower than 1.6pC.

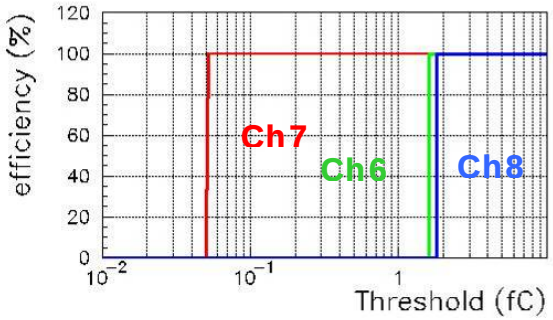

Fig. 25: Trigger crosstalk

A PCB hosting four HARDROC chips (4X64 channels) has also been designed to study the signal connection between the different chips before extracting it through a USB device. The PCB board will be associated to both RPC and µMEGAS detectors in order to validate the whole concept through exposure first to cosmics and then to beam test at CERN.

4.4 Conclusion

All the tests performed have showed a good performance of the chip which allows to mount it on the detector that will go on test beam. HARDROC will allow developing the 2nd generation DAQ of CALICE-EUDET and testing a digital hadronic calorimeter based on RPCs, GEMs or Micromegas.

5. SPIROC presentation

5.1 Introduction

The CALICE collaboration has designed an analogue HCAL prototype using Scintillating fibers read out by SiPM detectors. That 8000-channel physics prototype is currently in test beam at Fermilab. The read-out of that detector is ensured by an analogue front-end chip called FLC_SIPM [1].

A new front-end chip called SPIROC (standing for Silicon PM Integrated Read Out Chip) has been designed to read out the upcoming technological demonstrator foreseen in 2009.

5.2 SPIROC description

SPIROC has been designed to read out SiPM or MPPC through an ILC beam structure involving a sequence of operation mode as following:

- Acquisition mode: where the charges and the hit time are memorized in the analogue memory each time the chip triggers.
- Conversion mode: where the data are converted from the analogue memory into digital through ADCs. The data are then formatted and stacked up in a digital memory.
- Data transfer: where the formatted event (ie charges measurements and associated triggering time) are outputted to the data acquisition system.
- Idle mode: where the chip consumption is reduced by a factor greater than 1000 to wait for the next machine train

These entire operation modes are fully automatic.

SPIROC main characteristics are the following:

- AMS SiGe 0.35µm technology
- 30mm² (4mm × 7.5mm) area
- 3.3V power supply
- Package: CQFP240
- Internal input 8-bit DAC (0-5V) for SiPM gain adjustment
- Energy measurement :
  - 2 gains / 12 bit ADC 1 pe → 2000 pe
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11
- Time measurement :
  - 1 TDC (12 bits) step~100 ps
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~15ns

  - Auto-Trigger on ½ pe
- Analog memory for time and charge measurement : depth 16
- Power pulsing integrated
- Low consumption : ~25µW per channel (in power pulsing mode)
- Calibration injection capacitance
- Embedded bandgap for voltage references
- Embedded DAC for trigger threshold
- 12-bit Bunch Crossing ID
- SRAM with data formatting : 4 Kbytes
- Output & control with daisy-chain

The SPIROC chip will be send to foundry on June 2007. The layout at the abstract writing time is shown on *Fig 26*.

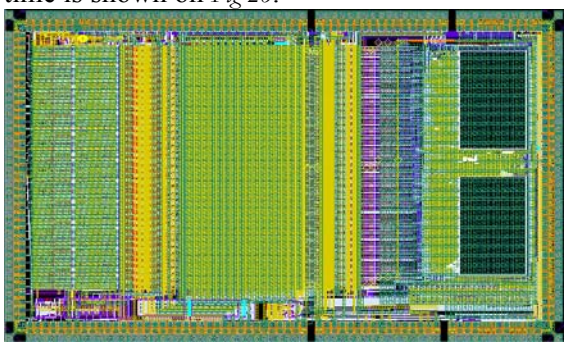

Fig 26 – SPIROC layout

The analogue core is composed of 36 channels embedding an input DAC for SiPM high voltage adjustment on 5V to tune gain channel by channel. Two preamplifiers allow the requested dynamic range and are followed by a trigger line made of a fast shaper and a discriminator. The charge measurement line is made of two variable slow shapers and two 16-depht SCAs. The block scheme of a channel is shown on *Fig 27*.

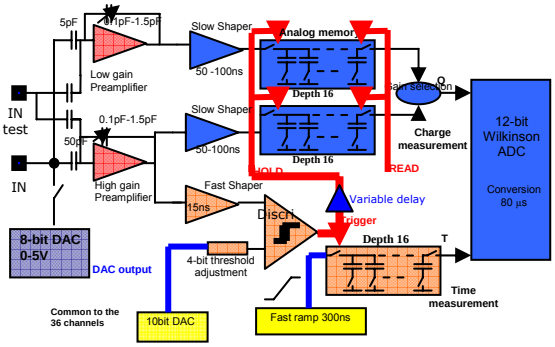

Fig 27 – One channel block scheme

The analogue core is an evolution of the FLC_SIPM 18-channel chip designed for the SiPM-Sci AHCAL physics prototype.

5.3 FLC_SIPM meas. and SPIROC sim.

The Results of the FLC_SIPM chip on the single photon counting has shown very good results shown on *Fig 28*.

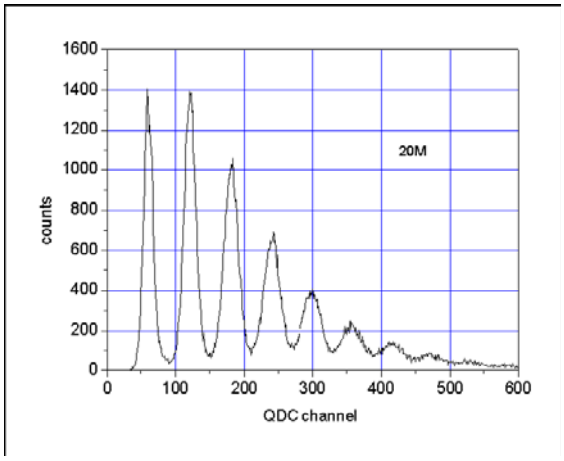

Fig 28 – Single photoelectron spectrum made with FLC_SIPM

The FLC_SIPM range is able to measure the single photoelectron for absolute calibration and can read a maximum input signal of more than 1000 photoelectrons by using two different modes involving complex range calibration.

The new analogue chain in SPIROC allows the SPE calibration and the signal measurement to be on the same range, simplifying greatly the absolute calibration.

An analogue simulation of a whole analogue channel is shown in *Fig 29*.

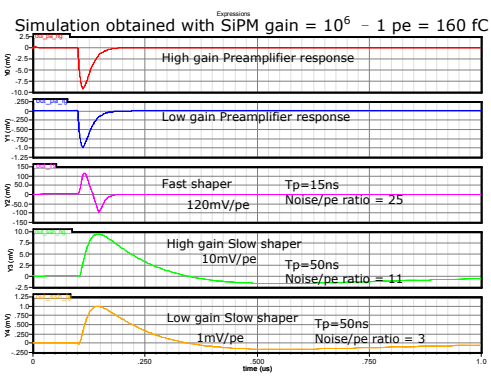

Fig 29 – SPIROC Analogue Simulation

The ADC used in SPIROC has been tested on a functional block before being integrated in the whole system. Integral non linearity of the 12-bit Wilkinson ADC is shown in *Fig 30*. The measurement shows a 11.5 ENOB (Equivalent Number of Bit) fulfilling requirements.

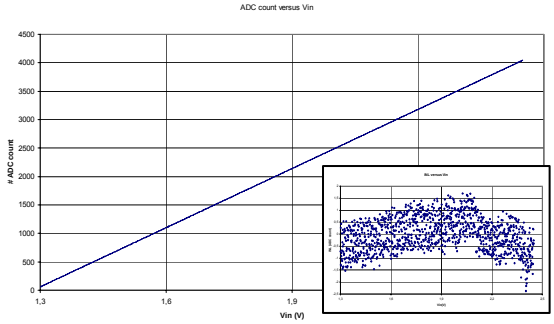

Fig 30 – 12 bit Wilkinson ADC INL meas. result

5.4 Conclusion

The SPIROC chip will be submitted in June 07 and will be tested in September 07. It embeds cutting edge features that fulfil ILC final detector requirements including ultra low power consumption and extensive integration.

The system on chip is driven by a complex state machine ensuring the ADC, TDC and memories control.

The SPIROC chip is due to equip a 10,000-channel demonstrator in 2009.

6. Acknowledgment

That paper is a description of several ASICs. It reuses existing papers for each chip description (cf references). I would like to thank the authors of these papers:

Erika Garutti for the FLC_SiPM description, Pierre Barrillon for the MAROC description, Nathalie Seguin for the Hardroc description and Ludovic Raux for the SPIROC description.

References

[1] E. Garutti (DESY) & Al, *Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM readout,* LC-DET-2006

[2] P. Barrillon (OMEGA) & Al, *Multi-Anode Readout Chip for MaPMTs,* IEEE NSS 2006, abstract.

[3] N. Seguin (OMEGA) & Al, *HARDROC1, Readout chip of the Digital Hadronic Calorimeter of ILC*, IEEE NSS 2007, abstract.

[4] L. Raux (OMEGA)& Al, *Spiroc and FLC_SiPM : Silicon Photomultiplier Read Out Chips for ILC*, IEEE NSS 2007, abstract.