PROCEEDINGS OF SCIENCE

Hybridization Issues for Future Applications

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After a short illustration of the demands of two future applications in the area of pixel detectors, namely the upgrade of the large hadron collider and the international linear collider, this article adresses the most basic interconnection problems occuring in building those devices. Selected technologies are reviewed for the connection of the sensor to the read out chip and the interconnection of the chips on a detector module. At the end of the article a summary is given.

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1. Introduction

Future applications for pixel detectors such as the upgrade of the Large Hadron Collider (SLHC[1]) or the international Linear Collider (ILC[2]) put strong demands on the devices to be used there. Common to both applications is the need for high granularity and low power consumption. In the SLHC case the emphasis also lies on the extrem radiation hardness of the devices, which is not such an issue for ILC pixel detectors, that aim for minimal material budget of the tracking devices. In both cases the detector systems will be assembled from small building blocks, the individual detector modules.

A typical detector module as seen in fig.1 has three levels of hybridisation:

- sensor to readout chips (ROCs)
- interconnection of ROCs on the module
- connection of the module to electrical infrastructure and cooling

In the following sections selected techniques for the first two items will be discussed.

2. Interconnection ROC-Sensor

The first connection in the signal chain is the one between the sensor and the front-end chips. It can be characterised as follows:

- high number of interconnections per area ($10*10^3$ /cm^2)
- low connection pitch increasing from the inner radii of a detector to the outer ones ($\sim$50 - 200 μm)
- low capacitance of the connection, to keep the noise and powerconsumption in the analog part low
- moderate resistance ($\sim$ few ohms)

Those connections can routienly be created by various techniques ranging from simple solder masks to SIO waferbonding.

The next subsections deal with some of those methods:

- flip-chip:
  - fine pich bumpbonding
  - C4NP - process
- other:
  - SIO waferbonding

2.1 Fine - Pich Bumpbonding

Common to all fine pitch flip-chip processes are simmilar processing steps to create a surface both on the sensor and the ROC part, that is compatible and wetable with the choosen bump material (see fig. 2):

After cleaning and photoresistive structuring of both bonding surfaces the so called Under Bump Metal (UBM) is deposited by means of electroplating, sputtering or evaporation. On top of this UBM the bump material is deposited in a similar way on one or both bump surfaces with an additional photolithographic step if needed. The ROC wafers are then thinned if desired and diced. Depending on the process an additional reflowing step has to be done on one or both bump-partners. Pictures of resulting bumps in different materials are shown in fig.3.

After this the flip chip can be done followed by another reflowing step of the bumpbonded device if needed by the process choosen.

Fine pitch bumpbonding features the following:

- minimum pitch of $\sim$20 μm
- low temperature process: normally $\sim$200-300 °C depending on alloy used. Without reflow temperatures as low as 50 °C are possible[3]
- almost free choice of sensor-material and chip-technology
- use of Known Good Devices (KGD) is possible
- yield of good devices is about 90 %
- bump yield on those devices is $\sim$99.9 %
- timeconsuming dice based process
- cost: $\sim$300 CHF/cm^2

2.2 C4NP - 'low cost' Bumpbonding

In the C4NP[4] process the bump material is filled in a special mold and subsequently transfered to one bump-surface (see fig. 4), normally the chip wafer. The mold can than be reused again several times. The preparation of the two bumpsurfaces with an appropriate UBM and the flip chip is done in a similar way as in the fine pitch case.

With this method bump pitches of $\sim$200 μm can routienly be done at prices of about 300 CHF/wafer(6 inch). Pitches down to 50 μm have been achieved. The cost of the process is highly dominated by tooling costs, and varies with the lot size and the number of cycles that can be done with one mold. The process can make use of KGD.

2.3 SIO Waferbonding

In contrast to the flip chip technologies described above the SIO wafer bonding process[5] works on whole sensor- and readout wafers at a time.

The process steps are the following (see fig. 5):

- first an oxide layer is created on the bondingsurface of the two wafers with different resistivity
- then the SIO bonding of the wafers is done by pressing the wafers against each other at $\sim$500 °C
- after that the low resistivity wafer, the later CMOS side, is thinned down to $\sim$10 μm
- then both wafers are processed to form the front end electronics and the sensor part of the device
- finally the vias are formed for the interconnection of sensor and electronics (see fig. 6)

The very appealing feature of having a monolythic device with electronics on SOI is paid by the fact that KGD is not possible in this process. In addition to that the choice of material especially for the sensor is quite limited.

3. Interconnection ROC-Periphery

To form a working detector module the ROCs have to be supplied with power and controll signals. The output of the ROCs on the other hand has to be collected and transmitted in a reasonable fashion to the next step of the data aquisition. This is normally done by a separate layer of interconnection lines mostly in conjunction with a specialised module controller chip placed on top of the module.

Two examples for this module interconnection are shown:

- flex hybrid
- MCM-D

3.1 Flex-Hybrid

A widely used solution for the interconnection of the ROCs to the periphery is the so called 'flex hybrid' (see fig. 7). It consists of several layers of metallisation interleaved with insulating layers of polyemid. The metallisation layers are connected with laser drilled vias where needed and can have a pitch of $\sim$80-150 μm. Typical metallisations are made from copper but very specialised processes exist that rely on aluminum to reduce the material budget of the flex[6]. Additional components such as a module controller chip, optical transceivers and passive components can be soldered or glued and wirebonded on top of the flex easiely. The hybrid is then glued on top of the module an the connection to the ROCs is done with wirebonds. The yield of such a hybrid reaches $\sim$90 % and the cost is $\sim$30 CHF/cm^2.

3.2 MCM-D

An other approach to do the module interconnection is followed by the MCM-D[7] technique. Additional metalisation layers are processed on the bump surface of the sensor that serve as power- and signal-lines for the readout chips. Vias connect the metall lines where needed. The chips are

connected to those extra metallisations and the sensor with bump bonds only, so no wirebonds are needed. The connection between the individual pixel cells on the ROC and the sensor is done with staggered vias as seen in fig. 8 without affecting the module performance.

The MCM-D technique gives the opportunity to optimise the geometry of the sensor pixels independent of the layout of the readout chip. Additional components and the connection cables are bumpbonded to the sensor too, that is there for bigger than the sensitive area of the device (see fig. 9).

The MCM-D technique offers several possibillities to optimise the module design and gives in return an almost monolythic module without fragile wirebonds. On the other hand the material budget is not smaller than a flex solution and the additional photolithographic steps on the sensor wafers are more expensive than a traditional flex hybrid.

4. Summary

We have given a overview on selected current technologies concerning module hybridisation. All processes given are suitable for SLHC and ILC applications. The choice of the technology depends highly on the exact demands of the application: bumpboonding has the advantage of matureness and medium cost for the fine pitch part. For not so fine pich the cost could even be reduced with the use of C4NP but only for not so small series to split the tooling costs among a larger number of devices. When the availiable sensor material meets the demands and the device yield is reasonable high, the monolythic and thin devices resulting from SIO waferbonding are also a good choice. Especially if material budget and easy handling is an issue. For the module interconnection part the flex hybrid is for sure a cheap and mature solution but it adds an additional component to the module. The handling of the assembled module needs special caution because of the significant number of wirebonds needed for the connection to the ROCs and the module controller chip. The MCM-D approach goes one step further to create a monolythic device but cost and complexity of the process are higher than for a flex print.

References

[1] The CMS Upgrade Project. CMS Expression of Interest in the SLHC. CERN/LHCC 2007-014.

[2] ILC-Report-2007-001, CERN-2007-006

[3] The ATLAS Pixel Collaboration. Study of indium bumps for the ATLAS pixel detector, Nuclear Instruments and Methods in Physics Research A 465 (2001) 200-203.

[4] C4NP (Controlled Collapse Chip Connection New Process) IBM/SUSS Microtec AG.

[5] Current Status and Future Perspectives of Wafer Bonding SOI Technology, Electronic Journal, Dec 15, 2004, p82

[6] ITS Technical Design report, CERN-LHCC 99ï£¡12, 1999.

[7] Pixel detector modules using MCM-D technology, Nuclear Instruments and Methods in Physics Research A 465 (2001) 211ï£¡218.

[8] Ch. Brönnimann et al. Development of an Indium Bump Bond Process for Silicon Pixel Detectors at PSI. These proceedings.

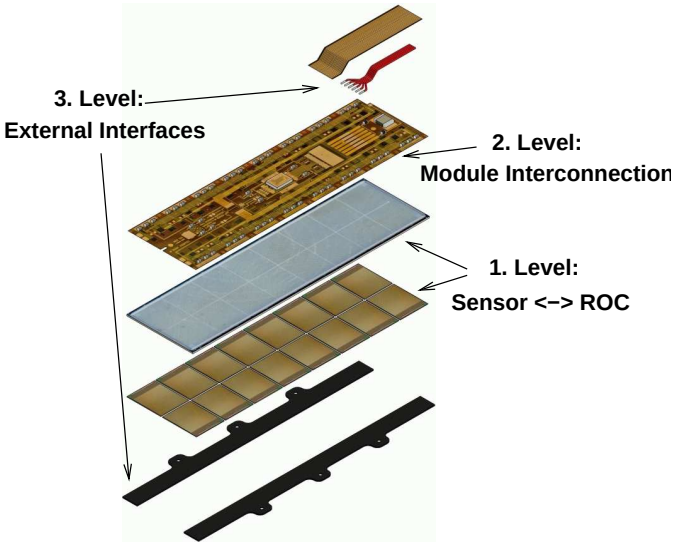

Figure 1: Three levels of hybridisation shown at the example of a CMS pixel detector module

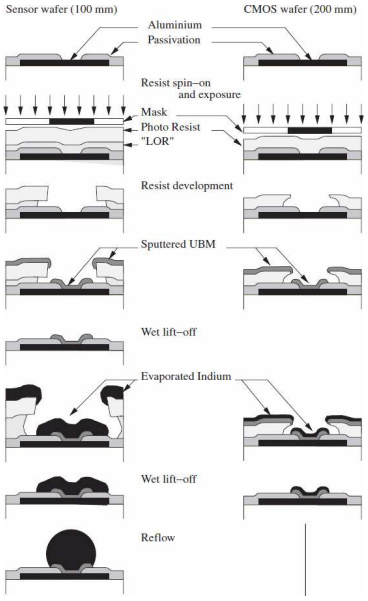

Figure 2: Workfbw of the CMS pixel indium process[8]

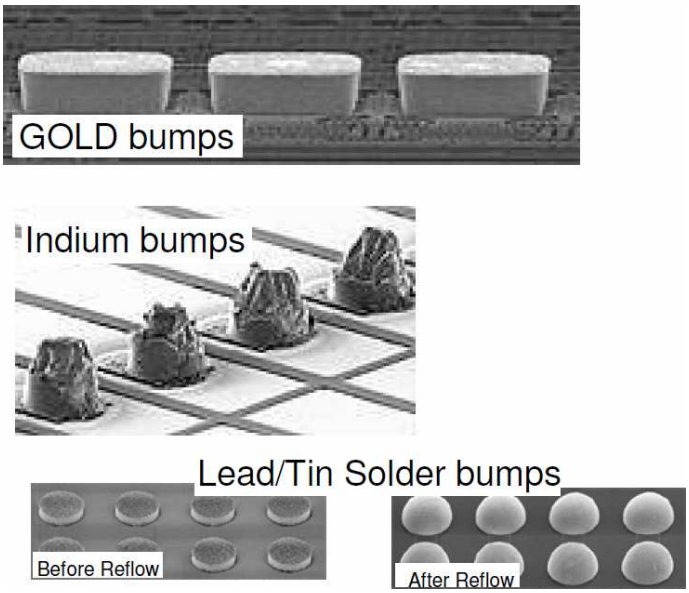

Figure 3: Pictures of bumps of various materials

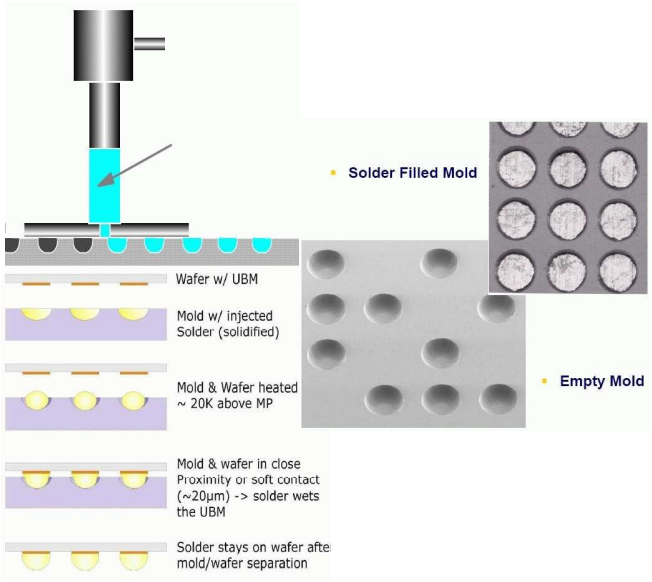

Figure 4: mold fi lling and bumptransfer in the C4NP process

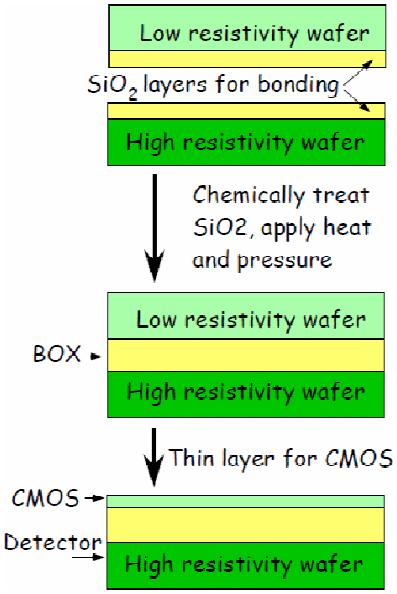

Figure 5: scema of the SIO wafer bonding process

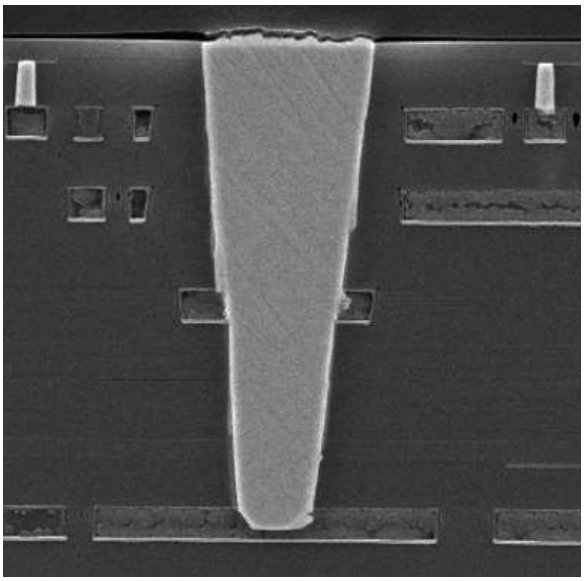

Figure 6: crossection picture of an eched via through a thinned CMOS chip

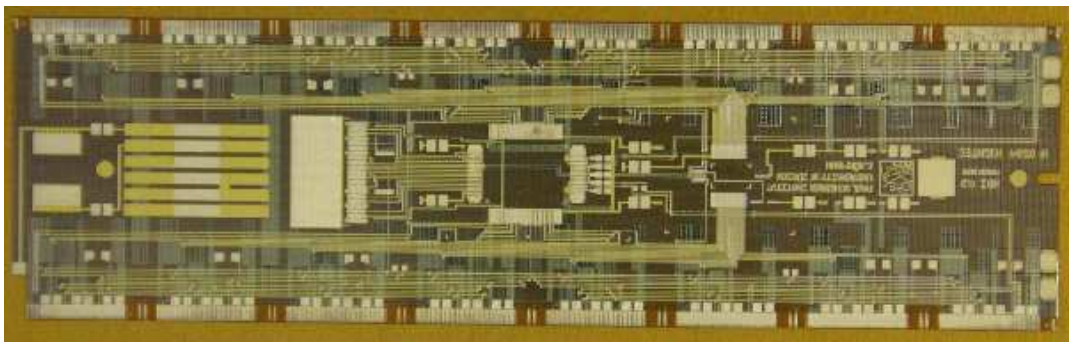

Figure 7: picture of the flex hybrid of the CMS pixel barrel modules

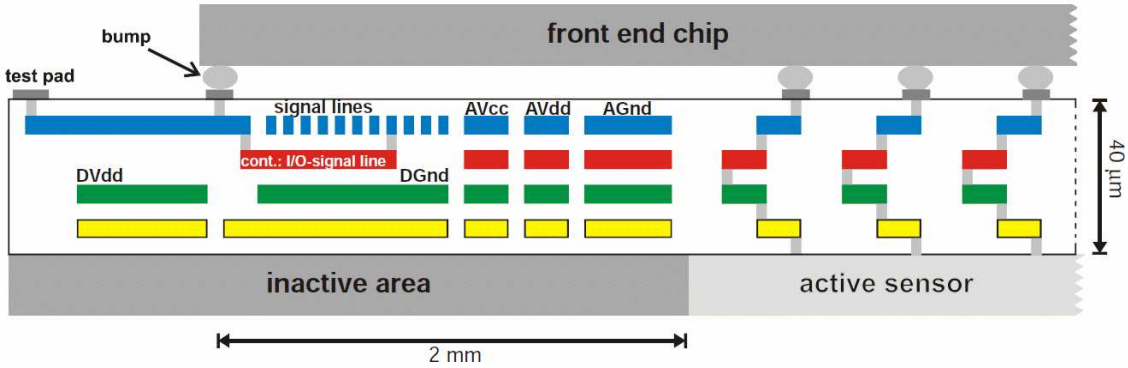

Figure 8: crosssection of a MCM-D module

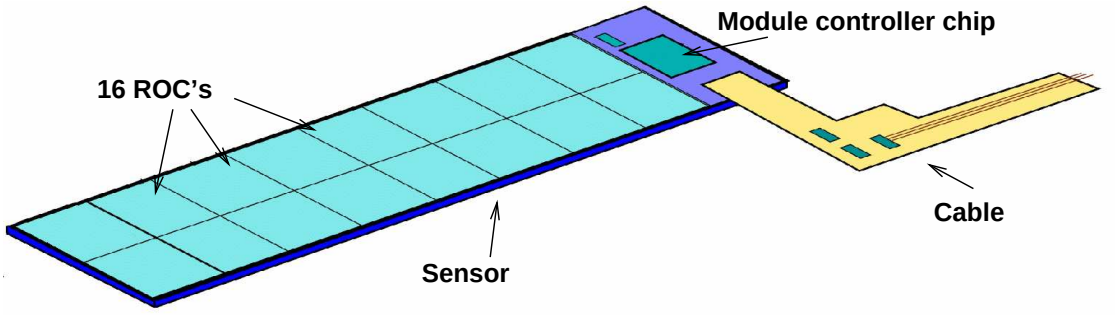

Figure 9: drawing of a MCM-D module with 16 chips