PROCEEDINGS OF SCIENCE

Thinned Silicon Detectors

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Silicon sensors used in tracking or vertexing detectors in particle physics are usually made with silicon wafers of 280 μm to 500 μm thickness. In order to reduce multiple scattering much thinner detectors would be desirable. Another motivation for thin detectors might arise from the need to operate detectors after severe radiation damage when charge carrier drift is limited by trapping. Since thin silicon wafers are difficult to handle fabrication of such sensors is challenging. This article describes a method to produce thin sensors using SOI wafers.

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1. Introduction

For many applications the sensor thickness is an important parameter. Thick fully depleted detectors are needed for x-ray detections (higher efficiency) and optical sensors for the near infrared (long absorption length). For tracking detectors the thickness should be minimized in order to reduce multiple scattering. However, thinning reduces the signal size, so there is a lower limit given by the minimal signal to noise ratio required to operate the detector. This is especially the case in large area detectors like strip and pad detectors or photodiodes where the large capacitance causes substantial noise. For pixel detectors with small pixel size and therefore low capacitance the noise is usually very small, a few 100 electrons, and detector thicknesses below 100 μm should be possible. As explained in section 2 thin detectors may offer advantages, like low leakage currents and operation voltage, for highly irradiated detectors.

2. Motivation for thin detectors

The detector thickness d controls several parameters of a sensor:

- Signal of a minimum ionising particle: A minimum ionising particle generates about 80 electron-hole pairs per μm silicon. Of course the detector has to be depleted in order to collect signal charges efficiently and the charge carriers must be able to drift through the depleted volume without being trapped.

- Detector capacitance: This is an important parameter for the noise of the signal amplifier. The noise contribution from the input FET channel noise is proportional to the total capacitance C. In parallel plate geometries the capacitance of a silicon diode is given by $C = \varepsilon \frac{A}{d}$ (A: area, $\varepsilon \approx$ 1pF/cm). Hence thicker detectors have lower capacitance and therefore less noise. However, in strip detectors the capacitance to the neighboring strips adds significantly to this and in pixel detectors with small pixel size (pitch $<$ thickness) the total capacitance is actually dominated by the capacitance to the neighbours.

- Leakage current: highly radiation damaged detectors have substantial leakage currents. These currents can cause shot noise and even (together with high depletion voltages) self heating of the sensor.

- Depletion voltage: the depletion voltage is $U = \frac{epd^2}{2\varepsilon}$ (e: electron charge, p: doping concentration). Again, heavily radiation damaged detectors have a large effective doping concentration leading to high depletion voltage, about 500V for a 300μm thick detector at $3 \times 10^{14} n/cm^2$ (1 MeV neutron equivalent) flux after reverse annealing [1]. Because of the square dependence the depletion voltage can be reduced very efficiently by thinning.

- Radiation length: The radiation length of silicon is 9.26cm. Hence a 300μm thick detector has already 0.3%X_0. For a particle of 1 GeV this introduces a impact parameter error of 10 μm at an extrapolation distance of 1.5cm, which is about the intrinsic position resolution of a fine pitch (25μm) detector!

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The minimum signal size which can be reliably detected is given by the noise of the readout electronics, which depends on many parameters, like detector capacitance, shaping time (bandwidth) and current (power) of the input transistor. Strip detectors with long strips (O(10cm)) have substantial capacitances and, together with the short shaping times needed (25ns at LHC), typical noise values are 1000 electrons and higher. Assuming a minimal acceptable signal to noise of 10:1 the detector needs to be $125\mu m$ thick which actually should be doubled to account for charge sharing. Pixel detectors have a much lower noise, less than 300 electrons [2], here a detector thickness of 100 μm could be possible. More advanced detectors like DEPFET [3] can achieve noise levels below 100 electrons, allowing a detector thickness as low as $50\mu m$.

Such thin detectors are actually required for high precision vertex detectors as needed at a future linear collider (ILC) [4]. Here the impact parameter resolution aimed is:

$$\sigma(IP_{r-\phi}) = 5\mu m \oplus \frac{10\mu m}{p \cdot \sin^{3/2}\theta},$$

where p and θ are particle momentum and polar angle, respectively. This requires less than $0.1\% X_0$ per detector layer which corresponds to about $100\mu m$ of silicon. Since any detector module has additional material besides silicon (carrier, electronics, interconnection material) the silicon thickness has to be much less, $50\mu m$ is probably realistic.

Another motivation for thin detectors could come from the need to operate silicon detectors at radiation doses of up to $10^{16} n/cm^2$ (1 MeV neutron eq.) at sLHC [5]. Besides the well known effects of increasing leakage currents and depletion voltages (exceeding 1000V for conventional detectors at this dose) a new problem arises due to trapping [6]. The inverse trapping time depends on the fluence Φ like:

$$\frac{1}{\tau_{e,h}} = \beta_{e,h}\Phi \tag{2.1}$$

β depends on annealing time and temperature. β is slightly different for electrons ($\beta_e \approx 4 \times 10^{-16} cm^2/ns$) and holes ($\beta_h \approx 5 \times 10^{-16} cm^2/ns$). At a fluence of $10^{15} n/cm^2$ the trapping time of electrons is $2.5ns$, if the electrons drift at the maximal (=saturation) velocity the effective drift length is $l_{trap} = 250\mu m$. Therefore in detectors of standard thickness (250 - 300μm) trapping becomes significant at doses above $10^{15} n/cm^2$, when the average drift length is reduced below the thickness of the detector. At $10^{16} p/cm^2$ the drift length is only $25\mu m$, so the charge collection efficiency of a $300\mu m$ detector drops to about 10%. A detector of $50\mu m$ thickness would give the same signal than a thick detector but at much lower depletion voltage and leakage current [7]. Clearly a thick detector could be operated at lower voltage, partially depleted such that the depleted depth matches the drift distance. Still thin detectors could have better performance, since at the same depleted thickness a thin, over-depleted detector reaches higher electric fields (and therefore high drift velocities and collection efficiencies) than a partially depleted thick detector operated at the same voltage. In addition the thick detector would have a larger depleted volume, resulting in higher leakage currents but not contributing significantly to the signal. Albeit, these advantages of thin detectors have a price: the signal is small already un-irradiated and the thickness has to be well matched to the dose expected at the end of the detector life.

There are more motivations for thin silicon which may not relevant for tracking detectors, but they may push the development of affordable thinning technologies:

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- Back-illuminated optical detectors should be thin either to remove all un-depleted bulk material which would be a parasitic absorber and/or to reduce depletion voltage and leakage currents which add to the noise. Back-illuminated optical CCDs are usually thinned.
- Industry pushes thinned devices, e.g. to produce flexible electronics to be used in smart cards or as basis for vertical integration technologies employing vias etched through thin silicon chips.

3. Thinning

A straightforward possibility is to process thin wafers. Standard wafer thicknesses are $300\mu m$ (4 inch wafers) to $500\mu m$ (6 inch wafers). Industry can actually deliver wafers which are much thinner ($10\mu m$) but the processing of such wafers is highly non-standard. Thin wafers become fragile and the risk of breakage during processing and handling becomes high. Nevertheless wafers as thin as $150\mu m$ have been processed successfully [8]. Of course the wafers had to be handled with great care. However, from our experience with some manufacturers, the limit for large scale production is probably $250\mu m$ (4 inch) and $300\mu m$ (6 inch).

Another possibility is the back-thinning of processed wafers. For ASIC electronics thinning to $50\mu m$ and below is already standard in industry. Usually the processed wafer is thinned by grinding and etching the unprocessed backside before the chips are tested and cut. It is also possible to thin single chips. Clearly the handling of the thin chips is more delicate and especially if intended for bump bonding some restrictions may apply. This method can be used for MAPS [9] detectors and CCDs where the signal is generated in a thin epitaxial layer and the bulk remains un-depleted. But for most of the detector types based on fully depleted substrates this method cannot be applied. In these detectors the backside needs an implantation, sometimes homogenous, sometimes even structured like for the n-in-n pixel sensors used in ATLAS and CMS. A backside ion implantation with a subsequent annealing step or a doping by diffusion needs high temperature processing steps which are incompatible with the already processed front side. A way out is laser annealing [10]. Here the annealing after ion implantation is done locally with a laser avoiding heating up of the front side. However, this method is time consuming, not yet available everywhere and therefore only suited for small series.

A third possibility is to etch small, thin windows in normal wafers [11, 12]. The detector structures are then built on these thinned windows. If these thinned regions do not cover too a large area of the wafer it can be processed rather conventionally. However, this becomes difficult for large area detectors. Another problem is the control of the thickness and the uniformity of the etched regions. If possible an etch stop should be used: a layer which is not dissolved by the chemicals and stops the etching process. This could be a highly doped deep implant, a highly doped epitaxial layer or the buried oxide of a SOI wafer [13]. Especially the use of SOI wafers allows a variant of this technique, developed at the MPI semiconductor laboratory [14], which could be used to process large area thinned devices. SOI wafers (**S**ilicon **O**n **I**nsulator) are made bonding two wafers together. This process is illustrated in figure 1.

The surfaces to be bonded are covered by oxide and these oxide layers are fused together applying high temperature using a technique described in [15]. It is possible to preprocess these

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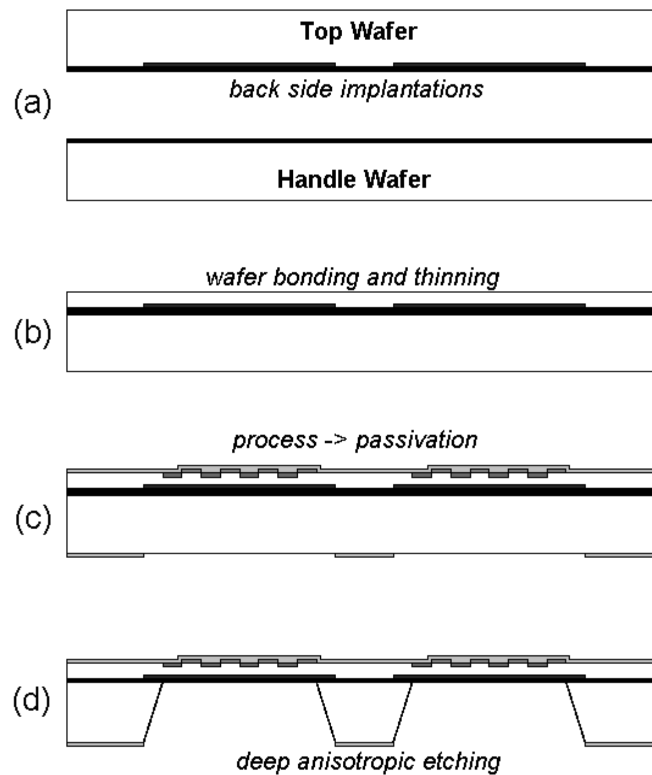

Figure 1: *Thinning of double sided processed detectors. a) The detector wafer, already after backside implantation, is bonded to a handle wafer. b) The detector wafer of the SOI stack is thinned. c) This stack can now be processed in a normal single sided production line. d) Finally the backside passivation of the handle wafer is removed at selected areas and the wafer etched away. The SiO_2 layer at the SOI interface acts as etch stop.*

wafers, allowing for a structured backside implantation. The top wafer is then thinned to the desired thickness using conventional wafer grinding and polishing. The thermal and mechanical stability of such a stack is almost like that of a conventional wafer and all subsequent processing steps can be done using standard equipment. Actually the handel wafer perfectly protects the backside, so no additional protection measures are needed during processing. At the end of the top side processing the wafer is passivated, except for the aluminum contacts. The back side passivation is then opened wherever desired and the handle wafer is selectively etched back. The etching is done using tetramethyl ammonium hydroxide (TMAH). TMAH has a high etch rate for silicon but does not remove SiO_2 and Si_3N_4, the commonly used passivation layers. The etch process stops when the handle wafer is etched through and the etch solution hits the buried oxide layer. If the backside needs to be contacted two more steps are needed: contact opening of the buried oxide and metallization. A nice feature of this technique is the possibility to keep parts of the thick handle wafer at the original thickness in order to form frames or other structures ensuring mechanical stability. Otherwise such thin detectors, especially for thicknesses of 50 μm and below, need to be glued on special carriers. The backside of a 150mm wafer with sample structures for ILC is shown in Fig. 2. The large structures have an area of $(13 \times 100) mm^2$. The thinned areas have a thickness

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of $50\mu m$. An example of such a thinned detector sample with a handling frame after cutting is shown in figure 3. In order to reduce material further even the handling frame can be patterned as shown in Fig. 4 keeping almost the same mechanical strength. The regular pattern is formed due to the different etch rates of TMAH for the 100 and 111 planes.

The mechanical stability of the 10 cm long module was measured at Fermilab. The deflection under gravity was only $20\mu m$ [16].

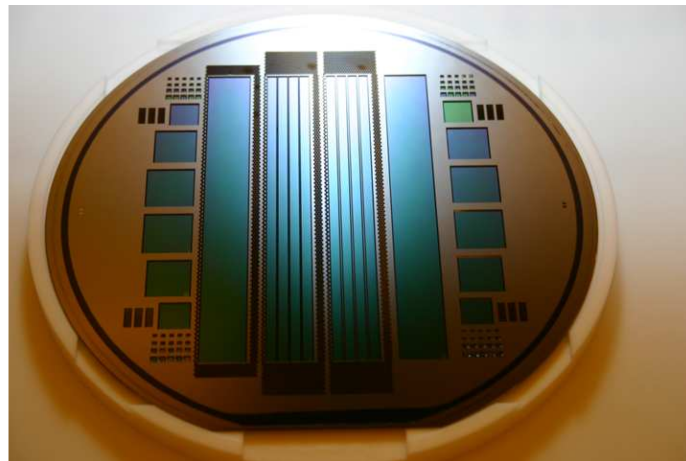

Figure 2: *Photograph of the backside of a 6" SOI wafer with areas thinned to 50µm. The large areas in the center correspond to ILC like modules,* $(10cm \times 1.3cm)$*, with and without reinforcement strips. The small structures in the periphery are test diodes.*

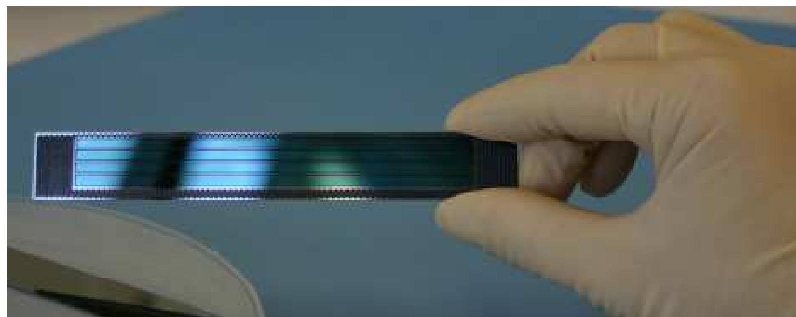

Figure 3: *Mechanical sample of an ILC sensor. The inner area is thinned to 50µm. The sensor (area 10cm × 1.3cm) is supported by a frame of 450µm thick silicon. This frame provides mechanical rigidness and support for ASIC chips. The width of the frame along the module is 1mm and 3mm respectively. Despite the thin sensor area the structure can still be handled manually.*

4. Electrical Measurements

Besides the mechanical samples mentioned above thinned test diodes were produced using this technique. A cross section of those diodes is shown if Fig. 5. The CV behaviour and the leakage currents of such $10mm^2$ diodes are shown in Fig. 6. The depletion voltage is 50V corresponding to a thickness of $49\mu m$ for the material used. The leakage currents at full depletion are about

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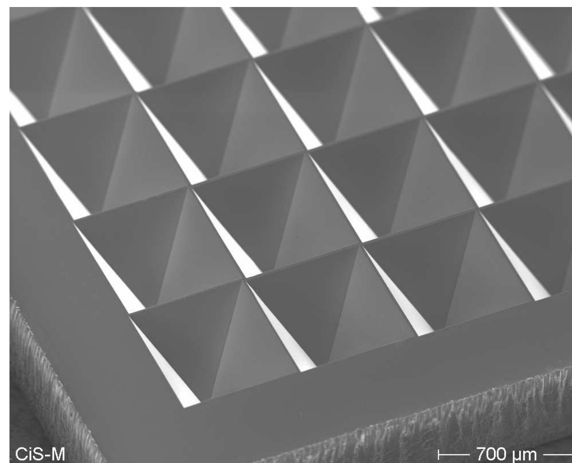

Figure 4: *Photograph of a pattern etched into the handling frame to reduce material. The dimension (length) of a cube is 650μm*

$100 pA/cm^2$, no deterioration of the currents could be observed due to the thinning and etching procedure.

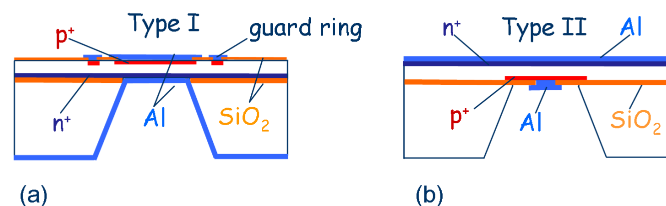

Figure 5: *Layout of tinned test diodes. Type I has a large area ohmic contact at the back side. Type II has a structured back side. The data shown in the article are measured using type I devices.*

5. Irradiations

Some of the thinned diodes were irradiated with protons up to $10^{16} p/cm^2$ [17]. The depletion voltage at this dose after short term annealing was still below 100V. The change of the doping concentration occurred at the reduced rate typical for oxygen enriched material, apparently the high temperature bonding process enriches the detector wafer with oxygen. Charge collection efficiency at $10^{16} p/cm^2$ was 66% corresponding to a collected signal charge of 2600 e- (most probable value).

6. Conclusions

Thin silicon detectors are needed for precision vertex detectors in future experiments like ILC. They might also offer a way to build detectors which can be operated after very high irradiations with low operation voltage and leakage current still giving a small but acceptable signal. A thinning procedure based on SOI wafer bonding has been developed at the MPI Semiconductor laboratory which allows to build large area fully depleted silicon sensors of arbitrary thickness. Prototype samples and diodes show excellent mechanical and electrical properties. As next steps we will

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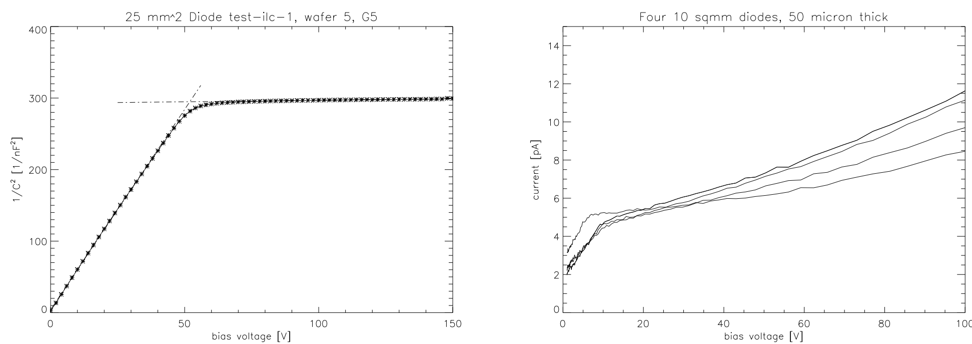

Figure 6: *Electrical properties of thinned test diodes. Left:* $1/C^2$ *as function of the bias voltage. Right: leakage currents of four diodes.*

produce real sensors for sLHC radiation tests (ini-strips, pixel sensors matching the ATLAS FEI3 chip [2]) and thin DEPFET sensors as prototypes for an ILC vertex detector.

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