OF SCIENCE

Monolithic Active Pixel Sensors at Saclay

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In close collaboration with the group from Strasbourg, Saclay has been developing fast monolithic active pixel sensors for future vertex detectors. This presentation gives some recent results from the MIMOSA serie, emphazising the participation of the group.

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1. Introduction

A Monolithic Active Pixel Sensor (MAPS) integrates a detector element and the associated processing electronics in the same substrate (System-on Chip). It is fabricated using a standard CMOS process and thus its development can benefit of low fabrication costs and fast turnover. The first application of MAPS appeared in 1993 for photography, but the idea of using such devices for high-energy charged particle tracking was proposed by a Strasbourg group (IReS-LEPSI) in 1999 [1]. Our group in Saclay started studying MAPS in 2001, in close collaboration with the Strasbourg group, with the aim of proposing a vertex detector based on that technology for the International Linear Collider (ILC) under study.

The requirements for an ILC vertex detector are particularly stringent since the need for very high-precision measurements leads to unprecedented performances in terms of high granularity (pitch below 20 μm on the first layer), high read-out speed (around 25 μs in order to keep the occupancy below a few %), while keeping a very low material budget and power consumption.

2. From the standard 3-T architecture to a fast MAPS

The key element of the MAPS technology is the use of a N-well/P-epi diode to collect, through thermal diffusion, the charge generated by the impinging particle in the thin (typically of order 10μm) mostly undepleted epitaxial layer, underneath the read-out electronics (Fig. 1 left).

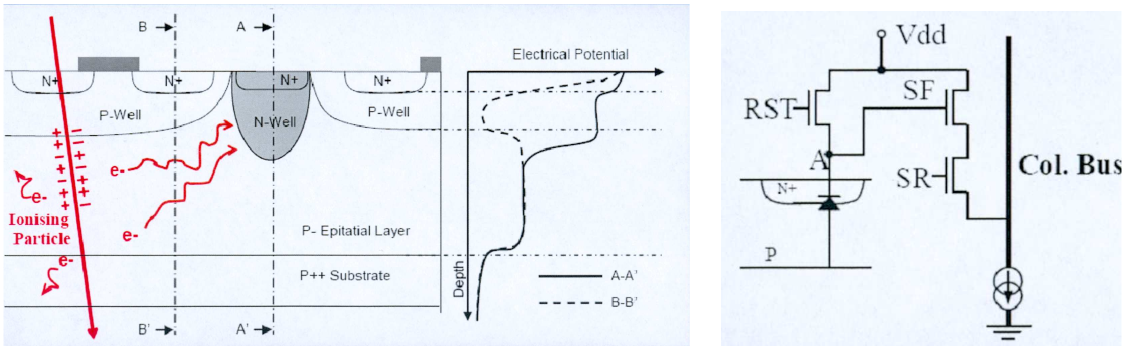

Figure 1: Detection principle of a minimum ionizing particle going through a CMOS sensor (left) and basic pixel read-out architecture (right).

As the early goal of these chips was to only demonstrate the feasibility of using MAPS for minimum ionising particles detection, the basic pixel design was chosen. Each pixel has only three transistors (Fig. 1 right) and the classical 3-T cell operation was carried on for reading out pixel signal. This has been achieved by Strasbourg.

In order to speed up the read-out, some signal treatment has to be included in the sensor design, in particular by implementing a pixel level correlated double sampling (CDS) and a column level offset compensated (autozero) discriminator as a first step towards a full numerization. These two important modifications from the original architecture have been carried out by the Saclay group.

2.1 Correlated Double Sampling

The useful signal is indeed the difference between a reference voltage, obtained just after the reset and the value read before the reset (Fig. 2 left). Because the useful signal and the fixed pattern noise (FPN) are of the same order of magnitude, and due to the need for on-chip data sparsification, an amplifier has to be integrated as close as possible to the charge sensing diode. Therefore, the pixel architecture is based on the combination of a charge detection diode, a double sampling circuit, a source follower (SF) and a row select switch (Fig. 2 right), which means only eight transistors per pixel.

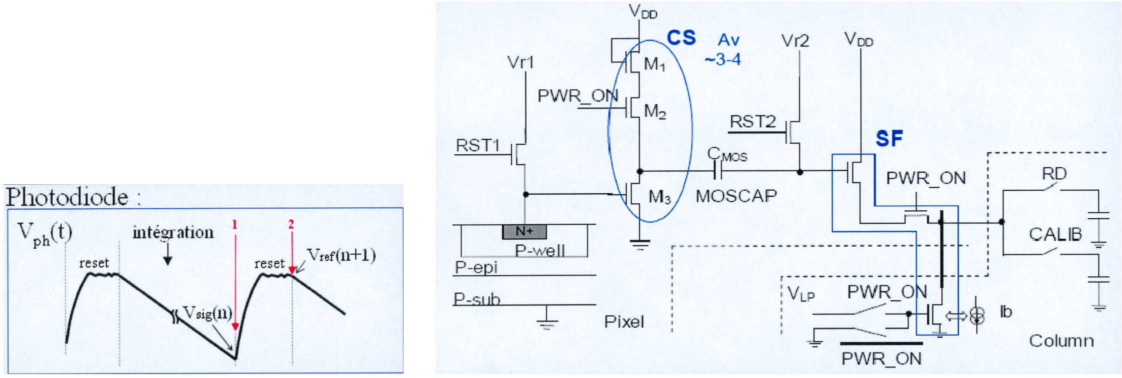

Figure 2: A readout cycle for MAPS (left), and Pixel architecture with integrated CDS (right)

2.2 Column level discriminator

A comparator transforming the output analog signal of a pixel into a 1-bit digital code is the first step towards a full digitization of the output data. Considering the small value of the analog signal, it is mandatory to use an offset compensated amplifying stage which corrects the residual offset of the comparator, leading to an architecture presented in Fig. 3.

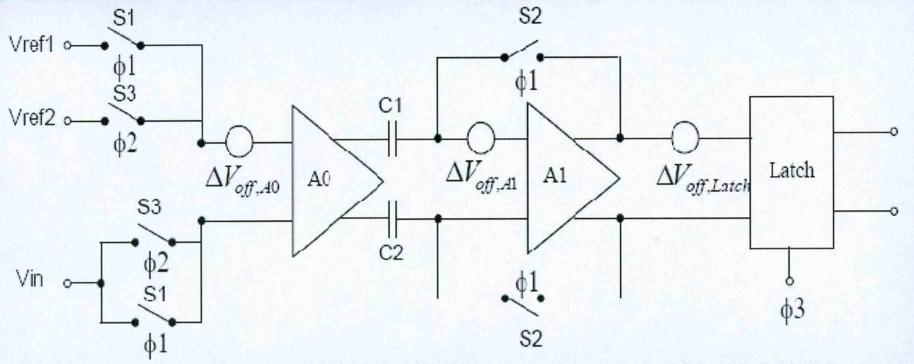

Figure 3: Architecture of the column level comparator

2.3 Prototypes fabricated with these features

Two prototypes have been realized in 2005 and 2007. Both chips consist in a 32 × 128 pixel matrix divided into four sub-arrays with essentially variations of the diode size. The pixel pitch is 25 μm $\times$ 25 μm. These chips have 24 columns connected with column level discriminators, leading to a binary output mode, while the remaining 8 columns have the original analog output. The chips are optimized to work at a main clock frequency of 100MHz, corresponding to a real readout speed of 20 μs per frame (column parallel readout scheme), with a power consumption as low as 430 μW per column (static). In early 2004, MIMOSA 8 was fabricated in TSMC 0.25 μm digital process with an epitaxial layer of 8 μm [2]. With the same general architecture, MIMOSA 16 has been fabricated in 2006 in AMS 0.35 μm OPTO process, in two versions corresponding to different thicknesses of the epitaxial layer : 14 μm and 20 μm.

3. Results and performances

Both chips have been characterized in laboratory, without and with a ^{55}Fe source, and then with high energy particle beams, at DESY and CERN.

3.1 MIMOSA 8 results

The main characteristics of the analog part (position of the calibration peak, temporal and fixed pattern noise, charge collection efficiency, ...) are rather independent on the main clock frequency. In particular, the noise is low (below 14 e$^-$) even for a readout speed of 15 μs per frame. The discriminator behaviour has been checked and worked properly. The detection performances have been measured at DESY, using a 5 GeV electron beam. Despite the modest thickness of the epitaxial layer, a signal over noise ratio of 9.5 (MPV) allows a very good m.i.p. detection performance summarized in Fig. 4. Typically, for a low discriminator threshold (around 4σ), the detection efficiency is above 99% with a fake rate of 0.1%, and the cluster multiplicity (binary outputs) around 3. All these results have been developed in [3].

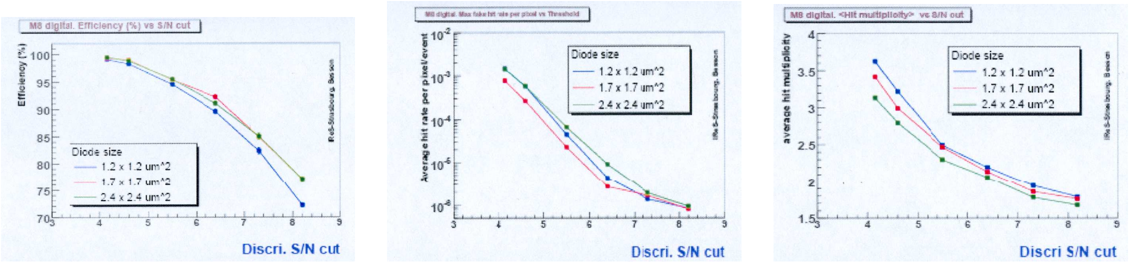

Figure 4: MIMOSA 8 : digital efficiency, fake rate and hit multiplicity as a function of the discriminator threshold

3.2 MIMOSA 16 results

These results are still preliminary since the the beam-tests took place only two weeks before the conference, in September 2007. Nevertheless, the noise performances have been found satisfactory (as for previous chips), but the charge collection efficiency is rather poor for three sub-matrices (probably due to too small diode sizes) and much better for the fourth sub-matrix (4.5 $\times$ 4.5 μm^2 diode). During this test campaign, at least one pixel architecture has been validated for next steps (Fig. 5, Table 1 and [4]).

Disc. threshold	det.efficiency	fake rate	single point resol.
4 mV	99.96 ± 0.03 (stat.)	$\sim 2.10^{-4}$	$\sim 4.9\ \mu$m
6 mV	99.88 ± 0.05 (stat.)	$< 10^{-5}$	$\sim 4.6\ \mu$m

Table 1 : characteristics of MIMOSA 16, submatrix S4

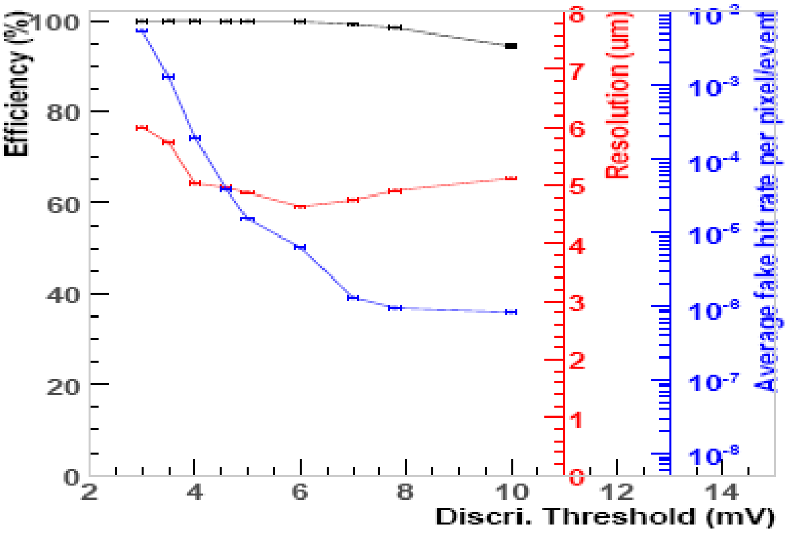

Figure 5: MIMOSA 16 : digital detection efficiency, fake rate and resolution as a function of the discriminator threshold

4. Contribution to the European project EUDET

Within the sixth framework program of the European Union, the EUDET project [5] has been financed with 21 Meuros for 4 years (2006-2009) in order to create an infrastructure to support the R&D for an ILC detector. 31 european institutes (and 20 more are associate) contribute. Inside this project, the JRA1 activity aims at the realization of a testbeam infrastructure including a fast, high-precision beam telescope. This pixel beam telescope consists in 4 to 6 layers of MAPS detectors, with an easy to use DAQ system including a trigger logic unit. A demonstrator has already been built with only three sensor planes made from MIMOSA 17 chips (256 × 256 pixels, 30 μm pitch, pure analog read-out) and first tests at DESY in June and July 2007, and at CERN early September 2007 (with a DEPFET pixel detector as Device Under Test) were very convincing. The final telescope (expected for mid 2009) will include an extension of MIMOSA 16 as sensors (1088 × 576 pixels, a read-out time of the order of 100 μs, an integrated zero-suppression, thined down to 50 μm), completed with a high resolution plane (pixels with 10 μm pitch). The standard setup will give a resolution around 2 μm, that can be improded to 1 μm with the help of the high-resolution tracker.

5. Conclusion :

Our next milestones include :

- MIMOSA 22 chip will be an extension of MIMOSA 16, with a larger surface, a smaller pitch, an optimised pixel architecture, JTAG and more testability. It will be the last step before the final chip for the EUDET telescope. The design is underway, and the submission is expected at the end of October 2007.
- Some 4 to 5 bits ADCs are studied at Saclay and in other french labs, in order to replace the (1-bit) dicriminators and increase the single point resolution. A mature design is expected during spring 2008.
- Strasbourg is developing a first fully digital prototype with a zero-suppression algorithm. It will be back from foundry late October 2007.

These studies are natural steps towards both the EUDET telescope and a vertex detector for a future linear collider.

Acknowledgements

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