PROCEEDINGS OF SCIENCE

Deep N-well CMOS MAPS with in-pixel signal processing and sparsification capabilities for the ILC vertex detector

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This paper is intended to discuss the features of a novel kind of monolithic active pixel sensors (MAPS) in deep submicron technology for use in charged particle trackers and vertex detectors. In such devices the triple well option, available in deep submicron processes, is exploited to implement analog and digital signal processing at the pixel level. This paper will discuss the design and performance of a deep N-well (DNW) monolithic sensor prototype including different test structures with both analog and digital functions. The paper also reports results from physical device simulations, aiming at evaluating the properties of the DNW sensor in terms of charge diffusion and charge sharing among pixels.

The 16th International Workshop on Vertex detectors
September 23-28 2007
Lake Placid, NY, USA

*Speaker.

PoS(Vertex 2007)016

1. Introduction

CMOS Monolithic Active Pixel Sensors (MAPS) represent a promising candidate for the innermost layer of the vertex detectors for experiments at future colliders such as SuperB or ILC ([1]-[3]). Their thin active volume (few tens of microns thick) allows a significant reduction of the material budget with respect to standard hybrid pixels. Moreover the increased radiation hardness brought about by the nanometer oxide thickness of modern deep submicron generations makes CMOS processes even more attractive to charged particle tracking applications [4].

In standard CMOS MAPS design, the charge released in the epitaxial layer by an ionizing particle is collected via thermal diffusion by an n-well/p-epitaxial diode. The charge-to-voltage conversion is provided by the parasitic capacitance of the sensitive electrode.

A different approach, with respect to the standard three-transistor (3T) front-end scheme, has been proposed to improve the readout speed potential of monolithic CMOS sensors. In the MAPS reported in this paper (whose basic structure is shown in figure 1) the collecting electrode is a deep N-well (DNW), which in CMOS deep submicron processes is used to shield n-channels devices from substrate noise in mixed-signal circuits. The use of a DNW as a collecting electrode makes it possible to lay out all of the n-channel transistors belonging to the front-end electronics over the sensor area, therefore reducing the impact of the electronics itself on the detector fill factor. In order to fully exploit the potential of complementary MOSFET processes and include also PMOS transistors in the design of the pixel level electronics, without significantly degrading the collection efficiency, the sensitive element has to take up a significant fraction of the elementary cell surface. Processing the signal from the deep N-well sensor by means of a charge sensitive amplifier decouples the charge sensitivity from the sensor capacitance and, therefore, from its area. Furthermore the large scale of integration of deep submicron CMOS technologies, while offering all the advantages of CMOS MAPS, may satisfy the need for implementing complex logic, such as a sparsification blocks in the small area of the elementary cell.

A set of prototype chips, called Apsel (Active Pixel Sensor Electronics) have been fabricated through CMP multiproject wafers in a STMicroelectronics 130 nm triple well process. These chips demonstrated the viability of the technology and the capability to detect ionizing radiation. A detailed description and results from the characterization of the prototypes can be found in ([5]-[9]).

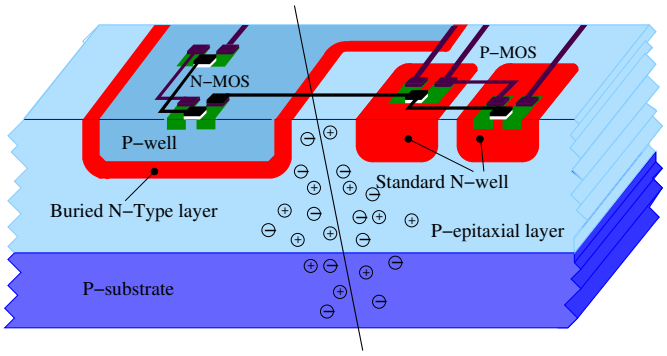

Figure 1: simplified structure of deep N-well MAPS.

The Sparsified Digital Readout chip, (SDR0), whose design and performance will be discussed in this paper, has been conceived in view of vertexing applications at the International Linear Collider. The chip includes a number of structures aiming at demonstrating the feasibility of pixel-level sparsification in MAPS designed in deep submicron technologies.

2. Deep N-well MAPS for the ILC vertex applications

2.1 ILC vertex detector requirements

The ILC is expected to have a beam structure with 2820 bunch crossings in a 1 ms train and a repetition rate of 5 Hz. The pixel detector is comprised of 5 small concentric cylinders of pixels wrapped around the beam interaction point. Physical simulations show that for a linear e+e- collider operated at 500 GeV, a maximum hit occupancy of 0.03 particles/crossing/mm^2 can be considered a reasonable assumption in the innermost layer of the detector [10]. If charge spreading in the sensor volume and interpixel hits are accounted for, 3 pixels can be expected to fire for every particle hitting the detector. Thus the hit rate on the innermost cylinder is about 250 hits/train/mm^2. If a binary readout approach is adopted, a resolution position better than 5 micron requires a square pixel with a pitch smaller than 17.5 μm. If a 17.5 μm pitch is assumed, then the occupancy for a single cell is close to 0.076 hits/train. Given these figures, the probability of a cell being hit at least twice during a bunch train is 0.3%, which means that a pipeline with a depth of one would be sufficient to record around 99.7% of the events without any ambiguity. This value changes, of course, as a function of the hit rate and of the detector pitch.

2.2 Prototype design

A test chip, named SDR0 (Sparsified Digital Readout), has been designed and submitted for fabrication in the 130 nm STMicroelectronics CMOS technology available through CMP (Circuit Multi Projets). The sparsified readout architecture implemented in this prototype is a simplified version of the FPIX digital readout scheme ([11]-[12]). A block diagram of a pixel cell is shown in figure 2. The analog front-end consists of a charge preamplifier followed by a threshold discriminator. In order to achieve a high charge sensitivity (about 800 mV/fC), the capacitance feedback is obtained from the drain-source capacitance of the feedback transistor, since design rules prevent such a small capacitor from being laid out using standard cells.

In the DNW-MAPS for the ILC vertex detector, besides the analog circuits, the elementary cell also includes a 5-bit time stamp register and a set of logic blocks implementing data sparsification, namely a hit latch, a token passing core and a get bus latch. The 5 time stamp bits are fed to the time stamp register by a Gray counter located on the chip periphery and allow the bunch train interval to be subdivided into 32 time slots.

Figure 3 shows the block diagram of a 16x16 DNW-MAPS matrix describing the sparsified readout architecture, which was first implemented in the VIP1 chip [13]. MAPS sensor operation in the prototype chip is tailored on the structure of the ILC beam and features two different processing phases: a detection (corresponding to the bunch train period) and a readout phase (corresponding to the intertrain period). During the detection phase the time stamp is sent to all cells. When a

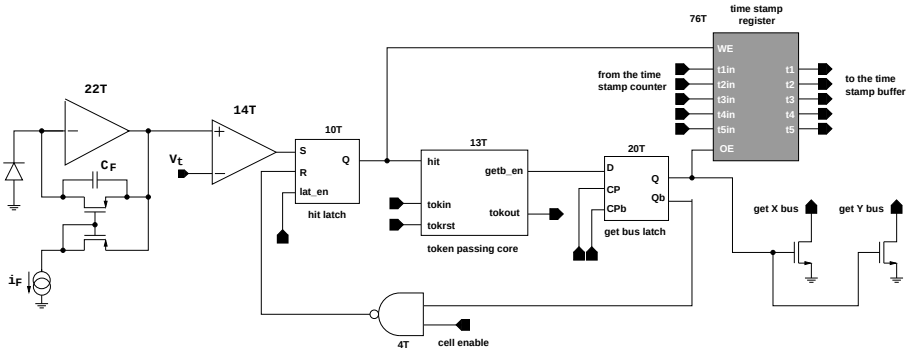

Figure 2: block diagram of the in-pixel electronics (charge preamplifier, discriminator and sparsification logic).

cell is hit, the content of its time stamp register is latched by the pixel hit signal (through the write enable line, WE). At the end of the bunch train period, the latches are disabled (by pulling down a latch enable signal) and the readout phase starts. A token is launched and a sparse readout is performed row by row. The token scans the matrix and stops in the first hit cell. This cell, at the first rising edge of the cell clock, gets hold of the X and Y buses, pointing to the address registers at the periphery of the matrix, and sends off the previously stored time stamp.

While a pixel is being read, the token is released and scans ahead, looking for the next pixel to read. All the digital information (X, Y and time stamp) is serialized and transmitted off the chip within a cell clock period. In the case of the ILC pixel vertex detector, 199 ms are available in each cycle to readout the hits from bunch train before the next train arrives. In a 1000x1000 array of

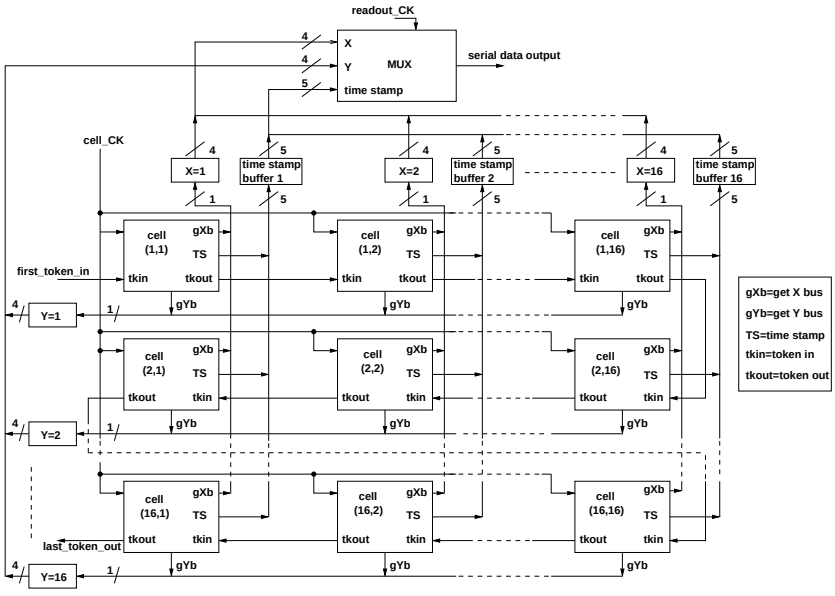

Figure 3: digital readout architecture of the DNW-MAPS sensor with sparsified readout and time stamping capability.

pixels, featuring a 17.5 μm pitch, the maximum number of hits in the hottest part of the detector is calculated to be about 76600 in a bunch train. If a 30 bit word is used for each hit pixel (10 plus 10 bits for the X and Y pixel coordinates and 5 for the time stamp, while the remaining 5 bits can be used, for instance, for chip identification) chip readout at 50 MHz takes about 46 ms, far less than the 199 ms allowed. Note that increasing the size of the matrix would require no further complication for the in-pixel logic, but just larger X and Y registers and a multiplexer with a larger number of inputs.

The power dissipated by a full scale version of this design has to be consistent with air cooling of the ILC pixel vertex detector. This sets very stringent constraints for the power dissipation of the entire detector, which should not exceed 20 W. The average dissipated analog power in this prototype is about 50 nW per channel, if a power cycling with 1% duty cycle is considered. The main contribution to the digital power consumption arises from the leakage currents in the devices belonging to the logic section and is about a factor of 5 smaller than the analog term. Given these figures, the overall power consumption in the full-scale detector does not exceed the power dissipation limits set in the Large Detector Concept (LDC) proposal for the ILC [14] .

3. Device simulations

Physical simulations with the TCAD package have been performed on a 3x3 matrix with elementary cells featuring the geometry shown in figure 4(left). The size of the elementary sensor, where as many as 164 transistors are integrated, is 25μm x 25μm. The simulated structure, which reproduces the geometry of the SDR0 matrix, required a mesh with 165000 vertices. Because of the really long computation time only 36 simulations, each one involving a different MIP collision point, have been performed according to the point grid shown in figure 4(right).

The Heavy Ion model, available for transient simulations, was used to generate a uniform charge distribution along the particle track with a release rate of 80 e-h pairs/μm. Figure 5(left) shows the charge collected by the central pixel as a function of the position of the impinging

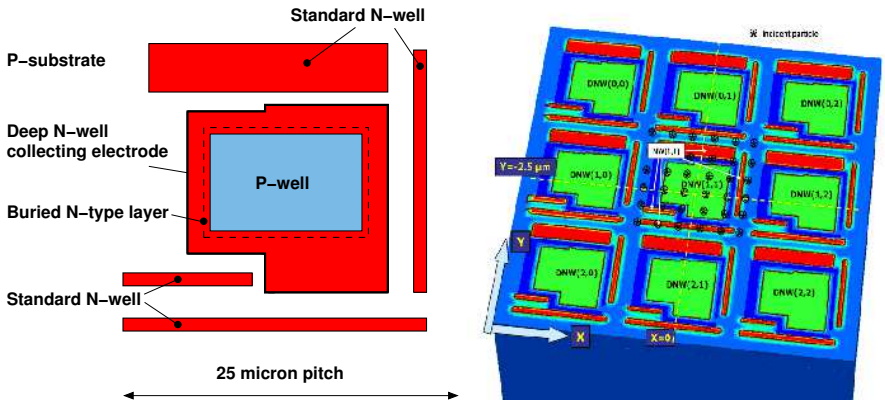

Figure 4: (left) top view of the SDR0 elementary cell layout; (right) 3x3 matrix featuring the SDR0 geometry simulated with the Synopsys TCAD package.

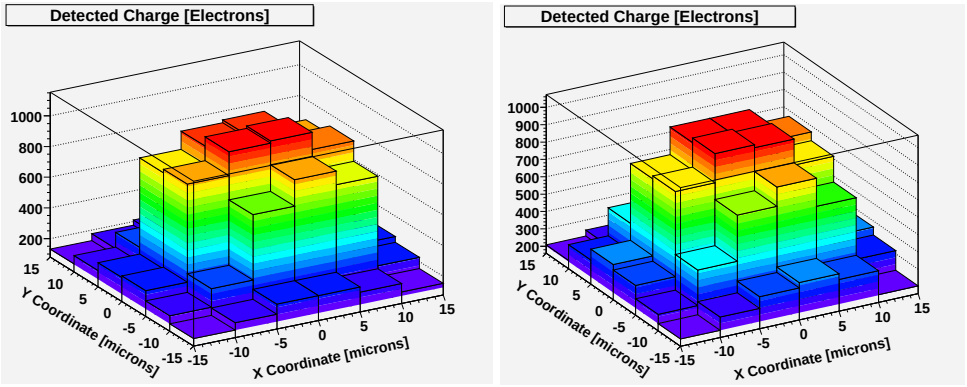

Figure 5: charge collected by the central pixel of the 3x3 matrix, as a function of the MIP collision point: (left) Synopsys TCAD and (right) Monte Carlo simulation results.

particle. Detected charge, featuring a maximum value close to 1000 electrons, almost uniformly decreases down to less than 200 electrons at the pixel periphery.

A Monte Carlo algorithm has been developed to simulate the random walk of electrons in the undepleted substrate of MAPS detectors, where diffusion is the main transport mechanism of minority carriers [15]. With reference to figure 5(right), which shows the charge collected by the central pixel matrix for the same 36 collision point used in the TCAD simulations, both the maximum collected charge and the overall distribution are in good agreement with results shown in figure 5(left).

Taking advantage of the really short computation time, Monte Carlo methods will be used, beside the Synopsys TCAD software package, in the design of the next generation prototypes in order to determine the best collecting electrode geometry from the standpoint of charge collection efficiency.

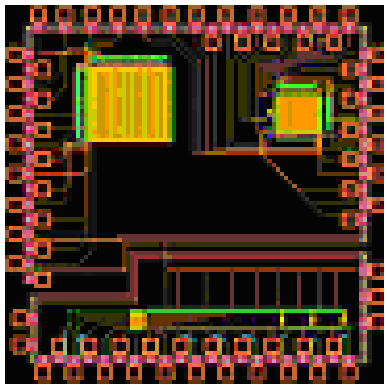

Figure 6: layout of the SDR0 prototype. The chip size is about 2.3mm x 2.3mm.

4. Experimental results

The SDR0 chip was submitted in November 2006 and delivered in July 2007. The layout of the chip is shown in figure 6. The test chip includes three DNW-MAPS matrices, and a number of single cell structures described in table 1.

In the SDR0 design the pixel level front-end processor includes a charge preamplifier and a threshold discriminator. This shaper-less version of a classical readout chain for capacitive detectors (as shown in figure 2) was forced by the resolution requirements of the ILC vertex detector, which, in the case of a binary readout channel, directly impact on the elementary cell dimensions and on the complexity and number of transistors in the readout electronics. Charge restoration in the preamplifier feedback network is obtained through a current mirror stage, providing a linear discharge of the feedback capacitor. The input NMOS transistor dimensions, W/L=22/0.25, were optimised for a sensor parasitic capacitance CD of 120 fF. The drain current in the input element was set to about 1 μA in order to cope with ILC power dissipation constraints.

The experimental results presented in this section are relevant to the 3x3 matrix and the C1, C2, C3 test structures. Figure 7(left) shows the signal at the charge preamplifier outputs of the 3x3 matrix. In this measurement an input charge of about 800 electrons is applied to the central element through an injection capacitance and the 9 charge preamplifier outputs are monitored at the same time. No crosstalk between pixels is present since the outputs of the 8 peripheral pixels are barely noticeable in the displayed amplitude scale with respect to the central one. An equivalent noise charge of 60 e- rms and a charge sensitivity of about 700 mV/fC were measured for the central pixel of the 3x3 matrix.

Actual operation of the deep n-well sensor was emulated by means of a low power InGaAs/Ga-

Cell name	Description
16x16 matrix	features the digital sparsified readout architecture described in section 2;
8x8 matrix	features the digital sparsified readout architecture described in section 2 and selectable access to the output of the charge preamplifier in each cell;
3x3 matrix	all the outputs of the charge preamplifiers in the 9 elements of the matrix are accessible at the same time. Charge can be injected at the preamplifier input in the central pixel through a 60 fF MIM capacitor;
C1 test structure	consists of a readout channel where the NMOS devices of the analog section are integrated inside the DNW, but the DNW is not connected to the preamplifier input; a 60 fF MIM capacitor in series with the input device gate is used for circuit testing through external charge injection; a 90 fF detector simulating MIM capacitor is connected to the input device gate;
C2 test structure	identical to C1, but with a 120 fF detector simulating MIM capacitor shunting the input device gate instead of a 90 fF one;
C3 test structure	identical to C1, but with a 60 fF detector simulating MIM capacitor shunting the input device gate instead of a 90 fF one;

Table 1: description of the matrices and of the single cell structures in the SDR0 chip.

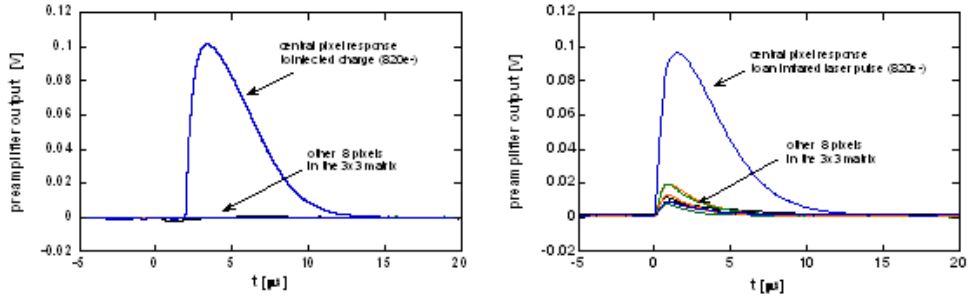

Figure 7: signals at the charge preamplifier outputs of the 3x3 matrix. An input charge of about 800 electrons is injected in the central pixel: (left) through a 60 fF MIM capacitor in series with the preamplifier input terminal and (right) with an infrared laser.

AlAs/GaAs laser source operating at a wavelength λ of 1064 nm. As compared to radioactive sources, the main advantage of using a laser device as a preliminary test source lies in the fact that the same signal can be used to synchronize both the laser and the scope operation thereby simplifying signal visualization without need for coincidence apparatus. The experimental set-up was described in [15]. In order to avoid reflection from the thick net of metal interconnections on the top side of the die, pixels were back-illuminated. The 3x3 matrix response to an infra-red laser with a focused spot (σ_{xy} about 15 μm) has been tested (see figure 7(right)), showing a limited charge spread between pixels.

5. Conclusions

In this paper we presented the design of a DNW-MAPS prototype chip tailored for vertexing applications at the ILC experiments. This prototype chip features a sparsified readout architecture, and time stamping capabilities. Preliminary results on the 3x3 matrix are very encouraging. Measurements on the 8x8 and 16x16 matrices are in progress in order to test the sparsified digital readout architecture. New tests with particle sources, which should be useful to provide a more precise calibration of the pixels, have been scheduled. A smart layout of the detector sensitive area will also be studied with the purpose of maximizing the charge detection efficiency. Based on the elementary CMOS pixel presented in this work, a 256x256 matrix for a beam test will be designed and submitted in 2008 in the same technology.

6. Acknowledgments

The authors wish to thank R. Yarema and the FNAL ILC R&D group for the useful discussions that helped us to choose the digital processing scheme implemented in the DNW-MAPS demonstrator. The authors also thank E. Pozzati who performed physical simulations of the MAPS devices, C. Andreoli, who laid out the prototype discussed in this work, M. Dellagiovanna who characterized the SDR0 chip discussed in this paper. The authors are also grateful to D. Christian for his useful suggestions about device simulations. The authors wish to acknowledge M. Caccia

and his collaborators at University of Insubria for their contribution to the fabrication and test of the SDR0 test board.

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