PROCEEDINGS OF SCIENCE

A CCD Based Vertex Detector

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The Linear Collider Flavour Identification (LCFI) collaboration is engaged in R&D towards a CCD-based vertex detector for the International Linear Collider (ILC). The demanding requirements for small pixel size, low mass and low occupancy readout pose significant challenges to the detector development. We are working on two detector technologies, the Column Parallel CCD (CPCCD) and the In-situ Storage Image Sensor (ISIS). The evaluation of our second generation CPCCD (CPC2) and its readout and driver chips is presently in an advanced stage. In stand-alone mode the high speed CPC2 achieved operation at 45 MHz, which is a major milestone. The column parallel readout chip CPR2 was bump-bonded to CPC2 and the voltage channels of the hybrid assembly showed good performance in X-ray tests. The signals from the CPC2 were amplified, digitized and sparsified by the logic in CPR2. After the successful proof-of-principle first generation ISIS1 we are now planning to continue with new, more advanced device. In this work we present the status and the tests results from our CPCCD and ISIS developments.

The 16th International Workshop on Vertex detectors
Lake Placid, NY, USA
23-28 September, 2007

[1] Speaker on behalf of the Linear Collider Flavour Identification (LCFI) Collaboration

PoS(Vertex 2007)020

1. Introduction

The ILC will require high performance vertex detector for accurate reconstruction of decay chains, pure and efficient *b* and *c* tagging and vertex charge measurements [1][2]. The vertex detector has to improve significantly upon the most accurate one built so far, the VXD3 [3], with several times better impact parameter resolution, lower mass and low occupancy readout. Charge Coupled Devices (CCD) were used as sensors in VXD3 due to their high resolution, excellent gain uniformity and small layer thickness, which makes them one of the most likely candidates for the vertex detector at the ILC.

CCDs are well suited for linear collider environments [4] because of the much cleaner interactions and low backgrounds compared to those at hadron colliders. The small CCD pixels (20 μm × 20 μm or below) allow excellent spatial resolution and two-track separation. This is helped by the low power dissipation, allowing the use of extremely low mass support mechanics. Large granularity, e.g. 2500 pixels/mm^2, permits integration of many events without loss of information due to overlaps. The CCD structure has 100% fill factor and all the active components are placed at the ends of the chip, which is very attractive for applications such as particle detection and imaging. Additionally, devices with an area of tens of square centimetres are readily available, which allows one to build detectors with optimal geometry.

2. Requirements

The physics program at the ILC demands vertex detector with point resolution of around 3.5 μm and mass below 0.1% X_0 per layer to reduce the multiple scattering in the support material and the sensors. Low mass is possible only if the average power dissipation in the detector is no higher than approximately 50 W. This allows gaseous cooling, essential for the reducing the amount of material.

One of the most severe requirements is to keep the pixel occupancy below 1% in order to ensure efficient pattern recognition. This is particularly challenging for the inner layer of the detector. One way to achieve that is to read out the sensors multiple times during the 1 ms-long bunch train, as done with the CPCCD. Another possible way is to collect a number of signal samples at regular intervals during the bunch train and store them in pixel, and read out in the 200 ms-long gap between the bunch trains. This method is used in the ISIS.

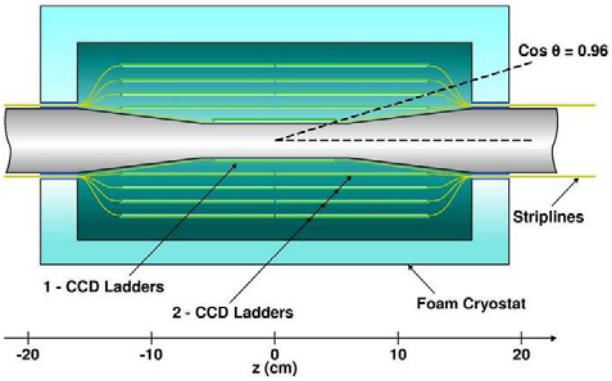

Figure 1. Conceptual vertex detector design.

The present conceptual vertex detector design is shown in Fig 1. It consists of 5 concentric sensors barrels at radii 15, 26, 37, 48 and 60 mm. The inner layer is comprised of 100 mm long sensors, clocked and read out from both ends. The outer layers are made off two 125 mm long sensors, butted together and each readout from one end only. The detector is placed in low mass foam cryostat and cooled by flow of nitrogen gas. The vertex detector in this design contains almost a billion 20 μm × 20 μm pixels.

3. Development of the CPCCD and readout and drive systems

The CPCCD work is the main detector R&D at LCFI. In the CPCCD the conventional serial register is removed; instead every column is connected to an amplifier and an ADC. This allows decrease of the readout time by 2 to 3 orders of magnitude, which is needed to reduce the hit pixel occupancy to below 1%. For the inner layer sensors this translates to column parallel readout at 50 MHz, while for the outer layers this is 25 MHz. Unlike the traditional CCDs, the whole image area of the CPCCD is clocked at a high rate, which creates the challenge of delivering large currents to the gate structure. To minimize power dissipation, the CPCCD is designed to work with low clock amplitudes, usually below 2 volts.

3.1 CPC2

The CPC2 is our second generation CPCCD, following the successful first prototype CPC1. An important new development in CPC2 is the busline-free design for clock distribution. In this architecture the clocks propagate on two metal layers covering the entire image area of the CCD, as shown in Fig. 2. This drastically reduces the parasitic resistance and inductance associated with the conventional CCD buslines and enables efficient clocking at high speed.

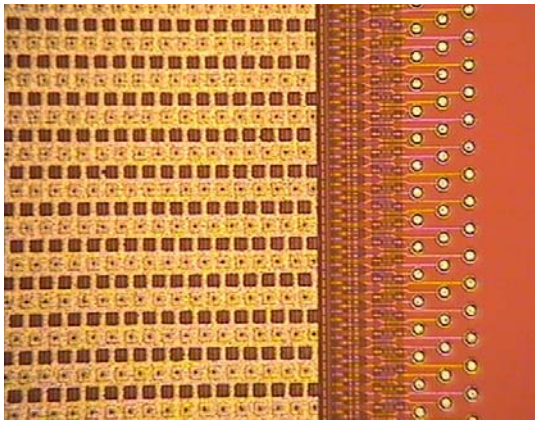

Figure 2. Microphotograph of the busline-free CPC2.

Three sensors with common design and functionality, but different size were manufactured by e2V Technologies, shown in Fig. 3. The largest CPC2-70 has an image area of 92 mm × 15 mm and total size of 105 mm × 17 mm, allowing for 2 bump-bonded readout chips. This device is almost the size needed for the outer layers of the vertex detector at the ILC. The middle size CPC2-40 (53 mm × 15 mm image area) represents half of the inner layer of the vertex detector and is being used for tests at speeds up to the design goal of 50 MHz. The smallest chip CPC2-10 (13 mm ×15 mm) covers most of the test program because of the large number of available devices.

The chips were produced on two types of wafers: some with 100 Ω.cm, 25 μm thick epitaxial silicon and the remainder on 1.5 kΩ.cm, 50 μm thick material. The purpose of this is to study charge collection in CCDs with different depth of the depleted region. In addition, low-speed CPC2 version with conventional single level metallization and buslines was also

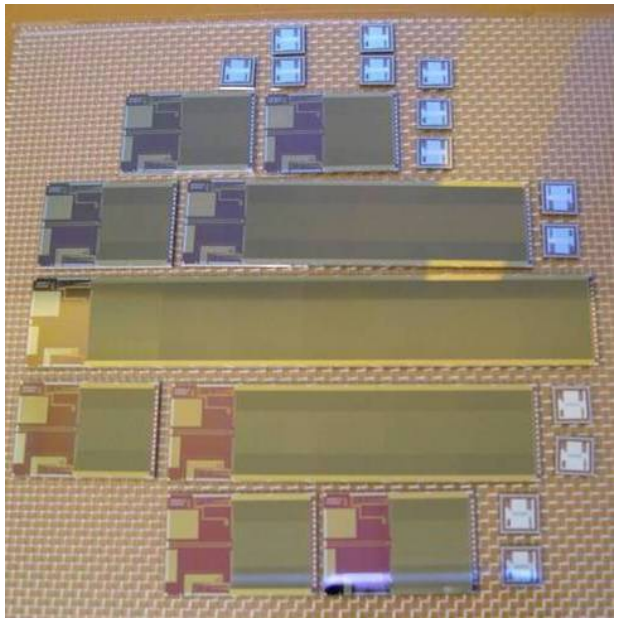

Fig. 3. CPC2 chips of different size.

produced.

In the first tests the busline-free CPC2 chips were driven by miniature air core transformers, embedded in a multi-layer PCB and fed from power RF amplifier. We observed X-ray signals from a ^{55}Fe source (5.9 keV, producing 1620 electrons) at clock frequency up to 45 MHz. The performance was dominated by the numerous parasitics of the PCB transformers, leading to clock asymmetry. In addition, we found that the noise from the RF amplifier was too high, and it coupled to the output CCD signal. Despite this, the result is very close to the desired clock speed and an important milestone for the LCFI collaboration.

3.2 Experimental CCDs for clock power reduction

One major issue associated with the CPCCD is the need to drive the large gate capacitance at high speed, which implies large currents and power in the driver system. Together with e2V Technologies, we have developed a range of small CCD which will allow us to study several measures for reduction of the inter-gate capacitance C_{ig} and the clock amplitude. Some of the designs could reduce C_{ig} by a factor of 2 to 4, with corresponding reduction of the clock power.

We have already submitted these experimental designs for manufacture and expecting delivery by December 2007.

3.3 Column parallel readout chip CPR2

Our second generation readout chip CPR2 builds on the experience gained with the previous chip CPR1, which was successfully operated bump-bonded to a CPCCD. CPR2 has banks of 125 voltage and 125 charge amplifiers, matched to the outputs of CPC2, and 5-bit ADC per column. In addition, CPR2 implements cluster finding logic on 2×2 pixel kernel and sparse readout circuitry. Numerous test features have been provided, such as direct analogue inputs and outputs from selected amplifiers, scan register for independent tests of the sparsifying logic and direct monitoring of any ADC channel. The clock distribution network has been improved to reduce the differential nonlinearity of the ADCs.

The chip logic continuously calculates the cluster sum within the 2×2 kernel from every two adjacent columns. Upon exceeding a global threshold, an area of 4×9 pixels around the cluster is flagged for readout and later multiplexed to the 5-bit wide chip output. Using the scan register and X-rays from a bump-bonded CPC2, the sparsification logic was tested with both simulated and realistic signals. It was found that CPR2 exhibits variable dead time between clusters separated in time by less than 60 to 100 pixels, as shown in Fig. 4. The reason for this is the limited memory in the column buffers, which leads to blocking of new clusters from reaching the output until the old ones have been read out.

The analogue front end was found to work well up to 9 MHz. The main limitation on the performance is the differential nonlinearity of the ADCs, which increases to the level when many missing codes begin to appear. The noise of the voltage processing channels is around 80 e- ENC. No signals were observed from the charge channels and the reason for this is under investigation. Gain loss of about 50% was observed in the voltage channels. This changes almost linearly from the edge of the chip to the centre, and is most likely due to voltage drop across metal tracks.

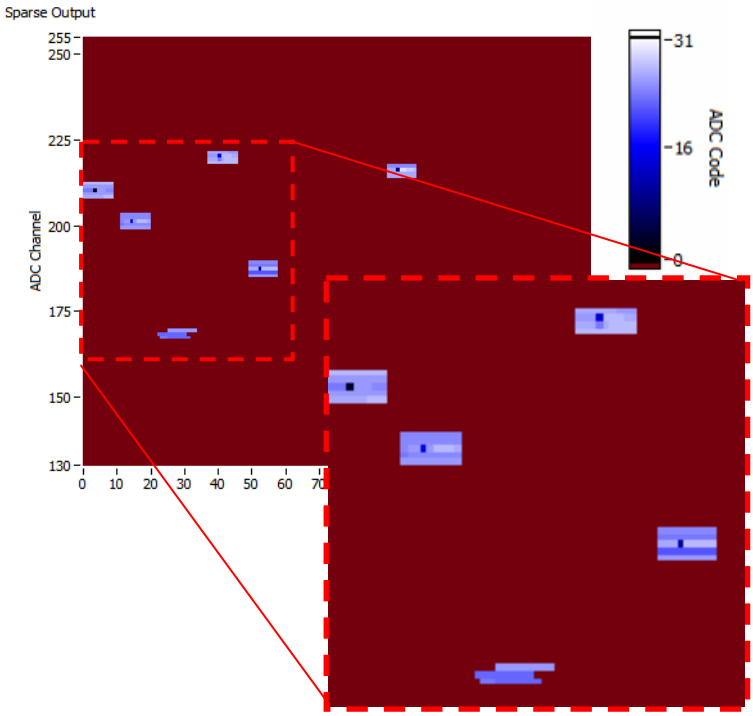

Figure 4. Output from CPR2 using X-ray signals from a bump-bonded CPC2. The direction of transfer is from right to left. The zoomed section shows correctly processed clusters from the voltage amplifiers, as well as a distorted cluster caused by the finite column memory.

All this is now being addressed in our new CPR2A chip, which is in an advanced design stage. In the CPR2A the local memory buffer has been increased 3-fold and the size of the cluster has been reduced to 4×6 pixels. The logic has been re-designed to efficiently store up to 3 consecutive clusters using the same timestamp, thus saving memory and space. In addition, each cluster finder column will have individual 7-bit threshold, needed to correct for gain non-uniformities in the signal amplifiers. These measures will significantly improve the chip's capabilities to process groups of dense hit patterns and reduce the dead time. To independently test the front end amplifiers, input calibration circuitry will also be included.

3.4 Driver system for CPC2

Due to the limitations of the transformer-based system, described above, we initiated another development based on CMOS technology. A CMOS chip could produce clean CCD clocks by switching between two stable supply voltages with controlled slew rate. It is also much less material, because the multi-layer copper transformer is avoided.

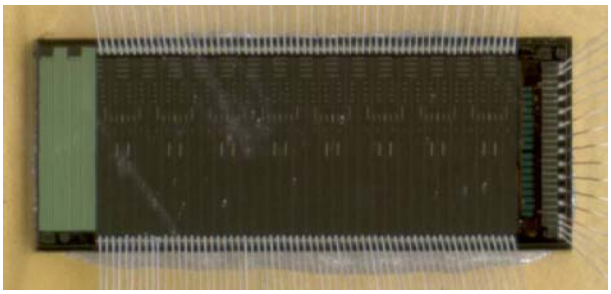

Fig. 5. The CPD1 driver chip for CPC2

We designed a dedicated driver ASIC, the CPD1 (Fig. 5), made on 0.35 μm CMOS process. It uses optimized layout techniques for achieving minimum parasitic inductance in the clock and power paths. CPD1 is nominally supplied with 3.3 V and the user can switch each of the 8 sections individually, as well as digitally control the slew rate of the output clocks. The gate capacitance of the busline-free CPC2-40 is 40 nF/cm^2/phase and current in excess of 20 A is required to drive it at 50 MHz. CPD1 is rated for that current and can generate both clocks needed for driving 2-phase CCDs such as CPC2.

CPD1 has a built-in capacitor, internally connected to one of the sections, which allows testing on an equivalent load of 32 nF with minimum parasitic impedance. The results at 50 MHz show excellent clock quality. We believe that similar performance could be achieved by bump bonding the CPD1 chip to a next generation CPCCD because of the very low interconnection impedance.

Using the CPD1 chip, the readout noise at 10 MHz was reduced from 200 e- ENC (with the transformer) to 75 e- ENC. The CPD1 could provide clocks in the range between 1.2 V to 3.3V when driving large capacitive load. Using clock voltage scans, the minimum clock amplitude for efficient charge transfer in CPC2 was found to be 1.35 V. An ^{55}Fe X-ray spectrum taken at 20 MHz is shown in Fig. 6. Further tests will continue by improving the experimental setup and possibly producing even better performance.

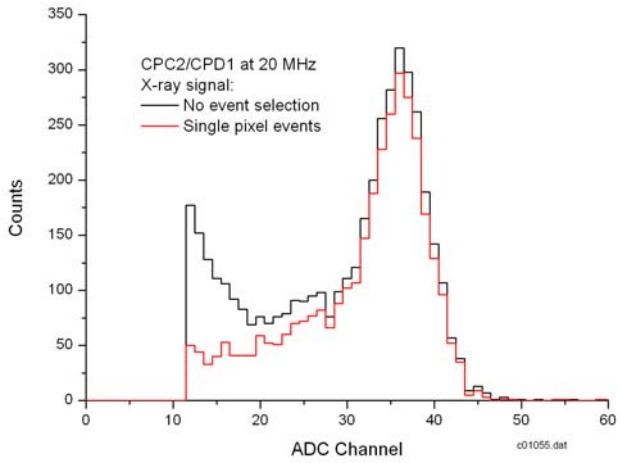

Fig. 6. ^{55}Fe X-ray spectrum from CPC2 at 20 MHz, using the CPD1 driver. The system noise is 110 e- ENC.

4. Development of the ISIS

4.1 Principles

In parallel with the CPCCD development, LCFI is pursuing another CCD-based sensor, the In-situ Storage Image Sensor (ISIS) [5]. In every pixel of this device there is a CCD with 20 storage cells and 3-transistor readout circuitry, similar to that found in the Monolithic Active Pixel Sensors (MAPS), and shown in Fig. 7. Charge generated by Minimum Ionising Particles (MIP) is transferred and stored in the CCD 20 times during the 1 ms-long bunch train at ILC. Readout is carried out in the 200 ms-long gap between the bunch trains, at 1 MHz rate, using column parallel architecture. This readout scheme is equivalent to 20 complete readouts of the CPCCD at 50 MHz.

The deep *p*+ shielding implant protects the CCD storage register from most of the direct charge collection by reflecting it back to the epitaxial layer. The contribution of the parasitic charge generated in the CCD channel is given by the ratio of thicknesses of the epitaxial layer above and below the buried *p*+ shield. This is 10% or less and should not be a significant source of error. The aperture allows the charge to enter the CCD register only through the photogate for sequential storage.

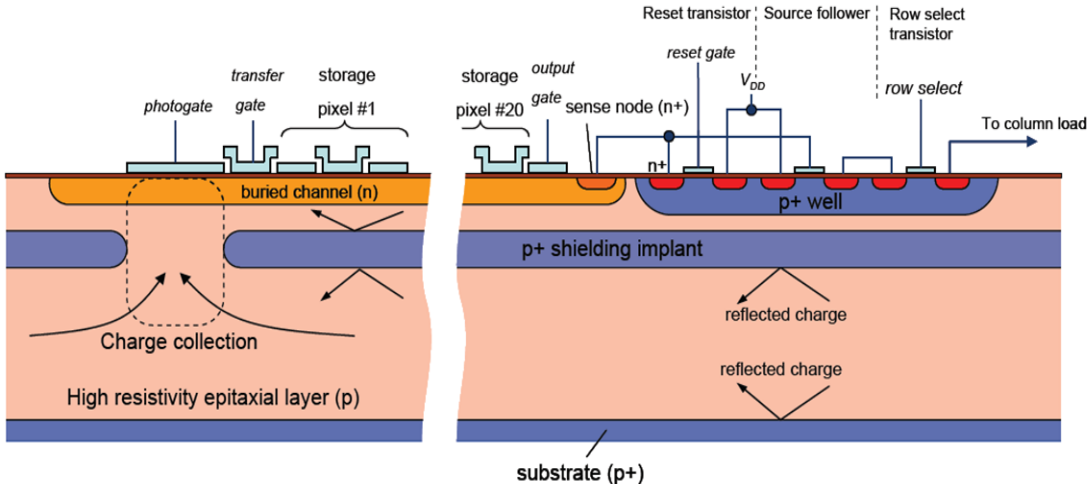

Fig. 7. The In-situ Storage Image Sensor.

One of the main advantages of the ISIS is its immunity to beam-related electromagnetic interference, because the signal is kept in the charge domain during the entire beam duration. In addition, the ISIS could be orders of magnitude more radiation resistant than the CPCCD due to the reduced number of charge transfers. One could also achieve lower readout noise because of the relaxed clock frequency, allowing longer shaping times.

The ISIS is also a lot easier to clock due to the low readout frequency and does not require a dedicated driver. Clocking during the charge storage phase should not be difficult because it is done at 50 μs intervals, resulting in clock speed of only 20 kHz. However, care should be taken to finish the charge transfer within the inter-bunch spacing of 337 ns to avoid smear.

4.2 ISIS1

Together with e2V Technologies, LCFI has designed and manufactured the first ISIS device (ISIS1), based on a standard CCD process. In contrast to the layout shown in Fig. 7, ISIS1 uses diffused deep *p*+ well for charge shielding of the CCD register. This choice was driven by technology constraints in producing deep doping profiles. The device is an array of 16×16 ISIS pixels, each containing a 3-phase CCD with 5 storage cells, reset transistor, source follower and a row select transistor. Due to process limitations the pixels are laid on 40 µm × 160 µm pitch and no on-chip logic for row selection and clocking is provided. The first tests of the ISIS1 used pulsed light for charge generation and showed correct capture and transfer of signal into the CCD register, corresponding to the different time samples. Initially only devices without the deep *p*+ well were available, and the results of the tests with 5.9 keV X-rays are shown in Fig. 8. Later chips with the *p*+ well were delivered and are now being tested.

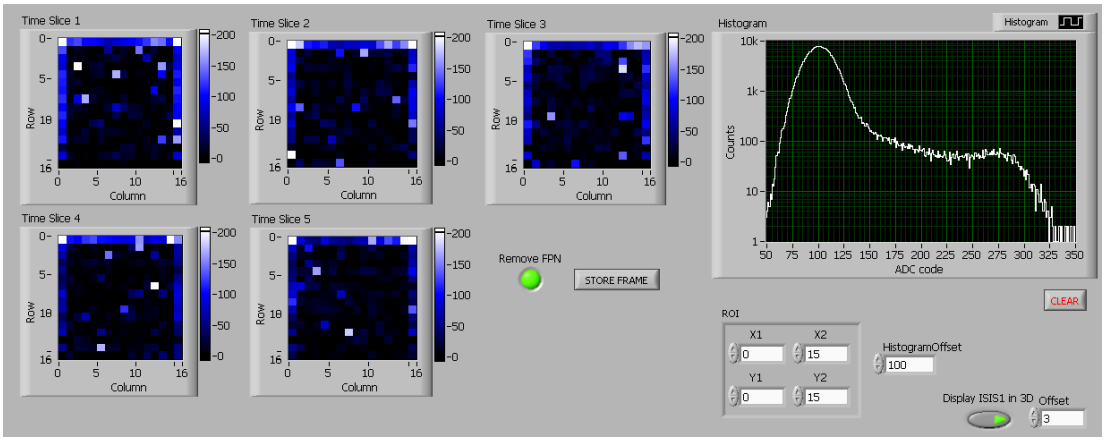

Fig. 8. X-ray tests of ISIS1 without deep p+ well. Each time slice shows X-ray signals collected in the corresponding storage cell with numbers from 1 to 5. The histogram of the signals from all pixels and storage cells is displayed in the fugure on the right. The 5.9 keV peak is clearly visible at ADC channel 275.

The development of a next-generation ISIS with 20 µm × 20 µm pixel size is an ambitious goal which LCFI is actively pursuing. The combination of active transistors in every pixel, logic circuitry and CCDs in one monolithic device is challenging and will most likely require modifications to an existing CMOS process with feature size below 0.25 µm.

5. Mechanical support studies

One of the main design requirements for the vertex detector is to reduce the amount of material to below 0.1% X_0 per layer, equivalent to only 100 µm of silicon. For comparison, the nominal active device thickness (the epitaxial layer) in CPC2 is 20 µm.

A part of our R&D programme is to study and design mechanical supports for such thin sensors, able to maintain mechanical stability at micron level. In the past, studies were done

with 20 μm silicon mounted on thin beryllium substrate with multiple glue pillars and even 50 μm thick sensor supported only at the ends and held under tension for stability. Due to thermal mismatch between silicon and beryllium the former was found prone to distortions at 100 μm level, while the latter could not satisfy the requirements for low lateral deformation.

At present we are working on support structures using modern foam materials, like reticulated vitreous carbon (RVC) and silicon carbide (SiC). Both are excellent thermal match to silicon. For example, 1.5 mm thick RVC foam with 3% relative density, sandwiched between two 25 μm silicon pieces could achieve 0.09% X_0. The two silicon pieces (of which one or both could be sensors) are required for rigidity. We have also made mechanical assemblies using SiC with 8% relative density. This achieves 0.16% X_0 with 25 μm silicon mounted on one side only. Unlike RVC, SiC has very high Young's modulus and does not require additional support. In the future, 5% SiC foams will become available, which will bring the material budget down to 0.09% X_0.

6. Conclusions

The work at LCFI towards a CCD-based vertex detector for the ILC is advancing. Our second generation CPC2 is a large device and a major step towards detector-scale demonstrator. Stand-alone tests have shown successful operation at 45 MHz using the developed busline-free devices and transformer drive. The driver chip CPD1 has also been successfully designed, manufactured and tested. It has shown satisfactory performance driving large currents at frequencies up to 50 MHz. In system tests, operation of CPC2 with CPD1 driver has been observed at 20 MHz and the effort to extend the range is continuing. The readout chip CPR2 was bump-bonded to CPC2 and operated at up to 9 MHz. X-ray signals from CPC2 were amplified, digitized and the output data sparsified by the powerful logic inside CPR2. Following the successful tests of CPR2 and some of the issues that were discovered, a new chip CPR2A is now being designed and is nearly finalized.

The CCD-based ISIS concept has numerous advantages tailored for the ILC environment and is an extremely promising device for the future vertex detector. The first prototype has already been manufactured and the initial tests have been successful. The second generation ISIS will be made on a smaller pitch, which will take it a step closer to satisfying the challenging detector requirements.

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