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DEPFET Active Pixel Sensors

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DEPFET pixels offer a unique possibility for a high resolution pixel vertex detector at a future linear collider (ILC) experiment. The key idea of DEPFET sensors is the integration of amplifying transistors into a fully depleted bulk. The excellent noise performance obtained through the low input capacitance in combination with the full signal from the depleted bulk leads to a large S/N ratio. The sensor itself can therefore be made very thin ($50\mu m$) without loss of efficiency. In this article the progress of the DEPFET development towards an ILC vertex detector is presented. Properties of prototype matrices and dedicated ASIC electronics have been characterized in various laboratory and test beam measurements. In particular a point resolution of less than 2 μm has been demonstrated (using 450 μm thick sensors). Based on these results larger matrices, improved readout and control electronics have been designed which are presently in production. In parallel software was developed to simulate the performance of a DEPFET based vertex detector in an ILC experiment.

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1. The DEPFET Sensor

1.1 DEPFET Principle and Operation

The DEPleted Field Effect Transistor structure (DEPFET) combines detection and amplification. The concept was proposed in 1987 [3] and developed to a level of maturity in the nineties [4–7].

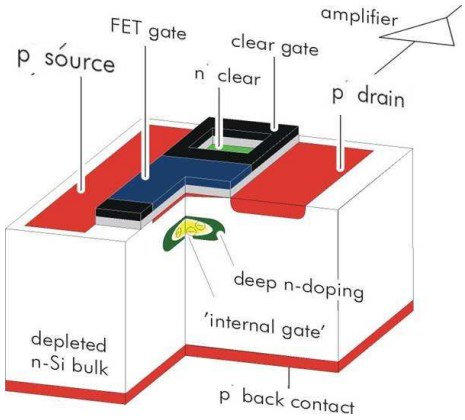

Figure 1: The DEPFET detector and amplification structure is based on a p-channel MOSFET structure on a completely depleted substrate. A deep n-implant forms a potential minimum for electrons which are collected there. The accumulated charge in this internal gate modulates the transistor current. The charge can be removed by the clear contact.

The DEPFET principle of operation is shown in Fig. 1. A MOS field effect transistor is integrated onto a fully depleted detector substrate. By means of an additional n-implant below the transistor a potential minimum for electrons is created underneath ($\approx 1\mu m$) the transistor channel. This can be considered as an internal gate of the transistor. A particle entering the detector creates electron-hole pairs in the fully depleted silicon substrate. The electrons are collected and stored in the internal gate. The signal charge changes potential of the internal gate, resulting in a modulation of the channel current of the transistor.

Low noise, even at room temperature, is obtained because the capacitance of the internal gate is very small, much smaller than the capacitance of standard hybrid pixel detectors of the same pixel area. The pixel delivers a current signal which is roughly proportional to the number of collected electrons in the internal gate. Signal electrons as well as electrons accumulated from bulk leakage current must be removed from the internal gate after readout. This clearing is performed by periodically applying a positive voltage pulse to a CLEAR contact. For individual pixel structures with full charge collection, the best noise value measured so far at room temperature is 1.6 electrons (see Figure 2). This noise value is obtained with $10\mu s$ shaping time and double correlated sampling.

In a real detector a single DEPFET pixel will be operated as follows:

- The DEPFET is switched off. In this state the transistor consumes almost no power, however, the pixel is sensitive to ionizing particles. Electrons generated by ionisation in the depleted bulk accumulate in the internal gate.

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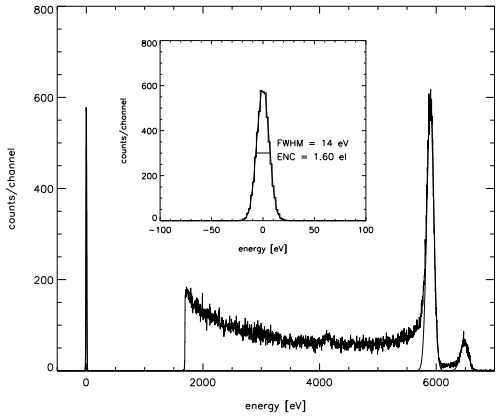

Figure 2: Fe^{55} spectrum obtained using a DEPFET single pixel. The rms noise of 1.6 e^- is obtained from the width of the pedestal, as shown in the insert.

- During a readout cycle a voltage (above the transistor threshold) is applied to the external gate, switching on the transistor. The source-drain current, composed of a pedestal current defined by the external gate and a signal current, proportional to the charge in the internal gate, is measured.
- A voltage is applied to the clear contact, removing completely the signal charge in the internal gate.
- Now the current is measured again, this time measuring the pedestal current. In an external readout circuit this pedestal is subtracted from the first reading, the difference giving the signal.
- The external gate voltage is set back, switching off the transistor.

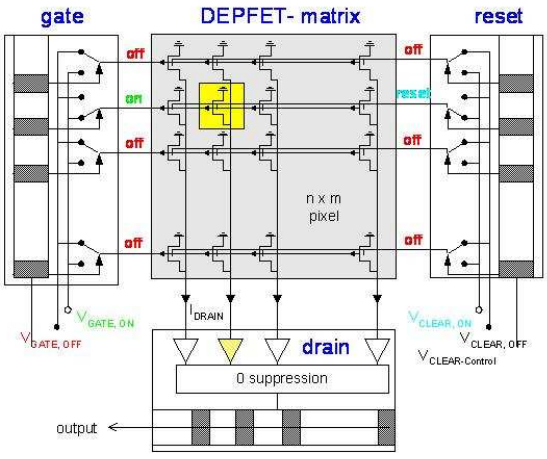

Figure 3: Schematics of a DEPFET matrix. Drains reading the current are connected column wise to a readout chip. Gates and clears are connected row wise to switcher chips. The switcher steps through the rows while all pixels of a row are read in parallel.

This sample-clear-sample cycle is planned to be as short as 50ns. In a pixel detector the pixels will be arranged in columns and rows (see Figure 3). All transistor drains of a column are connected to one amplifier node. The gate contacts and clear contacts are connected row wise, thus all pixels in a row can be read and cleared in parallel. In order to read out the matrix one row is switched on and all pixels of this row are read (sample-clear-sample cycle) in parallel. Then this row is switched off and the next row is read and so forth until all rows have been read and the cycle starts again.

In 2004 the first prototype DEPFET matrices were produced. The production (dubbed PXD4) was made on 450 μm thick high resistivity 6" FZ wafers. Double poly and double metal technology was introduced into the process line to build the complex DEPFET matrices with FET and clear gates and crossed contact lines. The largest matrices contain 64 $\times$ 128 pixels. The production contained several variants, e.g. using different clear structures.

2. The Readout and Control ASIC

As explained in the previous section two ASIC chips are necessary to operate a DEPFET matrix: Firstly a switcher chip which generates row wise the voltages needed to switch on the transistor and activates the clear. Secondly a chip reading out the current signal of all columns in parallel.

The SWITCHER chip is used to apply suited potentials for external gate and clear to the rows of the matrix. One SWITCHER can provide two voltages for 64 channels. An on-chip sequencer is used to connect the outputs to externally supplied voltages by means of simple analog multiplexers. Using high voltage transistors voltages of up to $25V$ can be switched. The chip operates at the required rate of 50 MHz. Several SWITCHER chips can be daisy chained.

Fast operation as required at the ILC was the major design goal for the CURO readout chip [8]. Therefore, signal processing (e.g. pedestal subtraction, signal storage and compare) on the chip is done in a current-mode operation perfectly adapted to the current signal of the DEPFET device. The chip performs correlated double sampling of the current values measured before and after clear suppressing the 1/f noise contribution of the sensor. The 128 channel chip offers the possibility of zero-suppression and sparse readout. All hits in a row are found by comparison to programmable thresholds. The analog amplitudes and the digital hit pattern are stored in a memory. The digital hit pattern is scanned by a fast hit finder. The addresses of the hits are stored in a RAM for later readout, the corresponding analog amplitudes are multiplexed to off-chip ADCs. The CURO chip has been fabricated using a $0.25\mu m$ process following radiation tolerant layout rules and should be sufficient radiation tolerant for use at the ILC. The analog part (double correlated sampling, current comparison) has been tested up to a row rate of $25MHz$. The intrinsic noise contribution of the sampling in the chip at this speed has been measured to be $100nA$. This is in disagreement with the calculated value (about a factor of two larger [8]). For the present DEPFET devices with a charge to current gain of up to $g_q \approx 400pA/electron$, this translates to a noise contribution of ENC$=$ 250 electrons. This problem could be traced to a wrong layout of the CURO's regulated cascode not matched to the drain capacitances.

Layer	Number of ladders	Radius (mm)	Ladder length (mm)	width (mm)	readout time
1	8	15.5	100	13	50 μs
2	8	26.0	2×125	22	250 μs
3	12	38.0	2×125	22	250 μs
4	16	49.0	2×125	22	250 μs
5	20	60.0	2×125	22	250 μs

Table 1: Default geometrical parameters of the DEPFET based ILC micro-vertex detector.

3. Layout of a DEPFET System for ILC

In our present concept we plan to use eight sensor modules in the inner layer, each 10 cm long and 1.3 cm wide. These eight modules cover the innermost radius of 1.5 cm with some overlap. Each module has 512 pixels (pitch 25 μm) in R-ϕ and 4096 along z. Readout is done from both sides, each side serving 512 $\times$ 2048 pixels. Due to the readout of two rows in parallel the effective row number per half is 1024, with 1024 readout channels. With 50ns readout time per (double-) row, a complete frame can be read in 50μsec, and 20 readout cycles can be performed during a bunch train of 1ms. In the outer layers background occupancy is less prominent and longer readout times and hence longer module dimensions are possible. A possible layout is described in Table 1, a view of the inner layer is shown in Figure 4.

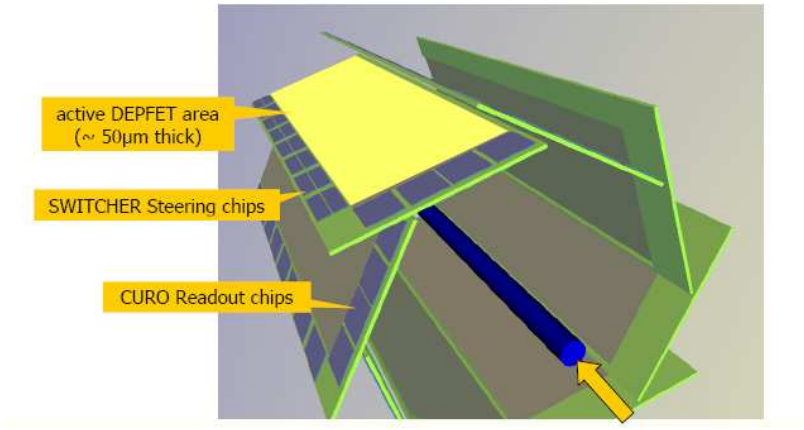

Figure 4: Artist's view of the innermost layer of the ILC vertex detector. Eight modules form the inner layer (one module per ladder). Each module is read out at both ends (only half of a module is shown). Along the module switcher chips control the gates and clears.

The module will be made out of one piece of silicon, thinned to 50μm in the active area surrounded by a 450μm thick silicon frame to provide mechanical stiffness. A gravitational sag of 20μm was measured with sample module [9]. The thinned switcher chips will be arranged along the module (on the thick frame) while the readout ASICs are on both module ends outside the acceptance. The technology needed to produce such an thinned module is described in [10]. Such a self supporting all silicon module would need no additional support material. In addition there is no CTE mismatch of different materials. Within the acceptance of the vertex detector

($|\cos(\Theta)| < 0.96$; ± 5 cm at R=1.5 cm) a material budget of 0.12% per ladder can be achieved including switcher chips and gold bumps.

The DEPFET has the inherent advantage that only during the readout sequence a pixel consumes power. In between readout cycles power consumption is almost zero. The power consumption of an active pixel is $500\mu W$ (for a drain current of 100 μA and 5V drain-source voltage). In an inner layer module 2×1024 pixels (two double rows) are active simultaneously, resulting in 1W per ladder. The two switchers chips switching the active rows consume 550mW, the remaining idle switcher chips 30×10mW, this adds to 0.85W. This includes the power needed to switch the gate and clear capacitances. One channel of the readout chip consumes 5mW, hence the 2048 channels total to 10.2W, the dominant contribution. Altogether an inner layer module consumes about 12W. The larger outer modules produce 21W per ladder. Hence the complete detector dissipates 1272W. Assuming that most of the active electronics can be switched off in the pause between the bunches the total power could be reduced by up to factor of 1/200. In the most optimistic case the complete detector could dissipate on average about 6.4W, suggesting that air cooling could be sufficient. However, power switching has not been demonstrated yet and may not be without problems. It should be stressed that most of the power is dissipated at the module ends, outside the acceptance, where additional cooling structures are less critical.

4. Test Results

4.1 Laboratory Test

Noise values as low as 1.6 electrons have been measured with linear, ILC like DEPFETs, albeit at long integration times (10 μs). The noise depends on the integration time τ like

$$ENC = \sqrt{\alpha \frac{8kTg_m}{3g_q^2}\frac{1}{\tau} + 2\pi a_f C_{tot}^2 + qI_{Leak}\Delta T_f} \tag{4.1}$$

The first term corresponds to the thermal noise of the DEPFET FET, α is a factor, appr. unity, depending on the exact shaping of the amplifier, g_m is the transconductance, g_q the charge amplification, and kT the thermal energy. The second term is the 1/f noise (with a process dependent normalisation factor a_f, C_{tot} the effective capacitance) and the third term is the shot noise due to the DEPFET leakage current I_{leak} accumulated during the frame readout time ΔT_f. Hence an increased noise is expected at a bandwidth of 50 MHz as needed at ILC. From calculations and extrapolations of the measurements obtained with long shaping times we expect that the intrinsic noise is well below 100 electrons at 50 MHz, dominated by the thermal noise. Unfortunately problems running a DEPFET/CURO system at high speed made it impossible to measure this noise directly. Therefore we used a single pixel with a high bandwidth amplifier (AD8015/AD8129 transimpedance amplifier with RC lowpass) to measure this intrinsic noise. Measured was the full sample-clear-sample mode, the noise values shown in Figure 5 are from fits to the width of the pedestal distributions. At full ILC speed the intrinsic noise of a DEPFET is still below 40 electrons.

In system tests and beam tests the best noise obtained was 250 electrons. As mentioned above the CURO is not optimized for the large drain capacitances. Further noise sources are pick up (internally in the CURO and of external amplifiers).

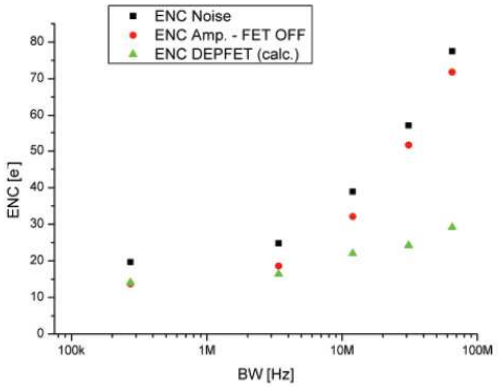

Figure 5: Noise of a DEPFET structure as function of the bandwidths of the readout node.

4.2 Radiation Hardness Tests

At ILC the vertex detector is exposed to radiation which could damage the device. Ionising radiation (γ, charged particles) leads to the creation of positive oxide charges at the $SiO_2 - Si$ interface. In FET transistors this leads to a shift of the threshold to negative values. In addition interface traps can reduce the mobility and hence the transconductance of the device. Bulk damage by NIEL (non ionising energy loss) from neutrons and charged hadrons (to a lesser extend also from electrons) leads to an increase of the bulk leakage current. Several irradiation tests with various particles were performed. The results can be summarized (Figure 6):

- Gamma irradiations were performed up to a dose of 913 krad, which exceeds by far the expected dose at ILC ($\approx$ 150krad in five years). A shift of the threshold voltage of $\approx 4V$ was observed which can be compensated. No other significant effects are observed.

- Neutron irradiations should lead only to bulk damage by NIEL. For doses up to $2.4 \times 10^{11} n/cm^2$ (1 MeV equivalent) no shift of the threshold voltage and no significant change of the subthreshold slope could be observed. A slightly increased noise at higher temperatures indicates additional shot noise due to higher leakage currents.

- Proton irradiation (up to $3 \times 10^{12} n/cm^2$, 1 MeV neutron equivalent) lead both kinds of damage. Threshold voltage shifts of 5 V were observed and an increase of the subthreshold slope indicates and increase of 1/f noise. g_m is reduced by 15%. The bulk damage leads to an increase of the shot noise which is proportional to the readout time of a complete matrix. For the planned readout cycle of $50\mu s$ the noise contribution would be 95 electrons. Cooling to 0^0C reduces this to 22 electrons. However, it should be kept in mind that the dose corresponds to about 35 years of ILC operation.

4.3 Test Beam Results

During 2005-2006 beam tests were performed at DESY and later at CERN. At the DESY beam test the main goals were a comparison of different DEPFET types, different operational settings, efficiency and purity studies, angular scans and an initial position resolution. One study made using

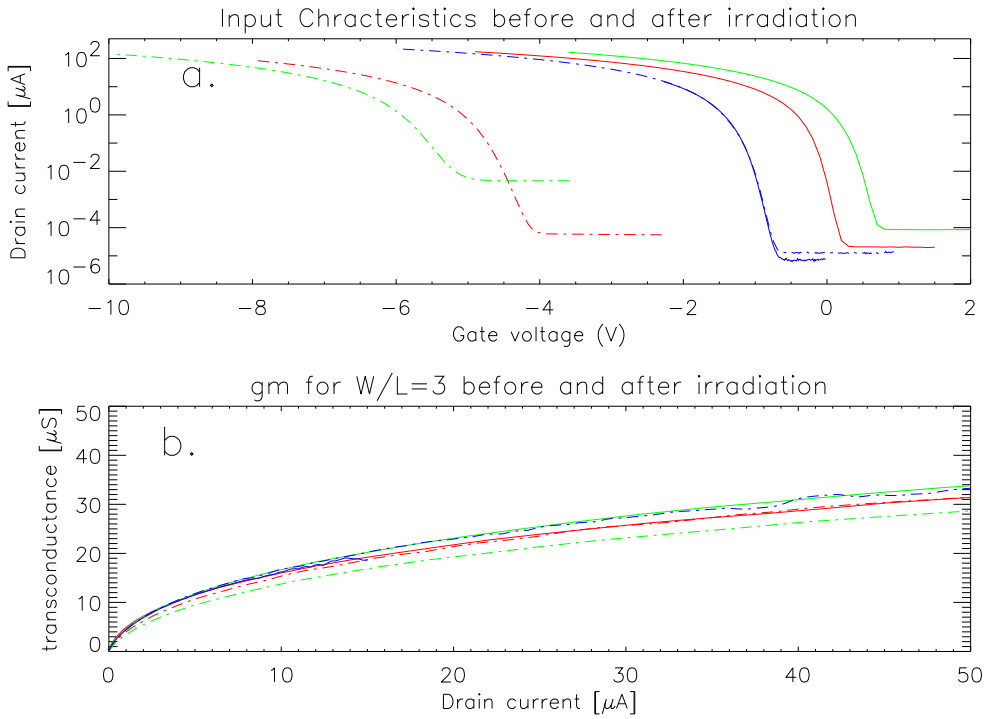

Figure 6: Transistor characteristics (upper figure) and transconductance (lower figure) of DEPFETs before (solid lines) and after (dashed dotted lines) γ (red), proton (green) and neutron (blue) irradiations.

DESY data was the dependence of the signal on the angle of incidence. Rotations around both the X-axis (ϕ) and the Y-axis (θ) were made, between 0 and 40^o. At large angles, tracks traverse the silicon underneath many pixels. Hence, the signal per pixel is very low. This allows the study of charge generation in thin layers and the charge collection directly underneath the DEPFET pixel where the field lines are non-trivial. These studies are very important for the tuning of the GEANT simulation for the 50 μm thick DEPFETs foreseen for ILC operation. The correspondence is excellent. These data provide a basis for the GEANT4 simulation of thin sensors.

At DESY, the electron beam energy is limited to 6 GeV. Due to multiple scattering and the limited precision of the telescope used, the uncertainty on the predicted position was limited to about 5-6 μm, larger than the expected intrinsic resolution of a DEPFET sensor. At CERN a high energy beam consisting of typically 180 GeV π's could be used. To improve the precision on the predicted position a telescope consisting of five DEPFET planes was built. The middle DEPFET is used as DUT while the others are used as telescope planes. The hit positions are reconstructed using an η-algorithm. The residual distributions are displayed in figure 7. This distributions are still preliminary including tracking and (small) multiple scattering errors and give an upper bound of the resolution. The RMS in direction with smaller pitch (22 μm) is 1.74 μm. In the other dimension with 36μm pitch the RMS is 3.77μm. Due to the design of the DEPFET pixels potential barriers between pixels are different in x and y, which could account for most of the difference of the resolution. Of course, this is for 450 μm thick sensors, the resolution of the 50 μm sensors will be worse (lower S/N, less charge sharing).

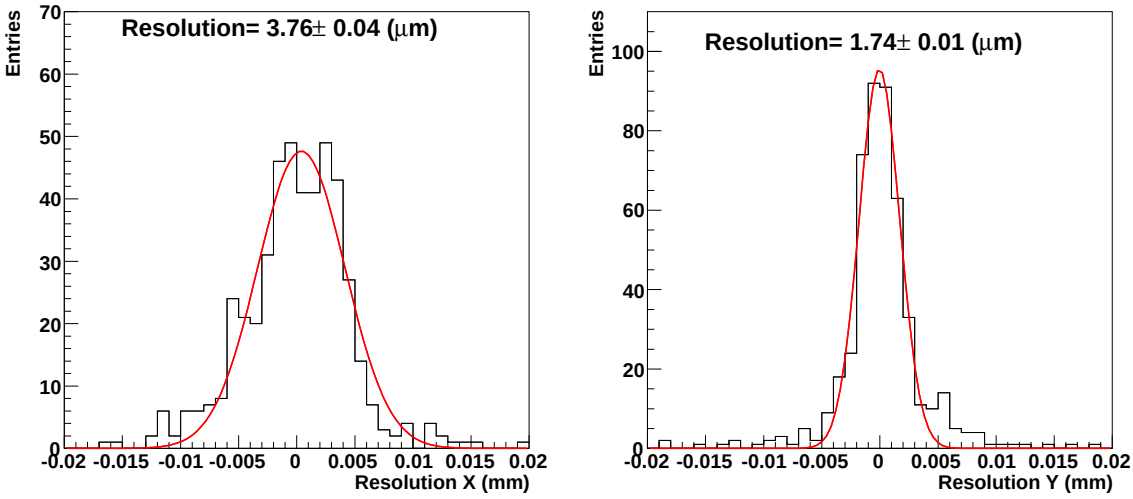

Figure 7: Residual width for a 36×22 μm (X×Y) DEPFET. The positions are reconstructed using the η algorithm.

5. MC Simulations

Simulation and reconstruction software is the key ingredient for the ILC detector optimisation and performance studies. Software tools allowing to perform detailed GEANT4 based modeling of particle interactions in a ILC detector and realistic signal digitisation accounting for specific properties of sensors are needed. To achieve this a detailed description of the DEPFET based vertex detector has been implemented in Mokka [11]. The geometry related parameters, namely the number of layers, the number of ladders in each layer, the geometrical parameters defining support frames, electronics, cabling etc, and the length, width and thickness of the active silicon wafers in each ladder are stored in a mySQL database. The simulation of particle interactions with the material of the micro-vertex detector has been complemented with the detailed DEPFET sensor response modeling implemented as a separate Marlin [12] module accounting for:

- fluctuation of energy loss along the particle trajectory within the active layer;
- diffusion of the released charge during its drift to the collection plane;
- Lorentz shift in the presence of the magnetic field;
- charge sharing across neighbouring pixels on the collection plane;
- electronic noise effects.

The simulation code has been tuned and validated using DEPFET beam test data taken at DESY in fall 2005. The validated software is used to study the performance of the DEPFET based ILC micro-vertex detector in terms of single point and impact parameter resolutions. Figure 8 demonstrates the single point resolution in $r-\phi$ as a function of the track polar angle for different thicknesses of the active sensor and pixel size. The noise is assumed to be 100 electrons, the silicon

thickness to 50 μm corresponding to a S/N of 40:1 (for comparison simulations with 75 μm thick silicon were done as well). Dead material like the reinforcement frames and ASIC chips and beam pipe is implemented. The $r-\phi$ impact parameter resolution as a function of particle momentum for normally incident tracks is also shown in Figure 8. The $r-\phi$ impact parameter resolution is well described by the relation

$$\sigma(IP_{r-\phi}) = a \oplus \frac{b}{p \cdot \sin^{3/2}\theta},$$

where p and θ are particle momentum and polar angle, respectively. The constant term is found to be $a \sim 4.5$ μm independent of the active silicon wafer thickness and a multiple scattering term b = 8.7(9.4) μm for the thickness of active silicon wafer of 50(75) μm. Thus, the DEPFET based vertex detector is expected to meet ILC requirements ($a < 5\mu$m, $b < 10\mu$m·GeV) [1]. It is worthwhile mentioning that the thicker silicon results in an improved point resolution due to a better S/N. However, the impact parameter resolution gets slightly worse due to multiple scattering. The simulations were done assuming a 4T magnetic field.

At the ILC, the micro-vertex detector will operate in severe beam background conditions. The primary source of the background are beamstrahlung photons which produce e^+e^- pairs hitting the vertex detector. Recent Monte Carlo studies showed that in the innermost layers of the vertex detector one should expect several hundred background hits per bunch crossing [2]. The total amount of accumulated background strongly depends on the readout speed. For the nominal set of the ILC machine parameters the expected number of background hits in the vertex detector per bunch crossing is about 400 in the inner layer. The impact of beam-induced backgrounds on the pattern recognition performance is quantified using a reference sample of the $t\bar{t} \rightarrow 6-jets$ at the centre of mass energy of 500GeV. Simulations have been done without background (scenario 1) or superimposing background hits corresponding to 75 (scenario 2, corresponding to 25 μsec frame readout time) and 150 (scenario 3, corresponding to 50 μsec frame readout time) interactions. Figure 9 shows the fake track rate and the track finding efficiency as a function of the transverse track momentum. The study emphasizes the importance of having a device with high readout speed, which would allow to minimize effects of beam-induced background. It should be noted at this point that this is not DEPFET specific and applies to any technology employed for the ILC vertex detector.

6. New Developments

6.1 PXD5 Pixel Production

A new production of DEPFET matrices, dubbed PXD5, started in 2006. After the proof of principle of the newly developed DEPFET technology in the first detector production PXD4 the first goal of PXD5 is to reproduce these features e.g. reliable transistor operation, radiation hardness, internal amplification, selective access within an array etc. In addition some parameters and dimensions are extended to values more relevant for ILC. Large 512 $\times$ 512 matrices address already the inner layer geometry of the ILC vertex detector. Wide format detectors with 1024 readout channels $\times$ 256 switcher channels (array size = 16.38 $\times$ 12.29 mm^2) are implemented to study the influence of long access lines (Gate, Clear) on the readout speed. For the other dimension very long arrays with 256 readout channels $\times$ 1024 switcher channels (array size = 3.07 $\times$ 49.15 mm^2)

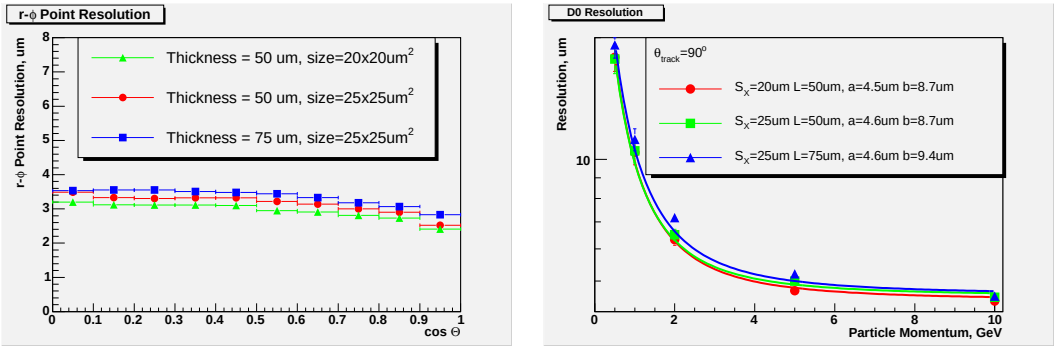

Figure 8: Left plot: The spatial point resolution in $r-\phi$ as function of particle polar angle θ. Right plot: the $r-\phi$ impact parameter resolution as a function of particle momentum for the polar angles θ=90^o.

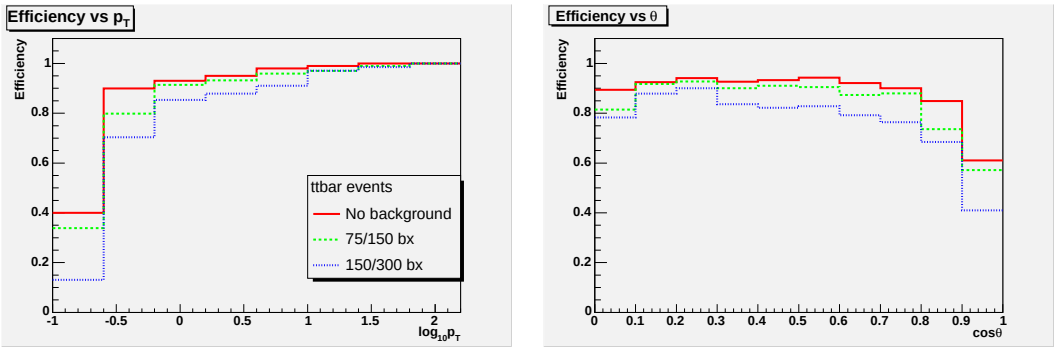

Figure 9: Track finding efficiencies as function of track transverse momentum (left plots) and polar angle (right plots). Solid lines corresponds to a no background scenario, dashed lines to the scenario characterized integrating 75(150) beam crossings and dotted line to the scenario integrating 150/300 beam crossings(see text).

are designed to measure the effect of the matrix input load on the readout chip. The pixel sizes vary from 32 $\times$24 μm^2 (as in PXD4), over 24$\times$24 μm^2 (base line) to 20x20 μm^2 (technology limit). Since the main noise contribution still comes from fast readout electronics an increase of the internal DEPFET amplification g_q transforms directly into S/N. The DEPFET offers a large scaling potential. As illustrated in Figure 10 g_q can be easily doubled by reducing the channel length from currently used 4.5 μm to 2 μm. This range will be investigated on test structures and small arrays.

PXD5 will be produced on high resistivity 6" FZ wafers of 450 μm thickness. Production finished in Summer 2007.

6.2 The New Switcher Chip

The existing Switcher can deliver high voltages (up to 25V) at the expense of high power consumption. The HV-CMOS process used is know to be not radiation hard, indeed, the device stops working after 30 krad. This choice was needed for the early prototype matrices when especially clear voltages needed for a complete clear were not known exactly. Now it is confirmed that maximally 10V are needed for a complete clear. Hence a new switcher chip (Switcher III) was de-

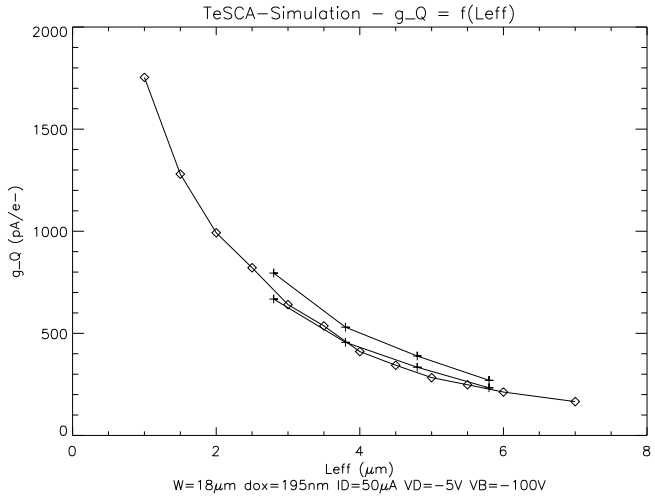

Figure 10: Dependence of the charge amplification g_q on the gate length. $\diamondsuit$: 2D TesCA simulation (50 μA drain current); $+$ measurements with 50 μA (lower) and 100 μA (upper) drain current.

veloped. It is a 128 channel chip in a radiation hard (0.35 μm) design. It can switch up to 10V with 4ns settling time. Compared to the previous chip its area is reduced, it needs less control signals and is prepared for bump bonding. The switching voltages of 10V is achieved by chaining three transistors, each switching maximally 3.3V [13]. The chip will fit well on the reinforcement frame of the DEPFET sensor. Test chips have been submitted and functionality and radiation hardness (up to 600 krad) has already been demonstrated [13]. A production of complete chips has been submitted.

6.3 The DCD1 Readout Chip

A new readout chip DCD1 (Drain Current Digitizer) has been developed which will overcome the shortcomings of the CURO which was designed for small matrices with low capacitance. In order to operate full size matrices the regulated cascode has been optimized for larger capacitances (about 40-50 pF for 5cm long columns). From simulations a noise of 34nA at 50pF is expected. An 8 bit, 16 MHz ADC is added to each channel. Data are sent out without 0-suppression. In test systems 0-suppression can be emulated using a FPGA. This will give a higher flexibility testing different 0-suppression and clustering algorithms. Power consumption should be 5mW per channel. The chip will be made in a potentially rad hard UMC 0.18μm technology and will read 144 channels. The connection to the DEPFET is done using an 18×8 array for bump bonding matching an fan-out structure integrated on the DEPFET sensor. The width of the chip is only 1.5mm, much smaller than the 1.8mm required for 144 lines of 12.5 μm pitch. Hence all chips servicing a DEPFET can be arranged in one row without staggering. A small 72 channel test chip has been submitted in March 2007.

7. Conclusions

Using DEPFET pixel sensors it should be possible to construct a vertex detector which fulfills the challenging requirements of ILC. Low noise, large signal at high readout speed have been

demonstrated with prototype detectors. The sensors are sufficiently radiation hard for ILC. Test beam measurements have shown very good spatial resolution. Detailed Monte Carlo studies show that the impact parameter resolution needed at ILC can be reached.

8. Acknowledgements

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