

Development of 3D detectors at FBK-irst

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We report on the development of 3D detectors at Fondazione Bruno Kessler - irst in the framework of the CERN RD-50 Collaboration. Technological and design aspects dealing with the 3D Single Type Column detectors are reviewed, and selected results from the electrical and functional characterization of prototypes are reported and discussed. A new detector concept, namely 3D Double-side Double Type Column detectors, allowing for significant performance enhancement while maintaining a reasonable process complexity, is finally addressed.

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1. Introduction

Ultra radiation-hard detectors are required for future high luminosity colliders. In particular, the foreseen upgrade of the Large Hadron Collider, i.e., the SLHC, will be able to reach a luminosity of $10^{35} \text{cm}^{-2} \text{s}^{-1}$, corresponding to equivalent hadron fluences up to 10^{16}cm^{-2} in the inner layers after five years of operation [1]. At such high fluences standard planar detectors can not survive: for a $300 \mu\text{m}$ thick planar detector, full depletion could not be achieved and, because of charge trapping, the device active thickness would be at most $50 \mu\text{m}$, so that the collected charge would be dramatically reduced. Due to their intrinsically radiation-hard structure, silicon detectors with three-dimensional electrodes (3D detectors) are one of the most promising technologies to cope with these very harsh radiation environments.

First proposed by S. Parker in 1997 [2], 3D detectors consist of an array of columnar electrodes of both doping types, oriented perpendicularly to the wafer surface (the 3rd dimension, whence the name "3D") and penetrating entirely through the substrate. Standard planar detectors have electrodes on top and bottom surfaces, so the depletion voltage depends on the substrate thickness and doping concentration. With 3D detectors the full depletion voltage can be orders of magnitude lower because the electrode distance is fixed by the inter-column pitch, that can be much smaller than the substrate thickness. Owing to the short lateral electrode distance and to the possibility to achieve high electric fields at low voltage, fast collection times (in the order of few ns) and high radiation hardness are obtained even after large particle fluences. In particular, electrodes can be placed at a distance comparable to the worst-case carrier drift length, so that a large charge collection efficiency is ensured. Considerable results have already been reported for these devices, among them a Charge Collection Efficiency up to 66% after irradiation with protons at $8 \times 10^{15} \text{1 MeV equivalent neutrons/cm}^2$ [3].

The remarkable advantages of 3D detectors over planar detectors are obtained at the expense of a higher electrode capacitance and a rather complex fabrication technology, which involves several non standard steps such as Deep Reaction Ion Etching (DRIE), wafer bonding (providing a sacrificial support wafer), and Chemical Mechanical Polishing (CMP) [4], so that a large scale production of such devices might be a critical issue. In this respect, modified 3D detector architectures allowing for a simplified fabrication technology are worth being investigated, and a few research laboratories are involved in this development [5, 6]. Among them, Fondazione Bruno Kessler - irst has developed 3D detector technologies since 2004 in the framework of the CERN RD-50 Collaboration. This activity has been supported by the Italian National Institute of Nuclear Physics under the "MEMS" agreement with the Autonomous Province of Trento and under the TREDI project of the National Scientific Committee V. As a first step toward the realization of full 3D devices, we have first proposed, fabricated and extensively tested a new 3D architecture, namely 3D Single Type Column (3D-STC) detectors [7], having columnar electrodes of one doping type only, which results in a much lower process complexity.

In this paper, the technology and design aspects related with 3D-STC detectors are reviewed and selected results from the electrical and functional characterization of prototypes are reported, highlighting pros and cons of this structure. Finally, the possibility to improve the detector performance while maintaining a reasonable process complexity by means of 3D Double-side Double Type Column detectors is addressed.

2. Technology and Devices

We have originally proposed the 3D-STC detector concept in [7]. Fig.1 illustrates the basic structure of the device with reference to its n^+ -on-p version, which should be preferred because of the advantages related to n-side readout. All the columnar electrodes are of the same type (n^+) and are etched from the front side of the wafer; p-stops or p-spray are used for surface isolation; on the back side a blank p^+ implant provides a uniform ohmic contact. The columns are empty and do not penetrate all through the substrate. As a result, there is no need for polysilicon deposition and for a support wafer. If compared to standard 3D detectors, the complexity is therefore largely reduced. Three batches of 3D-STC detectors with the same mask layout were fabricated at FBK-irst on high-resistivity p-type wafers of different characteristics: Czochralski ($300\mu\text{m}$ thick) and Float Zone ($500\mu\text{m}$ and $380\mu\text{m}$ thick). Since the DRIE equipment was not available at FBK-irst, this process step was performed at CNM Barcelona (Spain) for the first batch and at ESIEE (France) for the second and third batches. A maximum depth of $180\mu\text{m}$ was achieved for columns having a $10\mu\text{m}$ diameter (1:18 aspect ratio), but for most detectors the column depth is $150\mu\text{m}$. As an example, Fig.2 shows a Scanning Electron Microscope (SEM) image of a test wafer after the DRIE step.

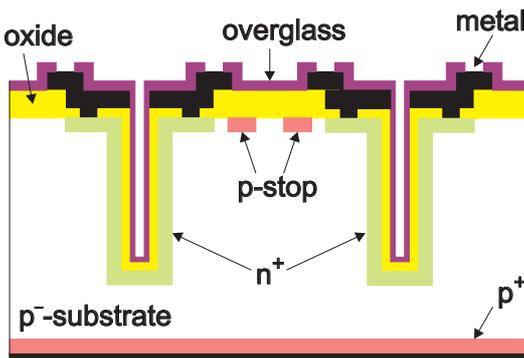


Figure 1: Cross-section of a 3D-STC detector.

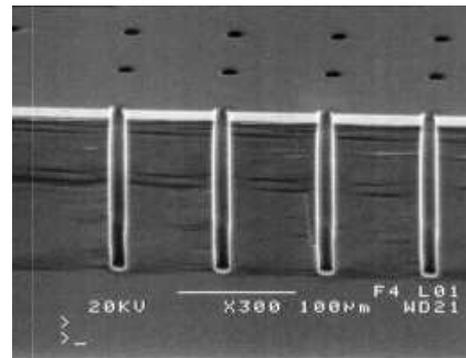


Figure 2: SEM image of a test wafer after DRIE.

The main features of the fabrication process are the following:

- Boron implantations are used to obtain the ohmic contact on the back side and the p-stop/p-spray surface isolation on the front side;
- circular columns with a typical diameter of $10\mu\text{m}$ are etched by DRIE using thick oxide and photoresist layers as a mask;
- n^+ doping of the columns is performed by Phosphorus diffusion from a solid source, and it extends to a circular region around the top of the holes to ease contact formation;
- after doping, columns are only partially filled with an oxide layer;
- contact openings are defined within the surface n^+ region surrounding the column hole, and aluminium sputtering is used for metal deposition;
- a low temperature oxide (LTO) layer is finally deposited (overglass).

The mask layout (see Fig. 3) includes mainly 3D detectors in the strip configuration, that can ease the electrical tests and the bonding to standard read-out chips for functional characterization. In strip detectors, all the columnar electrodes in one row are connected by the surface n^+ diffusion and/or by a metal strip, with a bonding pad at the end. Available designs differ by the following layout and process options: (i) two detector sizes, the first with 1.8 cm long strips and a total active area of 1 cm², the second with 1 mm long strips and a total active area of about 5 mm²; (ii) different pitches between columns, in the range 50 - 100 μm ; (iii) either DC or AC coupling between strip diffusions and metal layers; (iv) either p-stop (with different geometries) or p-spray for strip isolation at the surface. As an example Figure 4 shows a layout detail of a detector corner. The active area is surrounded by two frames of columnar electrodes acting as 3D guard-rings in order to shield the active volume from edge leakage currents. In AC-coupled detectors, strips are biased by punch-through at both their edges from the inner guard ring, used as a bias ring. The same mechanism can be exploited for test purposes in DC-coupled detectors.

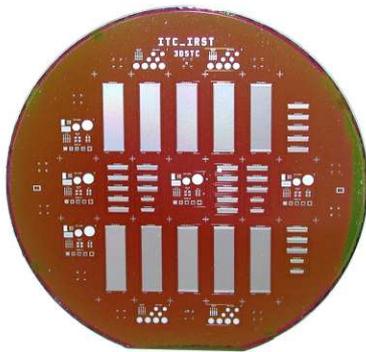


Figure 3: Photograph of a 3D-STC processed wafer.

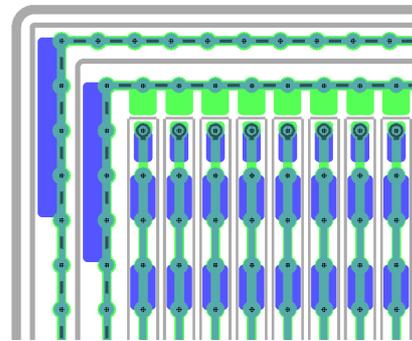


Figure 4: Layout detail of a strip detector.

The mask layout also contains planar test structures (e.g., diodes, MOS capacitors, gated diodes) aimed at monitoring the main process parameters and 3D diode test-structures (both single-column and multi-column arrays), which are a very important test vehicle since they allow for a more straightforward comparison between measurement data and simulation results.

3. TCAD Simulations

The behavior of the 3D-STC detectors in terms of the static electrical characteristics and of the signal response to minimum ionizing particles was investigated by means of numerical device simulations, performed with the software ATLAS by SILVACO [7]. Due to the peculiar detector structure, a three-dimensional simulation domain is needed, corresponding to a basic cell including four columnar electrodes (see Fig. 5a).

From simulations, insight is gained on the depletion mechanism, that first proceeds sideways between columns and then backwards from the column tips to the ohmic contact like in a planar detector. Notably, once full depletion between columns is achieved, the electric field strength in the inter-column region can not be increased further by increasing the reverse voltage, and its value depends on the substrate doping concentration only. As a consequence, low field regions exist in the middle of a cell (see Fig. 5b and Fig. 5c), which of course affect the charge collection mechanism.

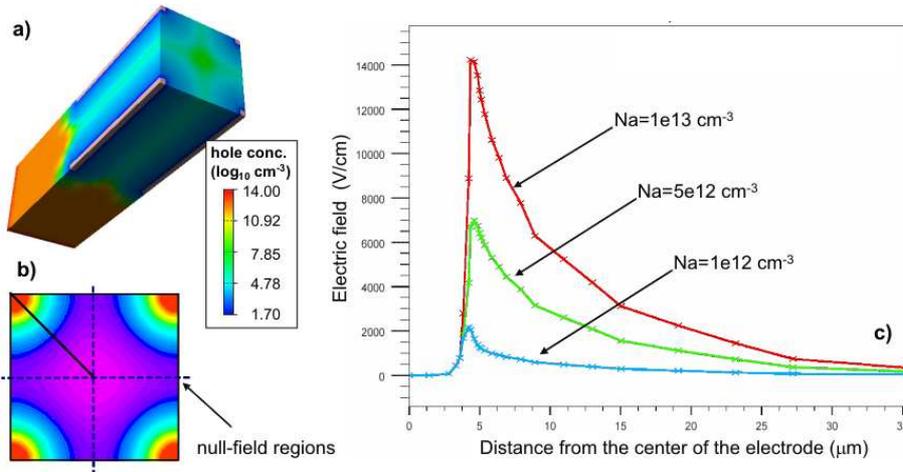


Figure 5: a) Three-dimensional simulation domain, showing hole concentration at 5V reverse bias; b) two-dimensional cross section parallel to the detector surface showing electric potential at 15V reverse bias; c) electric field along a cut-line from the center of the electrode to the center of the cell at three different substrate doping concentrations.

As an example, Fig. 6 shows the current signal induced on Electrode-1 by a uniform (mip-like) charge released along three tracks at different distance from the electrode. Signals feature: i) a fast peak component (in the order of a few ns), due to electron and hole horizontal drift towards the electrode and the center of the cell, respectively. As can be seen, the peak is delayed as the track is moved from the column to the center of the cell, because of the lower field value; ii) a slow tail component (in the order of few μs), independent of the track position, due to hole diffusion/drift to the back side (note that a high-field region can be present only below the column tips). Thus, we can conclude that 3D-STC structures are not expected to yield a uniform response to particles and to be as radiation hard as standard 3D detectors. Further details on the signal formation can be found in [8].

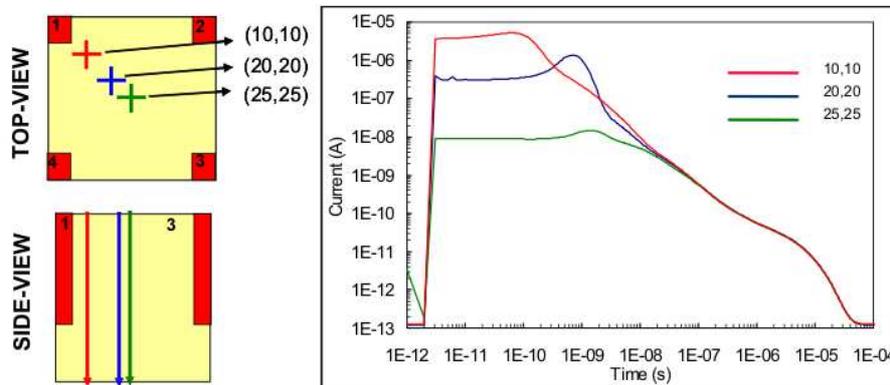


Figure 6: Simulation of the current signal induced on Electrode-1 by a uniform (mip-like) charge deposition along three different tracks. A sketch of the simulated cell showing the track positions is also shown.

4. Experimental Results

Devices from three batches were extensively tested on a probe-station with current-voltage and capacitance-voltage measurements. Experimental results relevant to test structures and strip detectors are reported in [9] and [10], respectively. In the following, we discuss the main electrical figures with respect to the parameters measured on strip detectors, that are summarized in Table 1.

Parameter	Unit	p-stop	p-spray
Lateral depletion voltage (between columns)	[V]	5 - 30	5 - 30
Substrate full depletion	[V]	> 30	>30
Total leakage current (bias ring) at lateral depletion voltage	[nA]	5 - 25	5 - 10
Breakdown voltage	[V]	100 - 200	40 - 120
Interstrip capacitance at lateral depletion voltage	[pF]	4 - 6	5 - 7
Single strip capacitance vs backplane at lateral depletion voltage	[pF]	< 5	< 5

Table 1: Typical range of the main electrical parameters measured on large strip detectors (1cm^2) from three different 3D-STC batches.

Lateral depletion between columns is achieved at low voltages in the range from 5V to about 30V, according to the pitch and to the substrate resistivity. The leakage current is very good: if normalized by the number of columns, the typical values are well below 1pA/column, evidence for a good process quality. Junction breakdown always occurs at the surface, as confirmed by the fact that the breakdown voltage is the same for planar and 3D test structures. The measured values are quite good for p-stop isolation, whereas for p-spray some detectors feature early breakdown at about 40V, since the p-spray doping profiles are not yet optimized in this technology. This problem prevented from reaching substrate full depletion in some detectors. As expected, the interstrip capacitance is much larger than in planar detectors, because of the stronger coupling between columnar electrodes. The capacitance versus the backplane is proportional to the area and scales with the depletion depth below the column tips in a planar-detector-like fashion [9].

Selected samples of pad and strip detectors from the three 3D-STC batches were delivered to a few groups belonging to the RD-50 Collaboration to the purpose of performing functional tests.

The signal dynamics was investigated at JSI Ljubljana by means of position sensitive multi channel Transient Current Technique (TCT) on small strip detectors. Three adjacent strips were connected to fast current amplifiers and the signal induced by fast 1060 nm laser pulses ($\sim 1\text{ns}$) was monitored as a function of the position of the beam, having a diameter in silicon of about $7\ \mu\text{m}$ FWHM and a resolution of $0.5\ \mu\text{m}$. Fig. 7 shows the TCT current signals induced on the central strip for two different beam positions: when the beam is focussed close to the read-out strip (Fig. 7a), the signal shows a very fast component and a long tail due to hole diffusion, in good agreement with device simulations; when the beam is focussed close to a neighbor strip (Fig. 7b), a bipolar signal with a high fast component can be observed. This is typical of the non collecting electrodes also in planar detectors, but in this case a much larger signal is obtained, which could actually be exploited to increase the position resolution by charge sharing and can contribute to increase the signal/noise ratio. Further details can be found in [11].

Charge Collection Efficiency (CCE) tests were performed with IR laser sources. Position resolved CCE measurements were carried out at the University of Freiburg to study the dependence

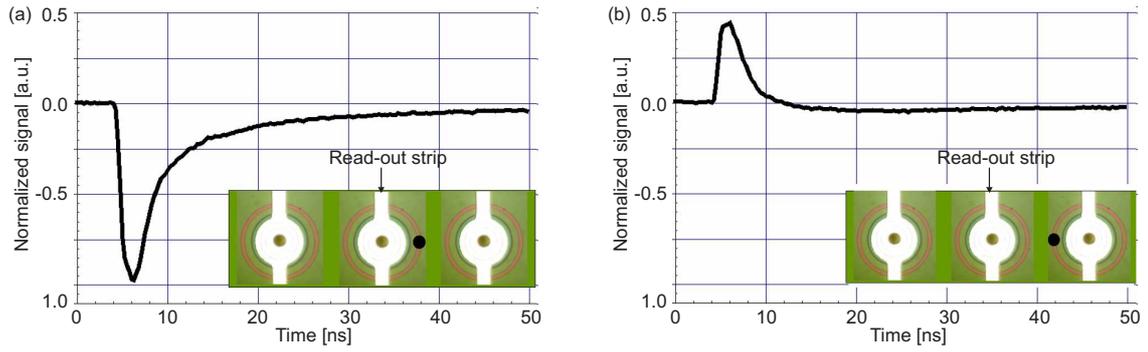


Figure 7: TCT signals induced on the central strip by 1060 nm laser pulses with the beam focused (a) close to the strip, and (b) close to the right neighbor strip, as indicated by the black spots.

of the charge collection on the position of light incidence. A 982 nm laser is used, having a light spot diameter of 4-5 μm and a pulse width of 2 ns, synchronized with the DAQ, which features the ATLAS SCT binary readout, operated at 40MHz and with a peaking time of 20 ns for the front-end. The sensor can be moved in the x-y plane with motorized stages with μm accuracy [12, 13]. As an example, Figure 8 shows the signal map over one basic cell of the detector at two different bias voltages. Lateral depletion between columns occurs at 22V: at 18V a large region with low CCE is present, but due to the low-field region also at 30V a row with reduced signal, parallel to the strips and about 4 μm wide, can still be observed. The reduced signal region is further extended after irradiation because of the concurrent effect of trapping [14]. Moreover, other TCT studies performed at JSI Ljubljana evidenced that the CCE can drop to low values ($\sim 40\%$) also for the regions close to the columns after irradiation with neutrons at 5×10^{14} 1 MeV eq. n/cm² and that the detector is not working after 5×10^{15} 1 MeV eq. n/cm² [15].

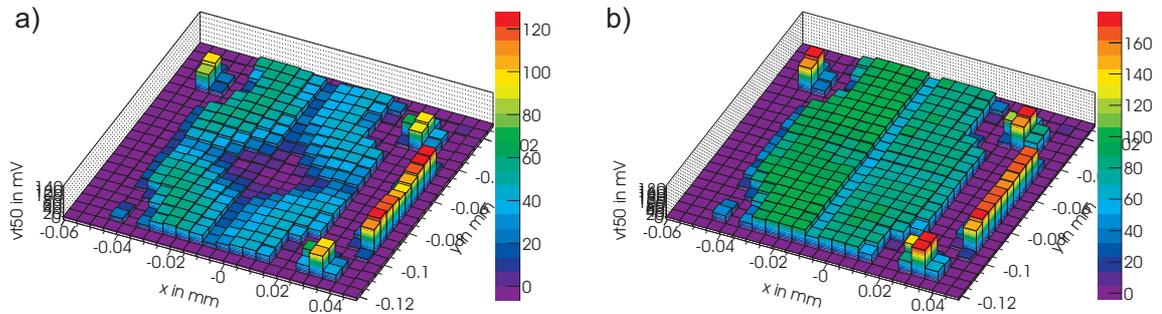


Figure 8: Output signal map over one basic cell of a detector as measured with the ATLAS SCT binary readout in response to 982 nm laser pulses: a) $V_{bias}=18\text{V}$, b) $V_{bias}=30\text{V}$.

CCE tests with Sr^{90} β sources were performed on pad detectors at INFN Florence and on strip detectors at SCIPP and Freiburg. A comparison between the results achieved in pad detectors with analog DAQ and strip detectors with binary DAQ is reported in [16], showing the same dependence of the collected charge with the bias voltage, in agreement with the simple picture of the depletion, i.e., with a rapid depletion between columns and a slow, planar-diode like depletion beyond that. The importance of the ballistic deficit is highlighted in Fig. 9, which compares the median collected

charge in detectors of differing thicknesses (but with the same column depth) read-out with binary DAQs featuring different peaking times. As can be seen, much more charge is collected in detectors read-out with 100 ns peaking time. Ballistic deficit rather than carrier trapping is also found to be the dominant effect after irradiation with 26 MeV protons to a fluence of 9.1×10^{14} 1 MeV eq. n/cm²: no degradation in the collected charge is indeed observed provided that lateral depletion between columns is achieved, which of course requires a much larger bias voltage (~ 300 V) after irradiation [17].

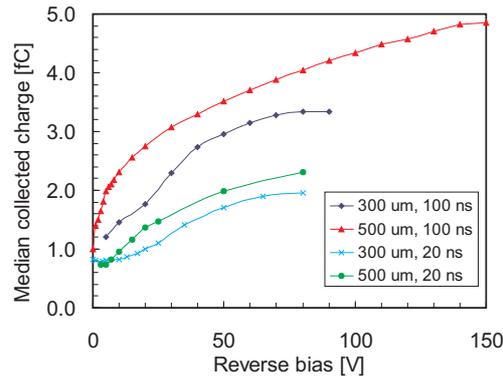


Figure 9: Median collected charge vs reverse bias in AC-coupled strip detectors of different thickness read-out with binary DAQs featuring 20ns and 100ns peaking times.

5. Concluding remarks and future perspectives

We have reported on the development of 3D detectors at FBK-irst. The first device produced, namely the 3D-STC detector, allows for a simple, high-yield fabrication process, and has been a very important step to learn aspects of the technology and to gain insight into the 3D operation. Nonetheless, as also confirmed by simulations, the charge collection mechanism is not very efficient due to the presence of low-field regions, so that a different detector concept is necessary for fast charge collection, which is a must in heavily irradiated sensors. To this purpose, we have developed a new detector concept, namely the 3D Double-side Double Type Column (3D-DDTC)

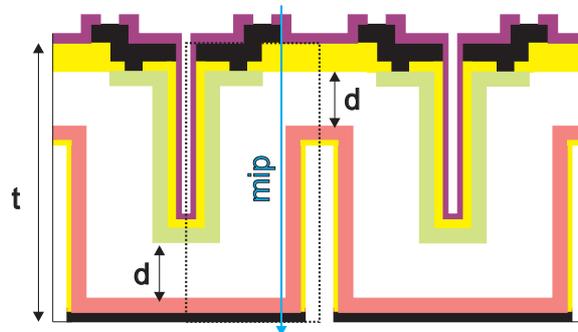


Figure 10: Cross-section of a 3D-DDTC detector.

detector, which is expected to significantly enhance the performance with acceptable process complication. Fig. 10 shows the cross-section of the proposed device, where columns are etched by DRIE from both wafer sides (junction columns from the front side and ohmic columns from the back side), stopping at a distance d (ideally not exceeding a few tens of μm) from the opposite surface. This results in an easier masking of the DRIE etching. Moreover, since columns are not etched all through the substrate, a sacrificial wafer is still not required. The process is indeed the same as in the 3D-STC technology for the front side, whereas on the back side lithography and DRIE have to be added. For these detectors, simulations predict a performance comparable to standard 3D detectors also after irradiation, provided that d is much lower than the wafer thickness (t). As an example, Fig. 11 shows the simulated signals induced by a minimum ionizing particle hitting close to the ohmic column (i.e., in the worst-case situation) in a n-on-p detector with $d = 25 \mu\text{m}$ and $t = 250 \mu\text{m}$, irradiated at $1 \times 10^{16} \text{ 1 MeV eq. n/cm}^2$ for different bias voltages (note that the lateral depletion voltage is 400 V).

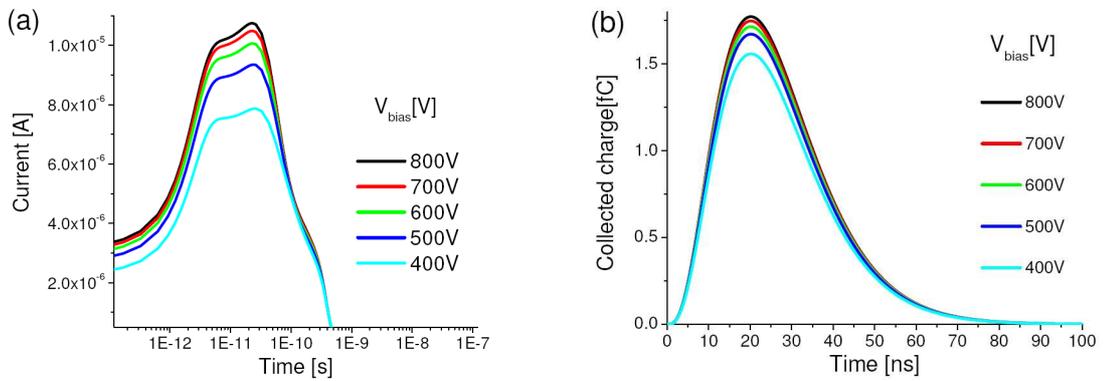


Figure 11: Simulated transient signals in response to a mip hitting close to the ohmic column in a 3D-DDTC detector irradiated at $1 \times 10^{16} \text{ 1 MeV eq. n/cm}^2$ for different bias voltages: a) current signals; b) equivalent charge signals at the output of a semigaussian CR-(RC)³ shaper with 20 ns peaking time.

Radiation damage is included in the simulations by using the effective doping concentration, (i.e., $2 \times 10^{14} \text{ cm}^{-3}$, calculated assuming an acceptor introduction rate of $2 \times 10^{-2} \text{ cm}^{-1}$ [18]), and by accounting for carrier trapping with the trapping times reported in [18]. Current signals (see Fig. 11a) are filtered with a semigaussian CR-(RC)³ function with 20 ns peaking time (see Fig. 11b) to account for a fast read-out (SLHC compatible). As can be seen, the collected charge exceeds 1.5 fC already at 400 V, corresponding to a CCE of about 48%, that is a very good result for this worst-case situation, and can be further increased by increasing the bias voltage.

Two batches of 3D-DDTC detectors were fabricated at FBK-irst on both n-type and p-type substrates. Preliminary results from the electrical characterization of the first prototypes (p-on-n) are quite promising, showing very low depletion voltage and leakage current, and also the n-on-p detectors will be available soon [19].

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