Development of Monolithic Pixel Sensors for the Linear Collider Vertex Detector

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This paper reviews the on-going R&D on Monolithic Active Pixel Sensors for charged particle tracking in the vertex tracker of an e^+e^- linear collider. The stringent requirements in terms of granularity, material budget and readout speed drive efforts along different directions which are being pursued worldwide. Recent achievements and future directions of these activities are reported.

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1. Introduction: requirements of the ILC Vertex Tracker

A linear collider will collide electrons and positrons with high luminosity at center-of-mass energies from $\simeq 0.25$ TeV up to 1 TeV, using supeconducting RF cavities as the proposed International Linear Collider (ILC) [1], or possibly several TeV, using novel beam acceleration techniques as in the CLIC scheme [2], providing a facility with characteristics complementary to those of the Large Hadron Collider (LHC). By colliding point-like particles with precisely tuned collision energy and beam polarization, the linear collider will enable precision studies of the Higgs sector and the mechanism of mass generation, to carefully identify the nature of New Physics beyond the Standard Model and probe its connections to Cosmology. An important part of this physics program relies on excellent flavor tagging capabilities in multi-jet events and on the determination of quark charge. This translates into an excellent accuracy in extrapolating particle tracks to their production point. The anticipated requirement of a resolution better than $\left(5 \oplus \frac{10}{p\sin^{3/2}\theta}\right)\mu m$ calls for a vertex tracker of unprecedented performance, with single point resolution $\lesssim 3$ μm and material budget of $O(10^{-3})$ X_0 per layer. This translates into thin (~ 50 μm) layers of high granularity (~ 20 μm pitch) silicon pixel sensors. Figure 1 shows as an example the impact parameter resolution obtained from the simulation of $e^+e^- \rightarrow ZH$ events at 500 GeV with a vertex detector meeting these requirements.

The readout architecture is driven by the rate of the machine-induced background, mostly due to incoherent e^+e^- pair production in the strong field of the two colliding beams [4]. These low-momentum pairs spiraling in the solenoidal field of the detector are responsible for an hit density estimated at $\simeq 5$ hits/cm^2 per bunch crossing at a radius of 15 mm for a magnetic field of 4 T. Figure 2 shows the expected background hit rate as a function of the radial position for different integration times. If we consider the ILC beam structure, which consists of ~ 3000 bunch
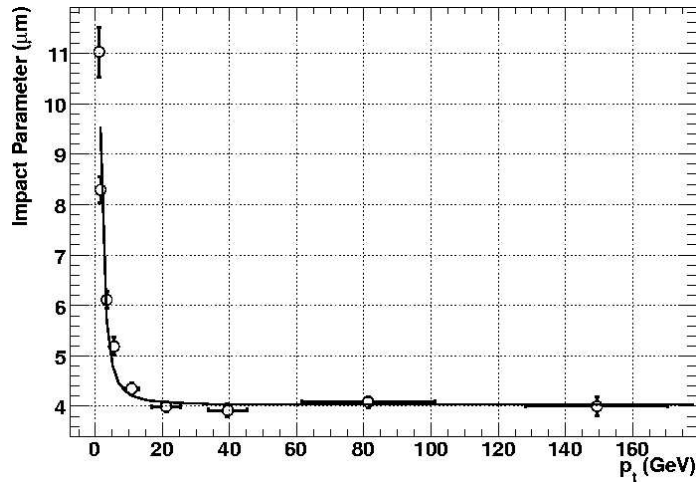

Figure 1: Impact parameter resolution as a function of track momentum obtained from Geant-4 simulated $e^+e^- \rightarrow ZH$ events at 500 GeV after full reconstruction and tracking using the Mokka and Marlin [3] packages. The simulation includes a 5-layered vertex tracker with 17 μm pitch pixels providing a single point resolution of 2.5 μm; the material budget per layer is 0.1% X_0, and the layers are equally spaced between R=15 mm and R=60 mm.
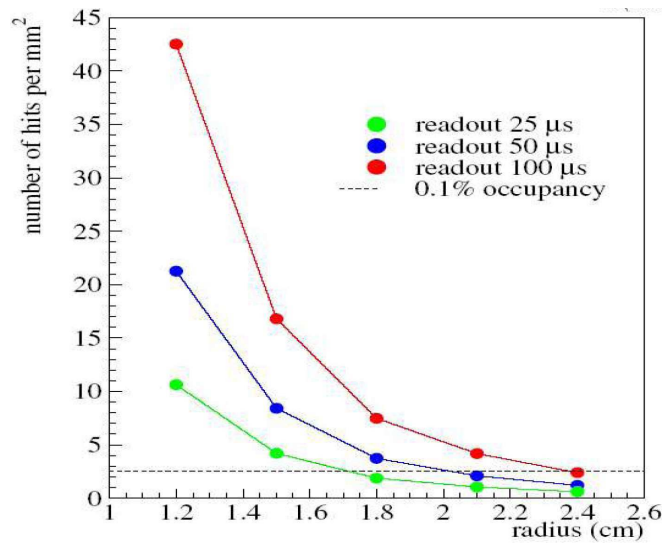
Figure 2: Expected background hit rate in the ILC Vertex Tracker as a function of the radial position and for different integration times. The rates have been calculated assuming 5 hits/cm^2/bunch crossing (from [5]).

crossings in a ∼1 ms long bunch train at a repetition rate of 5 Hz, pixels of 20 μm pitch, read out with an integration time of 50 μs result in an occupancy at the few % level. Keeping the occupancy low requires an integration time as short as 25 μs, which sets the requirement for the necessary readout speed of the pixel technology. Backgrounds are also responsible for the dose delivered to the sensors. The low-energy (∼10 MeV) pairs result in an ionizing dose of 50 krad/year and in a 1 MeV neutron equivalent fluence of $6 \cdot 10^{10}$ n_{eq}/cm^2/year [6].[†] Neutrons produced by beamstrahlung photons, e^+e^- pairs or radiative Bhabhas hitting the detector or the beam delivery system are expected to contribute an integrated fluence of the order of 10^{10} n_{eq}/cm^2/year [7].[‡]

The low material budget translates into the requirement of low power dissipation to minimise the material burden of the cooling system. Finally, the readout architecture must be proven robust against electromagnetic interference (EMI) [8]. The low beam duty cycle of 0.5% can be exploited by power cycling the detector and thus reducing the average power dissipation. At the same time, EMI effects could be avoided by locally storing the charge signals during the bunch train, and reading them out during the 199 ms long beam-off periods.

Hybrid pixel detectors of the type adopted by the LHC experiments are not applicable at the linear collider vertex detector due to their large pixel size and excessive thickness. The linear collider, with its emphasis on accuracy and the modest requirements in terms of radiation hardness, will accept sensors of new design, thus motivating an R&D stream complementary to that for the LHC and its upgrade. Several technologies are being considered, such as Charge Couple Devices (CCDs) [9] and DEPFET pixels [10]. CMOS Monolithic Active Pixel Sensors (MAPS) are an attractive option, since they combine a very high-granularity sensor with its readout electronics on the same silicon substrate. Since the sensitive volume is typically limited to a (∼10 μm) thin epitaxial layer, detector chips can be back-thinned to 50 μm and below without sacrifice in perfor-

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[†]The values include a safety margin of 3-5 with respect to the Monte-Carlo predictions.

[‡]The value given takes into account a safety margin of 10 with respect to the Monte-Carlo predictions.

mance. Finally, the use of readily available, commercial CMOS processes ensures low production costs while profiting of the trend towards decreasing feature size.

This paper is organized as follows. Section 2 describes the principle of operation of MAPS and summarizes the achievements of earlier prototypes; Sections 3 and 4 report the on-going R&D efforts for the ILC Vertex Detector. Sections 5 and 6 discuss the opportunities offered by emerging, alternative CMOS technologies while outstanding issues in detector system integration are addressed in Section 7.

2. Monolithic Active Pixel Sensors: principle of operation and early prototypes

CMOS imagers, which are the inspiration for Monolithic Active Pixel Sensors (MAPS), are an increasingly attractive alternative to CCDs for visible light imaging. Their advantages over CCDs are in the possibility of using commercial CMOS manufacturing processes, which bring down fabrication costs, in the lower power dissipation and in the possibility of integrating more advanced functionalities on the same sensor substrate. On the other hand, they suffer from a relatively poor fill factor, or the fraction of the pixel area sensitive to radiation. MAPS became applicable for particle tracking in high energy physics when a new pixel structure was proposed [11]. The principle of operation is shown in Figure 3 together with a cross-section of the proposed device. This was designed to be fabricated in a standard, double-well bulk CMOS process with a moderately doped epilayer grown on top of a low-resistivity substrate. The charge generated by an ionizing particle is reflected by the potential barriers due to the doping differences at the epitaxial layer boundaries, and is collected at a diode formed by the junction between the *n*-type well and the *p*-type epitaxial layer. Since the charge moves by thermal diffusion in the nearly field-free epitaxial layer, the collection times are of the order of 100 nsec. A first signal amplification is achieved on pixel, with a source-follower transistor implanted in the complementary *p*-well. In the simplest readout architecture, the pixel level is sampled twice, after an initial reset, with a delay defining the integration time. By subtracting the reset level, fixed pattern noise and leakage current can be removed, a technique referred to as Correlated Double Sampling (CDS).
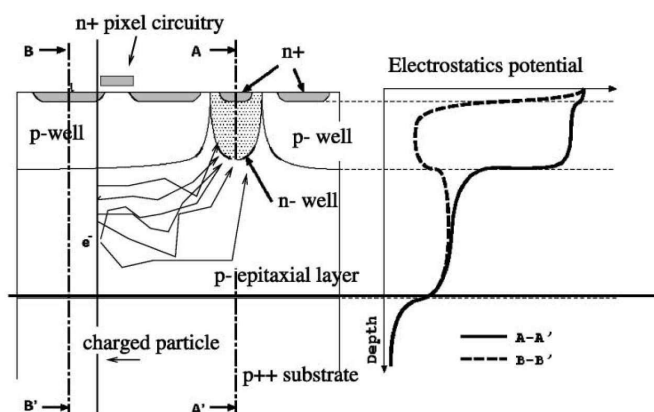

Figure 3: Schematic illustration of the principle of operation of Monolithic Active Pixel Sensors (from [12]).
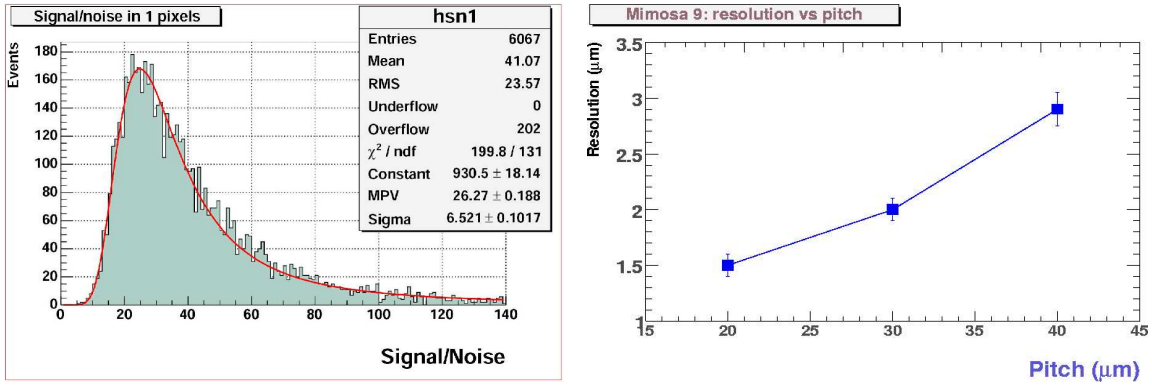
Figure 4: Test results of the MIMOSA-9 prototype from IPHC, Strasbourg. Left: signal-to-noise distribution in one pixel for 120 GeV pions. Right: single point resolution as a function of pixel pitch. Both plots refer to measurements performed at a temperature of $0°$C (from [13]).

Since the sensitive volume is limited to the 10-15 μm-thin epitaxial layer, the low-resisitivity substrate can be removed with a back-thinning process without altering the charge collection properties (see Section 7) and the MAPS technology lends itself well to the fabrication of thin sensors. On the other hand, such a thin sensitive volume yields charge signals of the order of ~1000 electrons, and therefore only moderate signal-to-noise performances when comparing to standard high-resistivity, reverse-biased silicon detectors. Moreover, the almost complete lack of electric field in the collection volume leads to a significant spread of the charge carriers among several neighboring pixels.

The development of MAPS sensors was pioneered by the IReS (now IPHC) group in Strasbourg with the design and characterization of several generations of chips in the MIMOSA series, which explored different pixel designs, sensor architectures and CMOS fabrication processes. So far the best performance in terms of signal-to-noise ratio has been obtained with the AMS 0.35 μm OPTO technology which features a 14 μm thick epitaxial layer. The sensor tracking performances have been extensively tested in beam tests with 120 GeV/c pions at CERN and with 6 GeV electrons at DESY. Signal-to-noise ratios up to 20-30 have been obtained, with equivalent noise figures between 10 and 20 electrons. These results could be reproduced on several chips at operating temperatures up to room temperature and above. Detection efficiencies >99% were measured, and single point resolutions of 1.5-3 μm for pixel pitches of 20-40 μm could be achieved [13] by using analog readout and cluster charge interpolation (see Fig. 4). Similar performances have been obtained on a reticle-size prototype, the MIMOSA-5 chip [14], featuring more than 1 million pixels arrayed on a 17 μm pitch for a total active area of 3.5 cm^2.

The radiation hardness of MAPS devices produced with different CMOS processes has been tested using both ionising and non-ionising radiation. Neutron irradiations have shown the occurrence of charge losses and decrease of efficiency after an integrated fluence of 10^{12} n_{eq}/cm^2 [15]. Irradiation with 10 MeV electrons showed a significant decrease of the sensor performance after an integrated fluence of 10^{13} e$^-$/cm^2. Nevertheless, good signal-to-noise values and detection efficiencies >99% could be recovered by cooling the device to temperatures below -10$°$C [13]. Tolerance to ionizing radiation up to a dose of 1 Mrad has been achieved with an improved pixel layout [16].

In recent years, other groups have joined the development effort on MAPS devices, in Europe and in the US. These activities are aimed at the optimization of the readout architecture for the ILC, for a possible use at a high luminosity *B* factory but also for applications beyond particle physics. Different options are being investigated which include analog architectures with fast readout and integrated functionalities like in-pixel CDS, on-chip digitization or discrimination and binary architectures relying on more complex capabilities like in-pixel time-stamping. MAPS sensors find applications in fields outside HEP, most notably in electron microscopy [17] and nuclear science experiments. The upgrade of the STAR vertex detector [18] and the innermost tracking region of the Compressed Baryonic Matter (CBM) experiment at the future Facility for Antiproton and Ion Research (FAIR) [19] will be equipped with CMOS monolithic pixels. Other potential applications of these sensors cover a very broad range from medical imaging to beam diagnostics.

3. MAPS with integrated functionalities and fast readout

The first way to cope with the high occupancy levels from the machine-induced pair background expected at the position of the innermost detector layers at the ILC is to read out the sensor multiple times during the 1 ms bunch train. The architecture that best serves this purpose is a fast column-parallel readout, in which all columns are read out synchronously, and analog to digital converters, or discriminators, are integrated at the end of each column followed by further integrated signal processing electronics such as circuitry for data sparsification and memory for data buffering.

A readout architecture based on a binary output simplifies the data processing and sparsification in a vertex tracker consisting of almost 1 billion channels, since only pixel addresses need to be output. However, it has to achieve a high granularity in order to preserve the required position resolution, limited to $p/\sqrt{12}$, where p is the pixel pitch. The first successful prototype featuring a fast column-parallel architecture with a binary output was the MIMOSA-8 chip from DAPNIA,
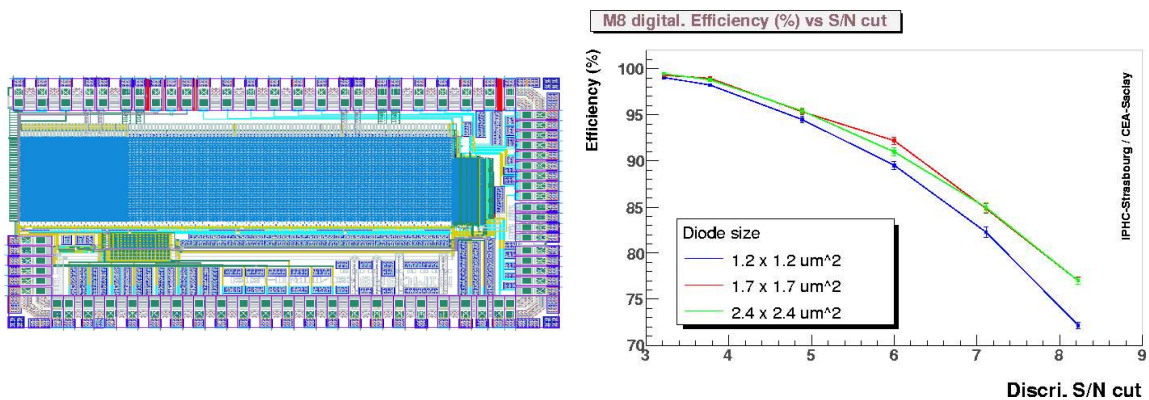

Figure 5: Left: layout of the MIMOSA-8 chip from DAPNIA, Saclay and IPHC, Strasbourg. The array of 32×128 pixels is subdivided into an 8×128 pixel analog section and a 24×128 pixel digital section, the latter implementing a discriminator at the end of each column [20]. Right: beam-test results of the MIMOSA-8 digital section, showing the detection efficiency as a function of the discriminator S/N cut. The integration time was 50 μs [21].

Saclay and IPHC, Strasbourg, which was fabricated in the TSMC 0.25 μm process and featured an $\sim$8 μm thin epilayer and a 25 μm pixel pitch. The chip was divided into an analog and a digital section with a discriminator at the end of each column [20]. The chip showed a good noise performance ($\sim$15 electrons ENC) and a low pixel-to-pixel dispersion. Beam test of the digital part showed an efficiency of 99%, and a fake hit rate smaller than 10^{-3}/pixel/event even for a low S/N cut of the discriminator (Fig. 5) [21]. The architecture has been recently ported in the AMS 0.35 μm OPTO process [16].

If the pulse height information is preserved to perform charge center-of-gravity interpolation, analog-to-digital converters (ADC) have to be integrated at the end of the column on one side of the pixel active area. The ADC accuracy needs to be optimized taking into account the single point resolution but also the ADC size, which contributes an inactive area at the edge of the ladder and its power dissipation. The required 2-3 μm resolution can be obtained with a 20 μm pitch and 4-5 bits ADC accuracy, provided that the pixel pedestal and fixed base levels can be removed before digitization by applying CDS [22] [23].

In-pixel CDS has so far been implemented with two approaches. The MIMOSA-8 prototype, mentioned above, implemented a double sampling circuitry in each pixel, based on the so-called clamping capacitor, in which the reset and signal levels were stored at the end of each column [20]. A different approach uses in-pixel charge storage. This has been implemented in the MIMOSA-9 prototype [24], designed at IPHC and in the LDRD-2 chip, designed at LBNL in the AMS 0.35 μm OPTO process. The latter has the signal and reset levels consecutively stored on two polysilicon capacitors integrated in each pixel, and subsequently sent to the chip analog output for the subtraction to be performed online [25]. The chip has been successfully tested up to a pixel rate of 25 MHz with no significant loss in performance (see Fig. 6).
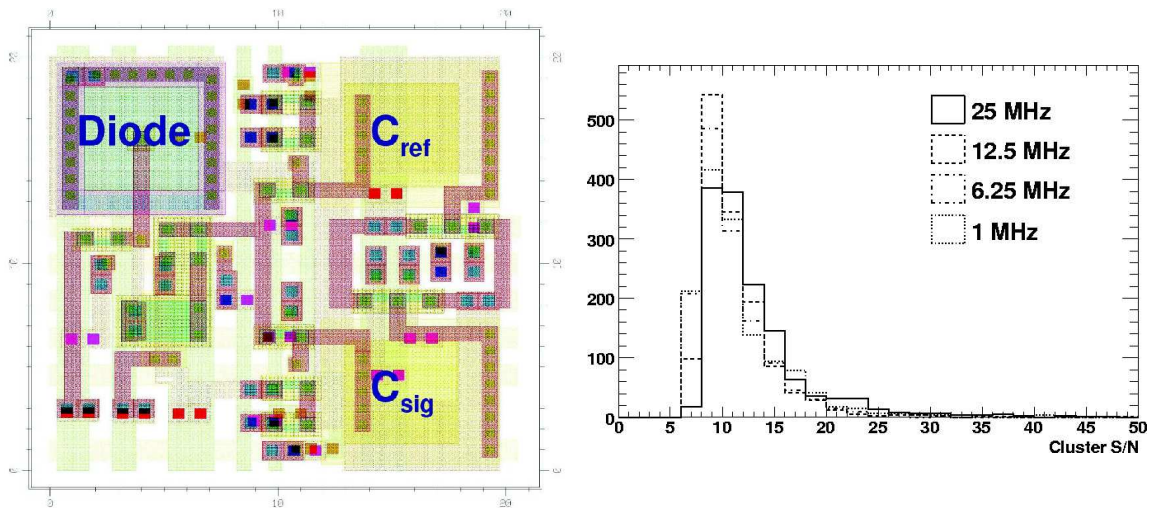

Figure 6: Left: pixel layout of the LDRD-2 chip from LBNL, Berkeley. The pixel pitch is 20×20 μm^2. The in-pixel CDS is performed by consecutively storing the pixel signal and (after a reset) base level on the C_{sig} and C_{ref} capacitors integrated in each pixel. Right: cluster S/N for 1.35 GeV e$^-$ from the LBNL Advanced Light Source (ALS) obtained with the LDRD-2 pixel chip for different readout frequencies. The integration time at 25 MHz is 184 μs (from [25]).
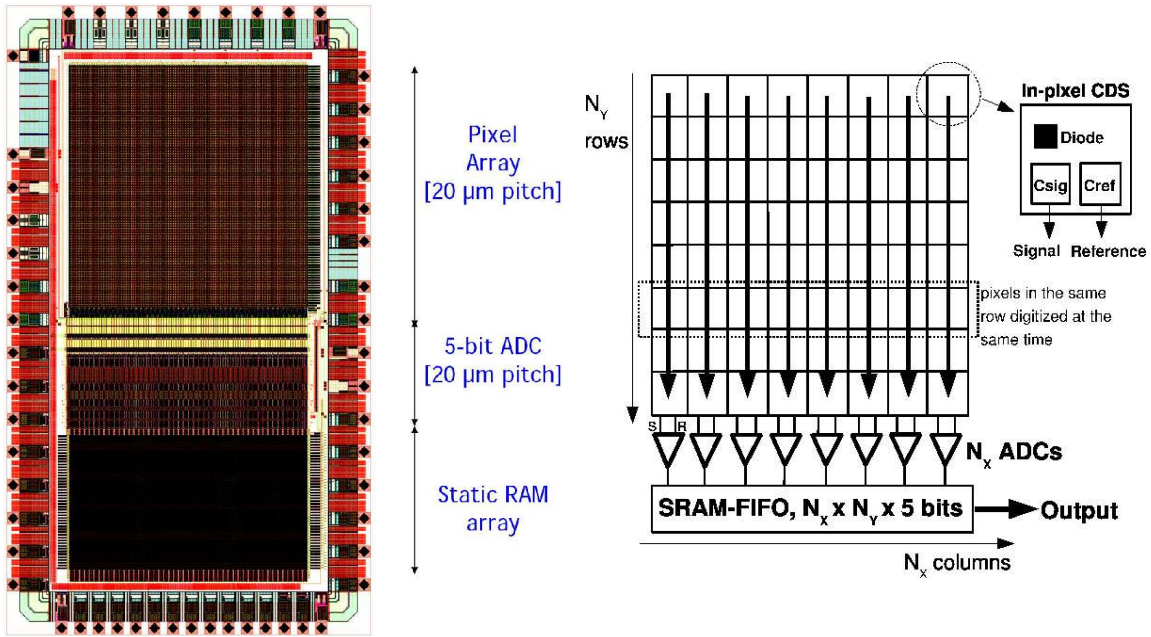
Figure 7: Layout (left) and schematic (right) of the LBNL LDRD-3 chip [27].

Several ADC architectures are being explored. The IN2P3-DAPNIA collaboration in France has designed flash, successive approximation, and Wilkinson ADCs. The characterization of test structures is under way, and the fabrication of a sensor prototype with integrated ADCs is foreseen in 2008 [26]. The LBNL group has designed and produced the LDRD-3 chip (Fig. 7), which features fast column-parallel readout with integrated ADCs at the end of each column, matching the pixel pitch of 20 μm. The 96×96 pixel chip has been fabricated in the AMS 0.35 μm OPTO process. Each pixel features the same in-pixel CDS architecture as the LDRD-2 chip, and a 5-bit successive approximation, fully-differential ADC at the end of each column, running at a clock frequency of 300 MHz. After digitisation, data is stored in a SRAM memory cell integrated in the chip [27]. The chip has been received in October 2007 and is currently being tested.

4. MAPS with local storage of charge signals

A different readout approach is sampling each pixel multiple times during the bunch train and storing the signals in local (in-pixel) memories, to be read out later during the 199 ms beam-off time between bunch trains (see Section 1). This scheme is in principle robust against EMI effects and allows for an easier handling of the large expected data flux. A multi-memory pixel architecture with delayed readout was first developed by the RAL group in the UK, in the so-called Flexible Active Pixel Sensors (FAPS) [28]. Signals from consecutive pixel readings are stored in capacitors integrated in each pixel, and read out at a later time. The same approach has been pursued by the IPHC group with the MIMOSA-12 prototype, which integrates four MOS capacitors of different values (50, 100 and 200 fF) in each pixel [13]. A similar approach is also adopted in the Continuous Acquisition Pixel (CAP) devices, developed for application at a high lumininosity *B* factory, and considered for application at the ILC [29]. Each CAP pixel includes a pipeline, 8-deep or 10-deep

in the CAP2 and CAP3 prototypes respectively, which can be used either for N independent samples of for $N/2$ CDS signal pairs, the difference being performed by the front-end readout electronics. This architecture makes it possible to decouple the frame sampling rate from the readout rate, so that the data transfer rate from the chip can be much reduced.

Such developments aim for a minimal size capacitor, so that many capacitors can be integrated in a small pixel pitch, providing satisfactory precision. Indeed, MOS capacitors are smaller but less precise, while polysilicon capacitors are more precise but larger. A trade-off between the pixel pitch and the number of capacitors implemented in each pixel is needed. Multi-memory devices appear most useful in the Vertex Tracker outer layers, where the number of channels is larger and the point resolution requirements more relaxed, allowing for a larger pixel pitch.

5. Binary architectures with time-stamping

The third architecture being considered adopts a binary readout with in-pixel time-stamping capabilities. Time information, precise enough to resolve few bunch crossings, if not single bunches, ensures a low enough occupancy without the need of fast readout or local charge storage. Implementing time stamping in CMOS pixels is a significant challenge. In standard MAPS one of the main obstacles is represented by the limitation to implanting only one type of transistor in the p-well (i.e. n-MOSFETs). A solution to this problem could be the use of triple-well processes, in which a deep n-well is used to shield the standard p-well; the p-well hosts n-MOS transistors like in standard MAPS, while the standard n-well may host p-MOS transistors, since the deep n-well is used to collect the charge generated in the epitaxial layer. The possibility for using the two types of transistors in each pixel allows the integration of advanced functionalities, at a price of possible charge collection inefficiencies due to the presence of the standard n-well. With respect to this, a deep p-well implant below the standard n-well would be beneficial in order to prevent parasitic charge collection, as proposed in [30]. A second challenge is to implement the needed circuitry in a pixel size of approximately $10 \times 10 \ \mu m^2$ to preserve the point resolution. The rapidly decreasing feature size of commercial CMOS processes offers a hope on the time scale of construction of a linear collider.

Experience with designing pixel sensors using a triple-well CMOS process has been gained by the SLIM collaboration of INFN groups in Italy, which has fabricated a series of prototype chips (named APSEL) that provide a proof of principle for the technology [31]. A new prototype has been recently submitted in the STM 0.13 μm triple well CMOS process, featuring in-pixel discriminators and a digital section with a 5-bit time stamp and data sparsification logic; the whole architecture results in 164 transistors integrated in a $25 \times 25 \ \mu m^2$ pixel. This technology might allow time-stamping during the ILC bunch train with subsequent inter-train readout, thus resulting in an architecture that is tailored to the ILC beam structure and is also EMI insensitive.

Single bunch crossing tagging for the ILC is the aim of the Chronopixel design, an effort carried out in the US by Yale U. and Oregon U. groups in collaboration with Sarnoff Corporation. A first prototype of the ambitious device has been designed and test structures in TSMC 0.18 μm process are expected to be delivered and evaluated in 2008 [32]. A bunch-by-bunch time tag is recorded for each pixel, the data is buffered during the $\sim$3000 bunches in a train and then read out in-between bunches. The high pixel complexity is demonstrated by the over 500 transistors
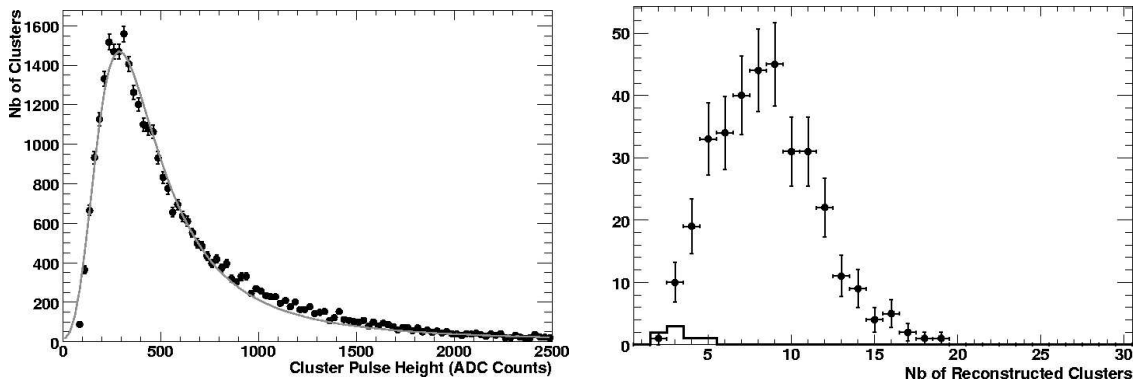
Figure 8: Test results of the LDRD-SOI chip with 1.35 GeV electrons at the LBNL ALS. Left: cluster pulse height distribution for 1.8 V analog pixels at a depletion voltage of 10 V. Right: hit multiplicity for digital pixels at a depletion voltage of 30 V (markers with error bars). The distribution of fake hits reconstructed in the absence of beam (continuous line) is also shown for comparison.

needed for the comparators and a 4-events deep memory with the bunch clock bus. In the currently available 0.18 μm process this is only feasible in a 50×50 μm^2 pixel, which is still far from the ILC resolution goals. A process with a feature size of 45 nm is necessary and the technology roadmap shows that this may be available by the time the ILC detectors will be built. A triple-well or quadruple-well technology is needed in order to increase the pixel sensitive area and collect enough charge. Moreover, depletion of the sensitive volume would be desirable in order to limit the charge spreading and thus keep the occupancy at manageable levels. All these issues and the characterisation of a 45 nm CMOS process for radiation detectors are part of the forthcoming R&D effort.

A novel concept binary readout is implemented in the latest prototype of the CAP sensor family developed by the Hawaii U. group [33]. The CAP4 chip features, besides an analog section, two binary sections with a comparator in each pixel. The digital bit corresponding to the hit pixel is continuously shifted to both the left and right adjacent pixels in a row; at the row outputs, the hit position and time are then reconstructed by an external pipeline from the timing of the left out and right out signals. In this approach, data are streamed continuously out of the sensor without trigger rate limitation, and the data flux is also significantly reduced from the intrinsic data sparsification.

6. MAPS in SOI technology

The Silicon-On-Insulator (SOI) technology has emerged in the past few years as a promising alternative in the fabrication of monolithic pixels. In this technology, the electronics layer can be isolated from a high-resistivity substrate by a buried oxide. The high-resistivity substrate can be contacted from the electronics layer by means of vias through the buried oxide, so that pixel implants can be created and, above all, the substrate can be depleted as in standard reversely-biased silicon detectors. Hence, the SOI technology potentially couples the advantages of a depleted substrate (presence of an electric field, fast charge collection) with a full CMOS process on the same sensor substrate.
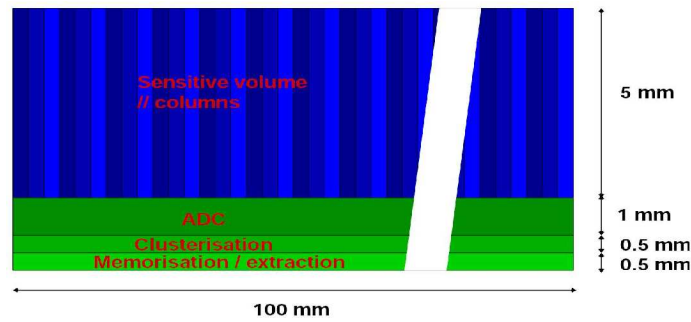
Figure 9: Concept for a Vertex Tracker Ladder based on CMOS sensors with column-parallel readout, integrated sparsification and digitization.

A first proof of principle of SOI technology adapted to particle detection applications was achieved by the SUCIMA collaboration. Their prototype chip was successfully tested with a ^{90}Sr source [34, 35], but it relied on an in-house process of 3 μm feature size, not compatible with a standard CMOS process. In 2005 OKI Inc., Japan, made a novel 0.15 μm fully-depleted SOI process available. Through R&D with KEK it has been possible to combine a high-resistivity substrate with full CMOS circuitry on the top layer. High speed, low power dissipation designs are thus possible, with improved latch-up immunity. A pioneering work by KEK led to the fabrication of prototype pixel chips with a 350 μm substrate, a 200 nm thin buried oxide and a 40 nm thin CMOS layer, which is fully depleted at operational voltages [36, 37]. The functionality of the first prototype has been demonstrated in 2006, and has led to a second run where several institutions in Asia and in the US submitted their designs. One of these is the LDRD-SOI chip designed at LBNL which features 10×10 μm^2 pixels arrayed in two analog sections (with 1.0 V and 1.8 V operating voltages) and a digital section with a comparator and a latch integrated in each pixel [38]. The LDRD-SOI chip is the first chip built in SOI technology to be successfully tested on a high-momentum particle beam, the 1.35 GeV electron beamline at the LBNL Advanced Light Source (ALS) facility. Despite a significant back-gating effect, which limited the maximum depletion voltage to $\simeq$15 V in the analog section, a S/N of 15 has been obtained. Figure 8(left) shows the observed cluster pulse height for analog pixels with 1.8 V operating voltage. The digital section of the chip proved also to be functional and higher substrate biases, up to 30-35 V, could be used. Figure 8(right) shows the hit multiplicity observed with and without the beam where a clear excess of hits can be seen in the presence of the beam.

A run in the OKI 0.20 μm FD-SOI process, optimized for low leakage current, is foreseen at the beginning of 2008. Despite being in its early stage of R&D, this technology is of great interest for its potential to implement complex architectures, such as digital pixels with in-pixel time-stamping, combined with a high-resistivity, depleted substrate ensuring faster charge collection, smaller cluster size and larger signals.

7. Vertex Tracker system integration issues

In parallel with the development of the sensor technology and readout architecture, R&D efforts on mechanical design and system integration have started in recent years. Different geometries
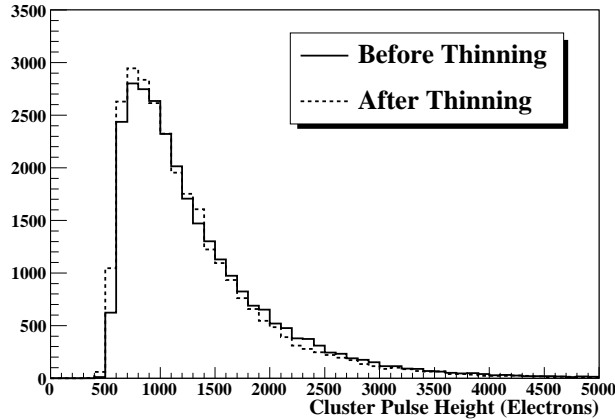
Figure 10: Characterisation of one MIMOSA-5 sensor before and after back-thinning to 50 μm: 1.5 GeV e$^-$ cluster pulse height, before (solid line) and after (dotted line) back-thinning, from [40].

are being considered for the vertex detector geometry, such as the option of having a barrel-only detector versus a short barrel plus forward disks. A detailed, realistic geometry for the first option has been proposed, based on CMOS monolithic pixels [13]. This features five cylindrical layers located at radii from 15 mm to 60 mm, with different pixel pitches in the various layers, amounting to a total of ~300 million pixels. This design has been implemented in the simulation framework of the LDC detector concept [39]. The integration of such a detector sets different requirements on the sensor architecture for the different layers. The inner vertex layers need sensors with a fast column-parallel readout and integrated signal processing. Figure 9 shows a sketch of the proposed layout: most of the ladder area is pixellated, with the pixel readout circuitry aranged along the short edge of the ladder. ADCs or discriminators, depending on the choice of analog or binary readout, are integrated at the end of each column and followed by circuitry for data sparsification and memory for data buffering. In the outer layers the constraints from the pair background are much less stringent, due to the solenoidal field, and a lower readout rate can be adopted for the larger data flux. On these layers, it may be advantageous to adopt larger pixels with local charge storage, read out during the time elapsing between bunch trains. This approach reduces the data flux and the power dissipation, as mentioned in Section 4.

Achieving the target ladder thickness while ensuring a mechanical stability to a few microns poses significant challenges. The starting point is the assessment of sensor back-thinning to ≤ 50 μm.

Significant experience on sensor back-thinning has been gained in recent years. Different post-processing techniques have been tested with industrial partners both in the US and in Europe. In particular, a systematic study including yields and MAPS response before and after processing has been performed by LBNL on diced chips using a proprietary grinding process developed by Aptek Industries (San Jose, CA). More than 25 MIMOSA-5 chips (see Section 2) were thinned down to a minimum thickness of 40 μm. The yield for chips after the grinding process was 90%. An extensive characterization with lasers of different wavelengths, radioactive sources and a high-momentum

12

Component	% radiation length
MIMOSA-5 sensor	0.0534
Film adhesive	0.0143
Cable assembly	0.090
Film adhesive	0.0143
CF/RVC carrier	0.11
Total	**0.282**

Figure 11: View of the STAR HFT ladder prototype (left) and associated material budget (right) [41]. The ladder prototype is 20 cm long and 2 cm wide, and is supported only at one end, consistently with the side-mount foreseen in the STAR HFT upgrade.

electron beam has been performed before and after back-thinning, showing that the thinning process does not significantly affect the charge collection and signal-to-noise performances [40]. Figure 10 shows the measured cluster pulse height for 1.5 GeV electrons before and after the grinding process, demonstrating that no significant effects on the charge collected are observed.

These, and other similar results, have promoted efforts in the design of thin detector ladders based on 50 μm thin sensors mounted on a carbon composite support to achieve the target material budget of $\simeq 0.1$ % X_0. An interesting precursor of this concept is the Heavy Flavor Tracker (HFT) currently under construction for the STAR detector at RHIC, Brookhaven. The HFT is based on thin MAPS, designed by the IPHC group, and aims at a minimal material budget motivated by the small transverse momentum of charm mesons produced in heavy ion collisions. The required layer thickness for the HFT is $\leq 0.3\%$ X_0. A low-mass ladder prototype using carbon composite materials and 50 μm thin MIMOSA-5 pixel sensors has been designed, built and characterised at LBNL. The material budget achieved by the prototype is 0.28% X_0, which is dominated by the contribution of the carbon composite carrier and the interconnections (see Fig. 11). The prototype carrier consists of a sandwich of 3.2 mm thick RVC foam in between two 50 μm thin layers of CFC. A cable assembly, made of four layers of 25 μm thin kapton and 20 μm thin Al conductor, is glued on top of the carrier via film adhesive and is used to drive the sensor power lines and analog outputs, allowing on-ladder functionality tests. Several (up to 8) 50 μm thin MIMOSA-5 chips have been glued via film adhesive on top of the cable assembly. The STAR ladder prototype has been used for various studies of accuracy of chip mechanical positioning and surface flatness, and also studies of heat removal using low speed air flow. It has been shown that an airflow of 2 m/s can effectively remove $\simeq 80$ mW/cm^2, inducing an r.m.s. displacement at the unsupported end of the ladder of 4.3 μm [41].

Two efforts on the engineered design and prototyping of low mass ladders are under way. The first is carried out as a collaboration by Washington U. and Fermilab. The second is developed at LBNL and is based on the experience with thin sensors and synergies with the STAR HFT experience. An interesting concept, which has emerged as a leading candidate for prototyping, is the so-called cool core ladder [42], in which a carbon foam layer with pixel chips mounted at both sides is a sandwich structure that acts both as mechanical support and as a guide for the airflow cooling, which is delivered through a longitudinal channel cut through the middle of the foam core. The RVC foam thus acts as a network of fins, substantially improving the effective heat transfer coefficient. Graphitic carbon foams have recently been obtained which offer low densities (0.2-0.6

g/cc) and high thermal conductivity (40-180 W/mK), and may be more effective than RVC for thermal management [43].

In parallel with the sensor R&D and the ladder mechanical design, significant experience is being gained on tracking and vertexing with CMOS pixel sensors in beam tests. The Hawaii U. group tested the first beam telescope made of CMOS pixel sensors, an array of four CAP1 chips on the 4 GeV/c pion beamline at KEK [44]. Subsequently, LBNL built the first pixel telescope based on thin CMOS pixel chips, the Thin Pixel Pilot Telescope (TPPT) [40]. The TPPT features four layers of 50 μm thin MIMOSA-5 chips, precisely spaced by 1.5 cm in an ILC-like geometry. The TPPT provides a good extrapolation resolution in a low momentum environment, and has been extensively tested both with 1.5 GeV electrons and with 120 GeV protons, at the LBNL ALS and the FNAL MTBF facilities respectively. The aim of the TPPT is the study of tracking and vertexing capabilities of a CMOS pixel tracker in a layout closely resembling the proposed ILC vertex tracker in a realistic environment with track multiplicities similar to those expected in the core of hadronic jets produced in e^+e^- collisions at 0.35-1 TeV. These data will also be important for validating the simulation and reconstruction software used for ILC physics studies. A collaborative effort of European institutions in the framework of the European Union funded EUDET project has been designing and deploying a CMOS pixel telescope based on MIMOSA chips [45] to be used for beam tests of new detector devices. A first 5-plane demonstrator has been commissioned on the DESY 6 GeV electron beam and on the CERN 120 GeV/c pion beam; the final telescope is expected to consist of 6 planes based on reticle-size chips with binary pixels. A 1 μm extrapolation resolution at the position of the device under test (DUT) should be achievable on the DESY electron beam with the aid of a high-resolution plane placed close to DUT at the center of the telescope. The telescope will be installed at the DESY and CERN beam-test facilities, and made available to a broad community. Finally, the IPHC, Strasbourg group also presented a pixel telescope based on thin, 10 μm pitch MIMOSA sensors which should provide sub-micron extrapolation accuracy at the DUT position [46].

8. Conclusions & Outlook

Monolithic Active Pixel Sensors is a leading candidate technology for a vertex detector at an e^+e^- linear collider. Test devices have shown excellent detection performances through several prototypes exploring different technologies and architectures. The fast readout needed to cope with the high background expected in the innermost layers may be achieved with a column-parallel architecture and the implementation of on-chip data reduction; the radiation hardness so far demonstrated is satisfactory with respect to the ILC requirements; thinning to 50 μm and below has been established, and the implementation of integrated ADCs and data sparsification capabilities is under way in forthcoming prototypes. The technology has shown significant progress over the past years and has achieved an important level of maturity; the next steps of the R&D efforts should address the optimization of the sensor architecture, bearing in mind the issues relevant to the integration of sensors on a realistic, low-mass ladder. With respect to this, the application in various pixel telescopes and in the STAR vertex detector upgrade are and will be important test benches.

Concerning the fabrication technology, it is apparent that bulk CMOS processes optimized for imaging applications are suitable for analog architectures with integrated functionalities like in-

pixel CDS and on-chip digitization. On the other hand, emerging technologies such as triple-well CMOS and SOI might be the optimal choice for digital architectures, possibly with in-pixel time stamping. The availability of a suitable fabrication process which provides both a small feature size to allow the integration of complex functionalities and an epilayer thick enough to yield reasonable charge signals, is an important issue, which so far has been favored by the availability of similar processes from the digital imaging market.

Acknowledgements

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