

Vertex Detector for the SuperB Factory

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A new concept for a high-luminosity B-Factory (SuperB) has been recently proposed to deliver a luminosity greater than $10^{36}\text{cm}^{-2}\text{s}^{-1}$ with moderate beam currents. Comparing to current B-Factories, the reduced center of mass boost of the SuperB machine requires improved vertex resolution for optimal time dependent measurements, which form the basis of the SuperB scientific program. Design studies indicate that such improved resolution is achievable with a vertex detector based on the BABAR silicon vertex tracker layout with the addition of an innermost Layer 0 at radius of about 1.5 cm, with a material budget of about 0.5% X_0 and capable to sustain a background rate of about 5 MHz/cm².

Several options for the Layer 0 design are reviewed in this paper. CMOS Monolithic Active Pixels (MAPS) is the most promising technology but extensive R&D is needed to meet all the requirements. The most recent developments on a new CMOS MAPS sensor, based on Deep NWell (DNW), are discussed. The design of DNW CMOS MAPS has been recently proposed by the SLIM5 Collaboration to develop a thin pixel system with sparsified readout suitable for application in the SuperB Layer 0. Several prototype chips, realized with the STMicroelectronics 130 nm triple well process, have demonstrated that the design is viable with good sensitivity to electrons from ⁹⁰Sr. Based on the new DNW MAPS design, a dedicated fast readout architecture to perform on-chip data sparsification is currently under development.

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1. Introduction

One of the main focuses of the elementary particle physics community in the next decade will be on the search for evidence of New Physics (NP) beyond the Standard Model. The detailed study of heavy quark and lepton decays (flavour physics) will play a crucial role in the understanding of the flavour sector of New Physics phenomena, being complementary with the LHC and LHCb programs. In fact the production and observation of new particles is not the only way to look for New Physics. The presence of new heavy particles, which can participate in higher order diagrams, can alter SM predictions of B, D and τ decays. In some cases [1] high precision measurements of heavy flavour decays could allow to probe NP even beyond the scale accessible at LHC.

The existing asymmetric B-Factories, PEP-II and KEKB with their detectors *BABAR* and *Belle*, have produced over the last eight years an extremely rich physics program. Thanks to the high statistics accumulated, with peak luminosity above $10^{34}\text{cm}^{-2}\text{s}^{-1}$, present measurements of the angles and the sides of the unitarity triangle represent a stringent test of the Standard Model and indicate the Cabibbo-Kobayashi-Maskawa mechanism is the dominant source of the observed CP violation in the K and B systems. Deviations from the SM expectations, due to NP effects, are likely to be very small but could be made accessible at the B-Factories if a larger data sample could be produced together with clean predictions from theory.

With a high-luminosity B-Factory (SuperB Factory) flavour physics will continue to play a crucial role in the next decade: the definitive test of the consistency of the CKM mechanism will be possible and the search of New Physics will be exploited in several B, D and τ decays that are experimentally accessible only in the clean e^+e^- environment. In many channels the required sensitivity can only be achieved with a data sample of about 50ab^{-1} , requiring a machine peak luminosity of about $10^{36}\text{cm}^{-2}\text{s}^{-1}$ [1].

Although the physics case for a high-luminosity B-Factory has been clearly established a few years ago [2], until recently building such a high-luminosity machine was considered extremely difficult and very expensive. Attempts to design a high-luminosity B-Factory date to 2001. These projects essentially proposed to improve the machine luminosity increasing substantially the beam currents. This has several drawbacks, including the high machine backgrounds and high wall plug power necessary to run the machine. Furthermore, this approach has an effective limitation in the maximum luminosity achievable at around $5 \times 10^{35}\text{cm}^{-2}\text{s}^{-1}$ [1].

In 2005 a new concept for a high luminosity e^+e^- collider at the $\Upsilon(4S)$ has been proposed to deliver luminosity greater than $10^{36}\text{cm}^{-2}\text{s}^{-1}$ with beam currents even below those of the present B-Factories ($2.3\text{A} \times 1.3\text{A}$) and an estimated total power consumption of only about 35 MW. This SuperB Factory would use a new combination of linear collider and storage ring techniques. In this scheme beams will be stored in low-emittance damping rings similar to those designed for the International Linear Collider (ILC). An ILC style interaction region will be included in the ring to produce a sub-millimeter vertical beta function at the collision point. The resulting very small vertical beam size at the IP ($0.035\mu\text{m}$), about a factor hundred smaller than in present B-Factories, will account for most of the large increase in the achievable luminosity. Furthermore a large crossing angle ($\pm 17\text{mrad}$), a large Piwinski angle and the so called Crab Waist scheme [1] are used at the collision point to allow beam separation, reduce beam-beam effects and instabilities, and further improve the luminosity. The new accelerator design requires a reduced beam energy

asymmetry ($4\text{GeV} \times 7\text{GeV}$) with respect to the present B-Factories. The resulting reduced average B vertex separation in SuperB will impose more stringent requirements on vertex resolution, crucial for all time-dependent measurements. Detailed parameters of the machine design can be found in the SuperB Conceptual Design Report [1].

Since the new machine concept was proposed, the interest of the HEP Community for the SuperB Project has grown rapidly. After a series of five Workshops, held between 2005 and 2007, a SuperB Conceptual Design Report (CDR) has been written and it is currently under review by an International Review Committee appointed by the INFN. The final report of the Committee will be available in Spring 2008.

In this paper the main issues for the design of a vertex detector for the SuperB Factory are reviewed (Sec.2-4). Recent developments on CMOS Monolithic Active Pixel Sensors (MAPS) are also reported (Sec.5). This new technology is in fact very promising for the design of the innermost layer of the silicon vertex tracker.

2. Vertex Detector Design Concept

The SuperB vertex detector concept, is based on the current *BABAR* Silicon Vertex Tracker (SVT [3]), with modifications required to operate at a luminosity of $10^{36}\text{cm}^{-2}\text{s}^{-1}$ and with a reduced center of mass boost. The main goal of the SVT is to allow a precise measurement of the vertex separation fundamental to all time dependent analyses, which form the basis of the SuperB scientific program, as it does for the existing asymmetric B-Factories.

Time-dependent analysis performed at the asymmetric B-Factories are based on precise measurement of Δt , the proper time difference between the two B mesons. This variable can be evaluated from Δz , the B vertex separation along the beam axis z , measured in the laboratory frame: $\Delta z \simeq \beta\gamma c\Delta t$, where $\beta\gamma$ is the $\Upsilon(4S)$ center of mass boost. This approximation still holds for the SuperB boost ($\beta\gamma \simeq 0.28$), which is almost a factor of two smaller than the boost of present B-Factories. Finite vertex resolution will cause an increase in the uncertainty of measured CP asymmetries. However, analytical calculations and Monte Carlo simulations have shown that this increase is less than 10% as long as the resolution on Δz is less than half of the average separation between B decays [4]. In SuperB the average B vertex separation in the z direction will be about $125\mu\text{m}$ ($\langle \Delta z \rangle \simeq \beta\gamma c\tau_B$), and the resolution on the z vertex separation should be $\sigma_{\Delta z} \simeq \langle \Delta z \rangle / 2 \simeq 60\mu\text{m}$, to perform precise CP time-dependent measurements.

Achieving this vertex resolution requires measuring the first hit on track as close as possible to the production vertex. The conceptual design of a SuperB vertex detector is therefore based on the *BABAR* SVT layout, with an additional innermost Layer 0 at very small radius to achieve the improved vertex resolution. A longitudinal section of the *BABAR* SVT detector, with a Layer 0 added is shown in Fig.1. The total material of the beam pipe and Layer 0 should be kept to a minimum, since the multiple scattering contribution dominates the track parameter resolution for the low momentum particles typical of B decays at the B-Factories. Furthermore the Layer 0 should be highly segmented to ensure a good intrinsic resolution, important for higher momentum particles. Impact of machine related background should also be taken into account in the design of Layer 0.

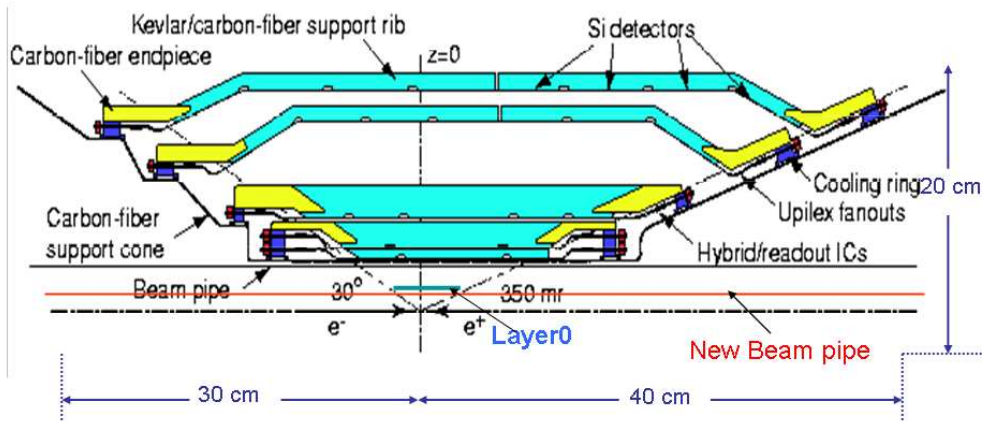


Figure 1: Longitudinal section of the *BABAR* SVT with the addition of an innermost Layer 0. The line just below the Layer 0 indicates the location of the new SuperB beam pipe.

3. Layer 0 design requirements

In order to optimize the design of the Layer 0, in terms of radial position, total material and intrinsic resolution, a fast simulation program (TRACKERR [5]) has been used, which employs analytical parametrizations to simulate the detector response. The resolution on the B decay vertices and on their proper time difference Δt has been simulated for several analyses that require time dependent measurements, using the present *BABAR* detector with an additional Layer 0 with different configurations. The benchmark was to reach a resolution on the proper time difference $\sigma_{\Delta t} \simeq 0.6\text{ps}$, equivalent to the *BABAR* resolution, according to the same fast simulation response.

In the SuperB interaction region, with extremely small beam dimensions in the transverse plane, the beam pipe radius could be reduced down to about 1 cm, and this would allow to have a Layer 0 at a radius as small as 1.2 cm. Preliminary studies on the beam pipe design indicate it can be realized with a total material budget of $0.42\% X_0$ that accounts for the beryllium pipe, a few microns of gold foil, and a water cooling channel needed to evacuate a beam related power load of about 1 MW.

As an example of the studies performed, Fig. 2 shows the resolution on the proper time difference, obtained for the nominal SuperB boost of 0.28, for different Layer 0 radii and as a function of the total material of the Layer 0. The intrinsic hit resolution was set to $10\mu\text{m}$. In the studies shown the decay mode, $B \rightarrow \pi^+\pi^-$ or $B \rightarrow D^{*-}\pi^+$, was exclusively reconstructed and the other B decay vertex was reconstructed using the charged tracks of the rest of the event, after rejecting long-lived particle decays and tracks not compatible with the candidate vertex.

According to the optimization studies [6], for the proposed SuperB boost of 0.28, the benchmark resolution is achievable with a Layer 0 radius of 1.2-1.5 cm and a Layer 0 thickness of about 0.5-0.8% X_0 , assuming a hit resolution of $10\mu\text{m}$.

Other requirements on the SVT and especially on the Layer 0 design are imposed by the machine related backgrounds. The Layer 0 will need to have high readout segmentation, to maintain

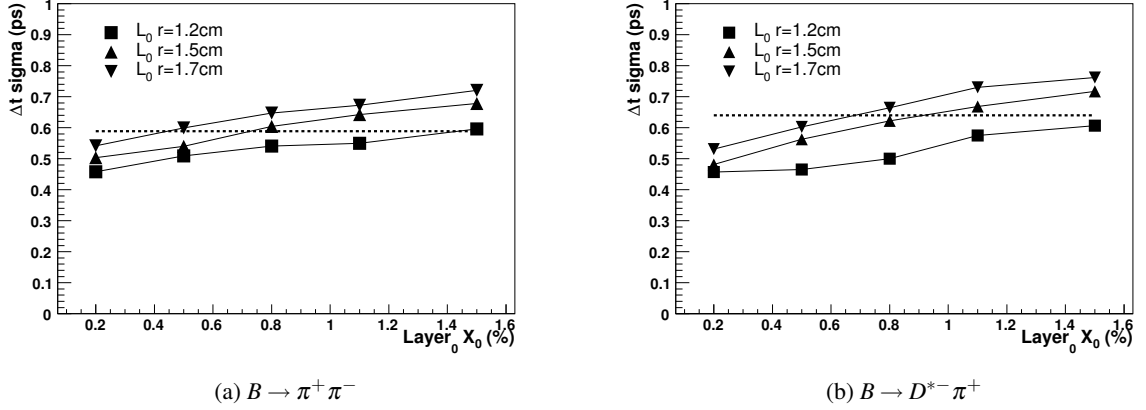


Figure 2: Resolution on proper time difference $\sigma_{\Delta t}$, for the nominal SuperB boost ($\beta\gamma = 0.28$), for different Layer 0 radii, as a function of Layer 0 thickness (in X_0 %). Results for the $B \rightarrow \pi^+ \pi^-$ channel are shown in picture (a), while the $B \rightarrow D^{*-} \pi^+$ channel is shown in picture (b). The dashed line represents the BABAR reference value for the corresponding channel according to fast simulation. In this study the beam pipe was set at $r=1$ cm with a total material of 0.42% X_0 . The resolution on the single hit (z and ϕ) was set to $10\mu\text{m}$.

the occupancy under a few percent for optimal tracking performance, fast readout electronics, to cope with the high background data rate expected, and adequate radiation hardness.

With the proposed collider design the primary sources of background are due to luminosity terms, like coherent $e^+ e^-$ pair production and radiative Bhabha production, and Touschek scattering. Terms that scales with beam currents, photons from synchrotron radiation and lost beam particles, give smaller contributions. These sources give rise to primary particles that can either hit the detector directly, or generate secondary debris that enters the apparatus. The different sources of background have been simulated and modeled with a detailed Geant4 detector and beamline description to estimate their impact on the experiment [1]. From these studies the background expected in the external layers of the SVT ($R > 3$ cm) is dominated by terms that scale with beam currents and will be similar or even smaller then the one seen in the present BABAR SVT. The technology of the BABAR SVT is therefore adequate to design the external layers of the SuperB SVT.

The main background at Layer 0 location is dominated by $e^+ e^-$ pair production. Despite the huge cross section of this process the rate of tracks hitting Layer 0 is strongly suppressed by the effect of the 1.5 Tesla magnetic field inside the detector. Particles produced, with low transverse momentum, loop in the detector magnetic field and only a small fraction reaches the SVT layers, with a strong radial dependence. A typical hit rate of 5 MHz/cm^2 is expected at a radius of 1.5 cm, corresponding to a dose of about 1 Mrad/yr. The rate goes up to about 15 MHz/cm^2 at a radius of 1.2 cm.

4. Layer 0 design options: striplets, hybrid pixels, CMOS MAPS

Taking into account the different requirements imposed by the vertex resolution and the ma-

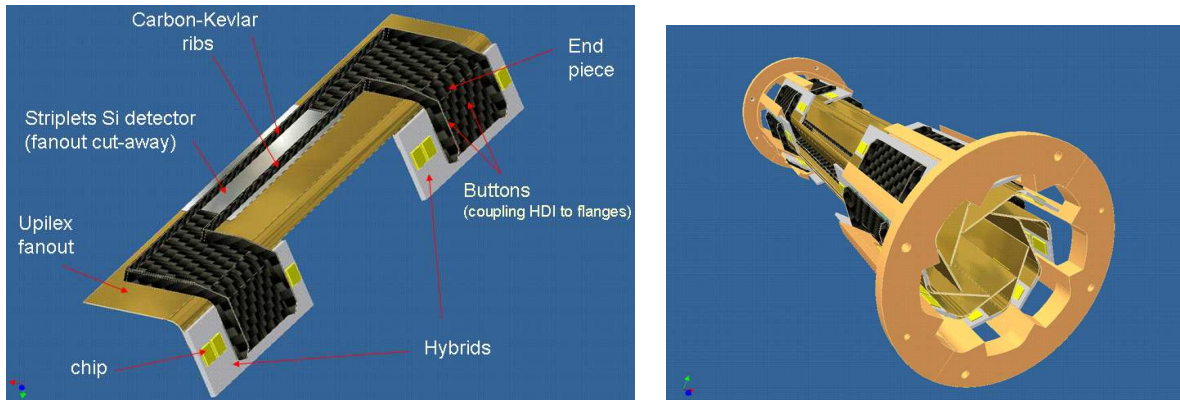


Figure 3: Right: 3D Drawing of a Layer 0 striplets module. Left: 3D view of the complete Layer 0 flange with the eight striplets modules.

chine related background, various options are under consideration for Layer 0 technology: standard high resistivity silicon detectors with short strips (striplets option), hybrid pixel detectors and CMOS Monolithic Active Pixel Sensors (MAPS options).

A baseline Layer 0 design based on striplets is described in detail in the CDR. The mechanical aspects of the design based on striplets have been worked out in some detail from module assembly up to the final mounting on the cooling flanges of the beam pipe. CAD drawings of a striplets module and the complete Layer 0 are shown in Fig. 3. Although the proposed design meets all the requirements and this technology is well established, it offers a modest safety margin with background rates higher than 5 MHz/cm^2 .

Hybrid pixel detectors, such as the ones realized for the LHC experiments, are on the contrary very robust against background occupancy but they have a larger amount of material due to the overlap of the sensor and the readout chip in the active area. As an example the total radial material for the ALICE hybrid pixel modules is about $1\% X_0$. This solution is viable although not optimal since it is slightly marginal in term of material budget.

CMOS MAPS technology is potentially very thin since the sensor and the readout electronics are integrated in the same substrate. This pixel option will be the optimal choice for Layer 0 if a chip design with the same advantage of thin CMOS sensor and a fast sparsified readout could be realized. A Layer 0 design based on CMOS MAPS modules has been proposed in the CDR. Each module will be composed of several MAPS chips glued onto a support structure that integrates a water-filled microchannel for cooling. The total material budget for the proposed Layer 0 MAPS design would be about $0.5\% X_0$, including 2 MAPS layers ($50 \mu\text{m}$ each), the support structure made of AlN ($680 \mu\text{m}$ thick, incorporating the water microchannel), and a multilayer thin bus hosting power, command and data lines.

With the Deep NWell (DNW) design proposed recently by the SLIM5 Collaboration [12], CMOS MAPS technology becomes very promising for the SuperB application but extensive R&D is needed to meet all the requirements. Key aspects to be addressed are: readout speed, pixel cell optimization in terms of S/N and power consumption, radiation tolerance and development of a thin mechanical support and cooling structure. Recent developments on DNW MAPS design and

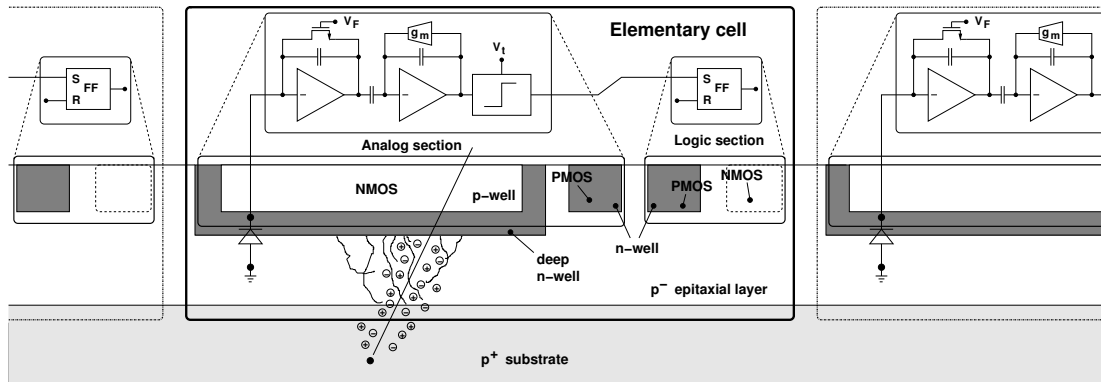


Figure 4: Cross section of the triple well active pixel sensor with in-pixel signal processing.

on the fast readout implementation are reported in section 5.

5. R&D on CMOS MAPS design

CMOS Monolithic Active Pixel Sensors (MAPS) are a promising candidate for thin tracking applications [7]: they incorporate on the same substrate the readout electronics and a very thin sensor, with the possibility to reduce the detector thickness down to $50\mu\text{m}$. The MAPS device uses an n-well/p-epitaxial diode to collect, through thermal diffusion, the charge generated by the impinging particle in the thin epitaxial layer underneath the readout electronics. In this technology the signal collected is only few hundreds of electrons, for typical p-epitaxial thickness of about $10\mu\text{m}$.

CMOS MAPS prototypes have been developed by several groups over the last few years [8, 9, 10, 11]. These designs follow the very simple readout scheme already adopted for imaging applications, based on the use of only three transistors on the pixel cell (3T), with a sequential readout. In this baseline MAPS the n-well collecting electrode should be as small as possible (typically only a few microns squared), since charge to voltage conversion is performed using the sensor capacitance. The use of PMOS in additional n-well regions inside the pixel cell, needed to develop a more complex in-pixel signal processing, is forbidden with this design approach. These “competitive” n-wells could in fact subtract charge from the main collecting n-well electrode causing an efficiency loss. Although these prototypes have shown excellent tracking performance, their readout speed, limited by the sequential processing, is one of their major limitations for the SuperB application.

A different approach to the design of CMOS MAPS has recently been proposed by the SLIM5 Collaboration [12] to improve the readout speed potential of these devices and at the same time to increase the sensitive element area. By exploiting the triple well option of CMOS commercial processes, a full signal processing chain has been implemented at the pixel level (charge pre-amplifier, shaper, discriminator and a latch), building a monolithic pixel with a readout scheme easily compatible with data sparsification.

The concept of the new design is illustrated in Fig. 4: the deep n-well (DNW) of the triple well process is used as a charge collecting electrode and also contains part of the front-end stage.

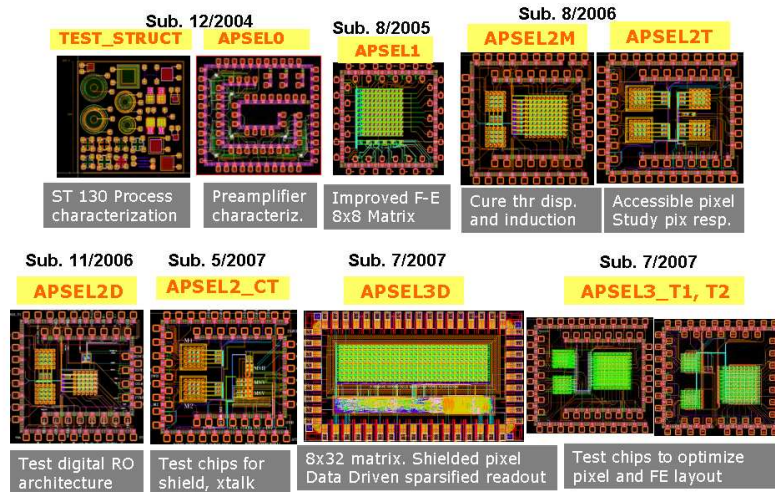


Figure 5: Submitted DNW MAPS chips with 130 nm STMicroelectronics triple well technology.

This is physically overlapped with the area of the sensitive element, allowing a more complex in-pixel readout electronics. Furthermore, since the voltage gain is now determined by the feedback capacitance of the charge preamplifier, the size of the collecting electrode can be increased to some extent, taking into accounts noise constraints. In the present prototypes the collecting electrode is about $900 \mu\text{m}^2$ in a pixel cell with a $50 \mu\text{m}$ pitch. Thus it is possible to include in the pixel cell some small competitive n-well regions, crucial to develop the logic for the sparsified readout, while keeping the fill factor of the sensor at the level of 90%.

The APSEL chips

Several DNW sensor prototypes, the APSEL chips shown in Fig. 5, have been realized with the STMicroelectronics, 130 nm, triple well technology, fabricated through CMP [13] multiproject wafers. The first prototypes proved the new design proposed for DNW MAPS is viable with good sensitivity to photons from ^{55}Fe and electrons from ^{90}Sr [14] [15].

The second generation of DNW MAPS prototypes (APSEL2 chips) implement a partial re-design of the analog circuit, realized to reduce significantly the threshold dispersion without increasing the noise figure.

Characterization of the APSEL2 chips

The detailed response of the APSEL2 sensor to charged particles has been measured on a 3×3 matrix with full analog output, using electrons from a ^{90}Sr source. The signal of the 3×3 cluster, surrounding the central pixel matrix, is shown in Fig. 6. The most probable value of the Landau distribution, used to fit the data, corresponds to a signal of 700 e- collected for a MIP crossing the sensor. The average pixel equivalent noise charge measured is about 50 e- ENC, resulting in a Signal-to-Noise ratio for MIPs of about 14.

Further cluster multiplicity analysis indicates that charge sharing among pixels is limited, with an average cluster size of only 2 pixels, for typical cuts on the seed and the adjacent pixels respectively of 5 and 3 times their noise.

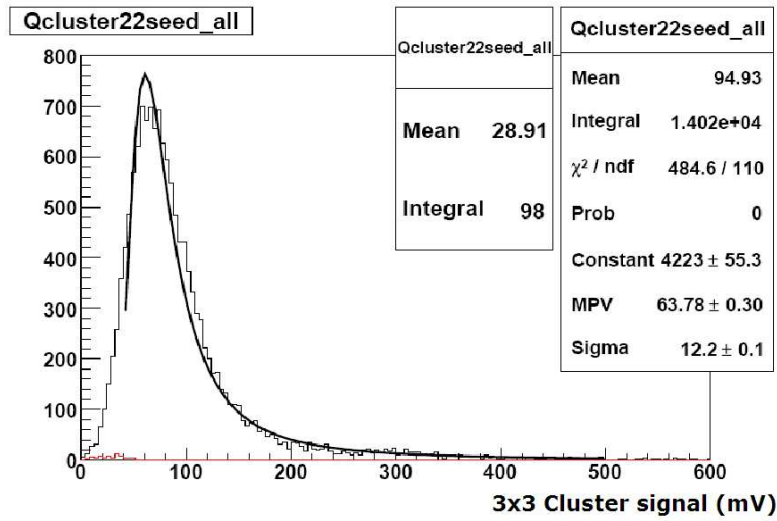


Figure 6: Cluster signal for electrons from a beta ^{90}Sr source. Landau most probable value corresponds to 700 e- (pixel gain calibration = 570 mV/fC)

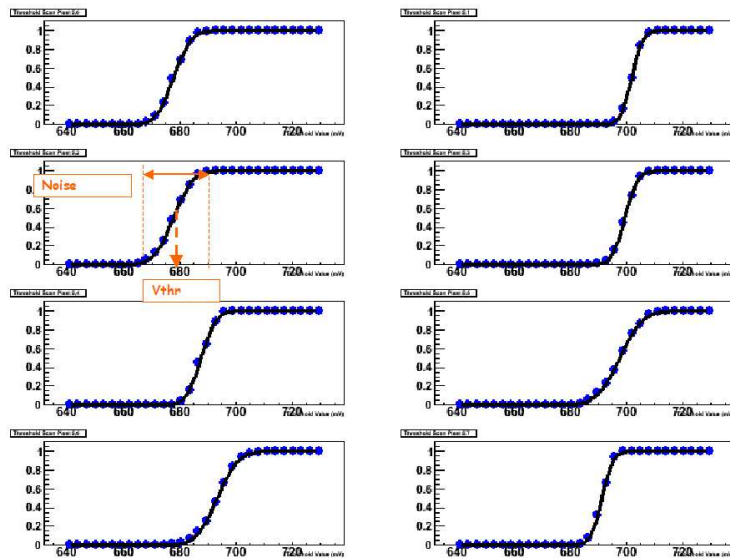


Figure 7: Hit rate as a function of the discriminator threshold for a matrix row.

On an 8x8 matrix with digital output the pixel ENC and the threshold are evaluated measuring the hit rate as a function of the discriminator threshold, as shown in Fig. 7. With a fit to the turn-on curve (using a modified erf function) we have measured a pixel ENC = 50 e-, with about 15% dispersion, and a threshold dispersion of about 100 e- (300 e- reported in a previous version of the matrix).

Improvements for the APSEL3 chips

A third generation of DNW MAPS (APSEL3 chips) has been submitted in July 2007. Tests for the characterization of the new prototype chips have just started.

In the new design a substantial redesign of the front-end and the sensor has been carried out to improve the S/N ratio and to reduce the power consumption with respect to the APSEL2 version. In the APSEL3 pixel the total sensor capacitance has been reduced significantly: the new collecting electrode is a combination of a deep n-well region and a standard n-well area (with smaller specific capacitance). This reduction of the total capacitance, from 500 fF to 300 fF, achieves a better balance between noise and power consumption: the power dissipation has been lowered by a factor two (down to 30 $\mu\text{W}/\text{ch}$) reducing also the pixel noise equivalent charge by 20%-40%. Post-layout simulation results indicate a pixel ENC of 41 e⁻ and 31 e⁻ for the two different versions of the front-end implemented in the APSEL3 chips.

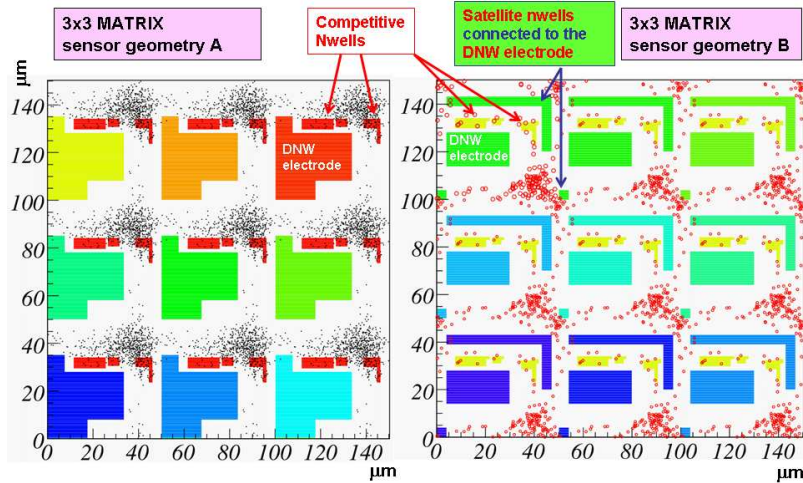


Figure 8: Schematic drawing of the two 3x3 matrix implemented in the APSEL3 chips with different sensor geometry: pixel geometry A (left), pixel geometry B (right). Dots indicate the inefficient regions located with the fast simulation: impact points of simulated MIPs crossing the matrix but not detected (collected signal below threshold).

We have developed a fast device simulation (taking into account the ionization process and charge diffusion) to optimize the sensor geometry for improved signal collection efficiency. The simulation has been tuned with the response of the APSEL2 pixel to electrons from the ^{90}Sr source: the fast simulation agrees to within 20% with the cluster signal collected from the real pixel matrix. The simulation is used to locate the low efficiency regions inside the pixel cell; efficiency is then improved by adding additional n-well electrodes connected to the main collecting electrode in these areas. Two different shapes of the sensor have been implemented in the APSEL3 chips as shown schematically in Fig. 8: the sensor named A (Fig. 8-left) has a single central collecting electrode, while in sensor B (Fig. 8-right) additional satellite nwell collecting electrodes are connected to the central one. The expected performance improvements with the APSEL3 chips are summarized in Tab. 1. In the table results from fast simulation have been corrected for the 20% overestimated collected signal.

Table 1: Expected performance for the APSEL3 pixel versions. Results from fast simulation have been corrected for the 20% overestimated collected signal.

Pixel Version	Sensor Geometry	Pixel Noise ENC	Efficiency (cut @ 5xnoise)	S/N
APSEL2 (data)	A	50 e-	88.7%	14
APSEL3-FE1	A	41 e-	93.6%	16
APSEL3-FE1	B	41 e-	99.4%	18
APSEL3-FE2	A	31 e-	98.6%	22
APSEL3-FE2	B	31 e-	99.9%	24

5.1 Data-Driven Sparsified Readout for CMOS MAPS

For the SuperB Layer 0 it is crucial to develop a fast readout for the MAPS matrix. Based on the new DNW MAPS design a dedicated readout architecture to perform on-chip data sparsification is currently under development. The architecture is data-driven to permit the use of the tracker information to generate a first level trigger. In an environment such as SuperB, silicon tracker information could be useful to realize a track trigger to reduce the high rate of Bhabha events.

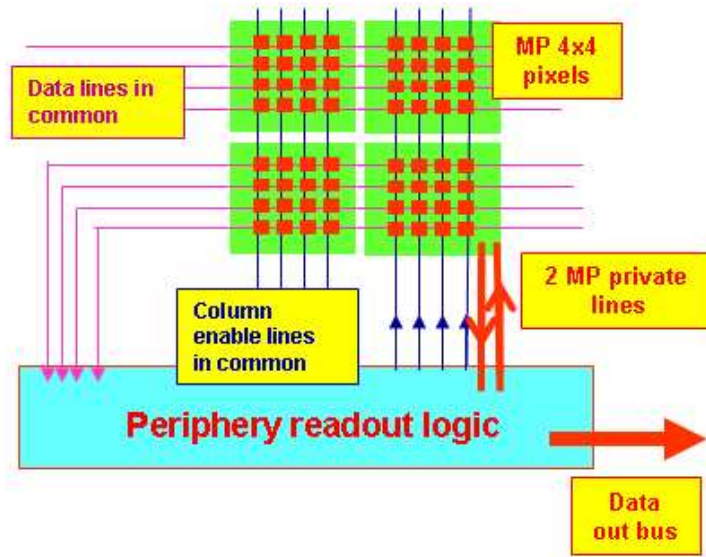


Figure 9: Schematic concept of the architecture for MAPS matrix readout: each MacroPixel has two private lines for point to point connection toward the periphery readout logic: one line is used to communicate that the MP has got hits, the other freezes the MP until it has been read out. Common vertical lines are shared among pixels in the same column to enable the readout of the column. Common horizontal lines are shared among pixels in the same row to bring data from the pixels to the periphery.

The key issues in this development are 1) to minimize logical blocks with PMOS inside the active area, to preserve the collection efficiency, and 2) to reduce to a minimum the digital lines crossing the sensor area, to allow the readout scalability to larger matrices and to reduce the residual crosstalk effects. With these criteria a readout logic in the periphery of the matrix has been

developed, as schematically shown in Fig.9. To minimize the digital lines crossing the active area pixels are organized in MacroPixels (MP) with 4x4 pixels, and each MP has only two private lines for point to point connection to the readout logic: one line is used to communicate to the readout that the MP has got hits, while the second private line is used to freeze the MP until it has been read out. When the matrix has some hits the readout logic sweeps the matrix by searching fired MPs, then it enables the readout of an entire column of pixels using a shared vertical line. Common horizontal lines are shared among pixels in the same row to bring data from the pixels to the periphery readout logic that sparsifies and formats the data to the output bus.

With the improved APSEL3 cell design (sensor shape A, 50 μm pitch) the APSEL3D chip has been fabricated. It includes a 256 pixel matrix with a data driven sparsified readout and timestamp information for the hits. The chip has been realized following the concept described earlier with a mixed mode design approach. While the pixel matrix has a full custom design and layout, the periphery readout architecture has been synthesized in standard cell starting from a VHDL model; automatic place-and-route tools have been used for the layout of the readout logic [16]. Using the VHDL model of the chip and MonteCarlo generated hit patterns encouraging preliminary results on hit efficiency have been obtained: running with a 40 MHz readout clock hit efficiency above 99% have been measured with hit rate up to several hundreds of MHz/cm^2 .

6. Conclusions

With a high luminosity B-Factory flavour physics could play a crucial role in the next decade in the search for New Physics beyond the Standard Model. A new concept for a SuperB collider has been proposed to reach and exceed a luminosity of $10^{36}\text{cm}^{-2}\text{s}^{-1}$ with modest beam currents. In the new collider scheme the beam energy asymmetry will be reduced with respect to the present B-Factories imposing more stringent requirements on vertex resolution, which is crucial for all time-dependent measurements. The required vertex resolution could be achieved in SuperB with a vertex detector based on the *BABAR* SVT layout with an additional Layer 0, very close to the collision point ($r \simeq 1.5\text{cm}$), with low material budget ($\simeq 0.5\%X_0$) and able to cope with the expected background rate (about $5\text{MHz}/\text{cm}^2$). Several options for Layer 0 design have been presented in the SuperB CDR. The one based on CMOS MAPS, potentially very thin, offers more margin against background occupancy and looks very promising.

The SLIM5 Collaboration has recently proposed a new approach in the design of CMOS MAPS, exploiting the Deep NWell option available in commercial CMOS process. With this new design several DNW CMOS MAPS chips have been fabricated with the STMicroelectronics 130 nm triple well technology. They implement a full in-pixel signal processing chain allowing the realization of a sparsified readout for thin MAPS sensors. Characterization of the second generation of the chips, APSEL2, has been reported. Good sensitivity to electrons from a ^{90}Sr source has been measured with improved pixel noise and threshold dispersion with respect to the previous prototype chips. A third generation of the APSEL chips has been recently fabricated with a substantial redesign of the pixel cell to improve noise figure, power consumption and charge collection efficiency. The development of a data-driven sparsified readout architecture has started and a 256 pixel matrix with the latest pixel version has been just realized. A 4k pixel matrix will be in pro-

duction by the end of 2007 and will be tested with beams (August 2008) to measure rate capability, efficiency and resolution.

The new approach in the design of DNW MAPS is very promising to develop a thin pixel system with a fast sparsified readout suitable for the application in the SuperB Layer 0. Extensive R&D on this new technology is under way on several key aspects with very encouraging preliminary results.

References

- [1] The SuperB Collaboration, "SuperB: A High-Luminosity Asymmetric e^+e^- Super Flavor Factory. Conceptual Design Report", *SLAC-R-856, INFN-AE-07-02, LAL-07-15 (2007) arXiv:0709.0451v2*
- [2] J. Hewett et al., "The Discovery Potential of a SuperB Factory", *SLAC-R-709 (2004)*.
- [3] B. Aubert et al. [BABAR Collaboration], "The BABAR Detector" *Nucl. Instrum. Methods*, **A79 1** (2002).
- [4] The BABAR Collaboration, "Letter of Intent for the Study of CP Violation and Heavy Flavor Physics at PEP-II", *SLAC-443 (1994)*.
- [5] W.R. Innes, "TRACKERR: A Program for calculating tracking errors" *SLAC-BABAR-NOTE 121 (1993)*.
- [6] N. Neri et al., "Vertex Detector Concept for a SuperB Factory", *Nucl. Instrum. Methods*, **A582** (2007) 811.
- [7] R. Turchetta et al., "A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology" *Nucl. Instrum. Methods*, **A458** (2001) 677.
- [8] G. Deptuch et al., "Design and Testing of Monolithic Active Pixel Sensors for Charged Particle Tracking", *IEEE Trans. Nucl. Sci.* **49** (2002) 601.
- [9] H. S. Matis et al., "Novel Integrated CMOS Sensor Circuits", *IEEE Trans. Nucl. Sci.* **50** (2004) 1020.
- [10] D. Passeri et al., "RAPS: an innovative active pixel for particle detection integrated in CMOS technology", *Nucl. Instrum. Methods*, **A518** (2004) 482.
- [11] G. Varner et al., "Development of a super B-factory monolithic active pixel detector-the Continuous Acquisition Pixel (CAP) prototypes", *Nucl. Instrum. Methods*, **A541** (2005) 166.
- [12] SLIM5 Collaboration - Silicon detectors with Low Interaction with Material, <http://www.pi.infn.it/slim5/>
- [13] <http://cmp.imag.fr/>
- [14] G. Rizzo et al., "Novel monolithic active pixel detector in 0.13 μm triple well CMOS technology with sensor level analog processing", *2005 IEEE Nuclear Science Symposium, Puerto Rico, October 24-27, 2005*.
- [15] F. Forti et al., "Development of 130 nm Monolithic Active Pixels with In-Pixel Signal Processing", L. Ratti et al.; "Design and Performance of Analog Circuits for DNW-MAPS in 100-nm-scale CMOS Technology", *2006 IEEE Nuclear Science Symposium, San Diego (USA), October 30-November 2, 2006*
- [16] A. Gabrielli et al., "Proposal of a data sparsification unit for a mixed-mode MAPS detector", *2007 IEEE Nuclear Science Symposium, Honolulu (USA), October 27-November 3, 2007*.