

Radiation Damage Study of the DØ Silicon Microstrip Tracker

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The Run II DØ experiment at the Fermilab Tevatron collider has been operating since 2001. At the heart of the DØ tracking system is a silicon microstrip detector. It is built from four layers of single sided and double sided sensors organized in six barrels, and two sets of seven disks. An additional, very small radius layer of silicon sensors, consisting of eight barrels, was inserted during the spring of 2006.

We monitor the silicon sensors for radiation damage. A bulk carrier-type reversal was observed in the innermost layer of the original detector after 1.5 fb^{-1} of integrated luminosity. We present the results of aging studies and predictions for lifetime of the detector for the rest of Run II at the Tevatron.

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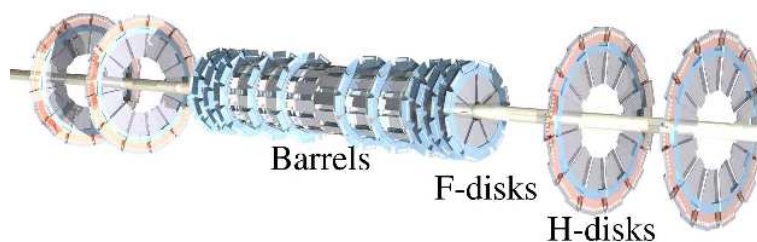


Figure 1: The DØ Silicon Microstrip Tracker. Layer 0, installed in the spring of 2006, is not shown. Also note that the outermost H-disk on each side was removed during the Layer 0 installation.

1. Introduction

The Run II DØ detector has been operating since March 1, 2001. It consists of two central tracking detectors inside a 2 T solenoidal magnet; central and forward preshower systems; liquid argon calorimeters; and muon spectrometers with a 1.8 T torodial magnet.

The Silicon Microstrip Tracker (SMT) is the innermost tracking detector at DØ. It contains six four-layer barrels; twelve small radius "F-disks" interspersed with, and forward of the barrels; and two large radius "H-disks." Formerly, there were four H-disks, but two were removed in the spring of 2006. This was done to accommodate the installation of a new layer of silicon sensors at small radius (Layer 0), consisting of eight barrels. It was installed to mitigate the anticipated degradation of the first layer of the SMT from radiation damage. All layers of the SMT barrels consist of two staggered sublayers to ensure full coverage in ϕ . An isometric view of the SMT, prior to the installation of Layer 0, is shown in Figure 1.

A variety of sensor configurations are used in the SMT. Layer 0 consists of only single sided devices. The first and third layers of the outermost barrels (excluding Layer 0) also consist of single sided devices. The remaining sensors in these layers are double sided double metal (DSDM) sensors with a 90° stereo angle. All sensors in the second and fourth layers are double sided (DS) devices with a 2° stereo angle.

Here we present measurements of the depletion voltage of the SMT barrel sensors. We make these measurements by studying the charge collection efficiency of the sensors as a function of applied bias voltage. We also extract the depletion voltage of some double sided sensors from studies of the n-side noise. Both methods are part of an ongoing program to monitor the status of the the DØ silicon tracker. These measurements are fit to the Hamburg model of the aging of silicon detectors [1].

From these fits we predict the depletion voltages for the SMT after 8 fb^{-1} of delivered luminosity. Micro-discharge and the breakdown of the AC coupling capacitors on the sensors limit the applied bias voltage to less than $\sim 150 \text{ V}$ (the Layer 0 devices can tolerate voltages in excess of 200 V). Our current projections indicate that full depletion of all sensors in Layer 1 may not be possible at the end of Run II. We expect that full depletion of Layer 0 should remain achievable.

2. Aging Studies of the DØ Silicon Tracker

The bulk material of the silicon sensors at DØ was initially slightly n-doped. One effect of

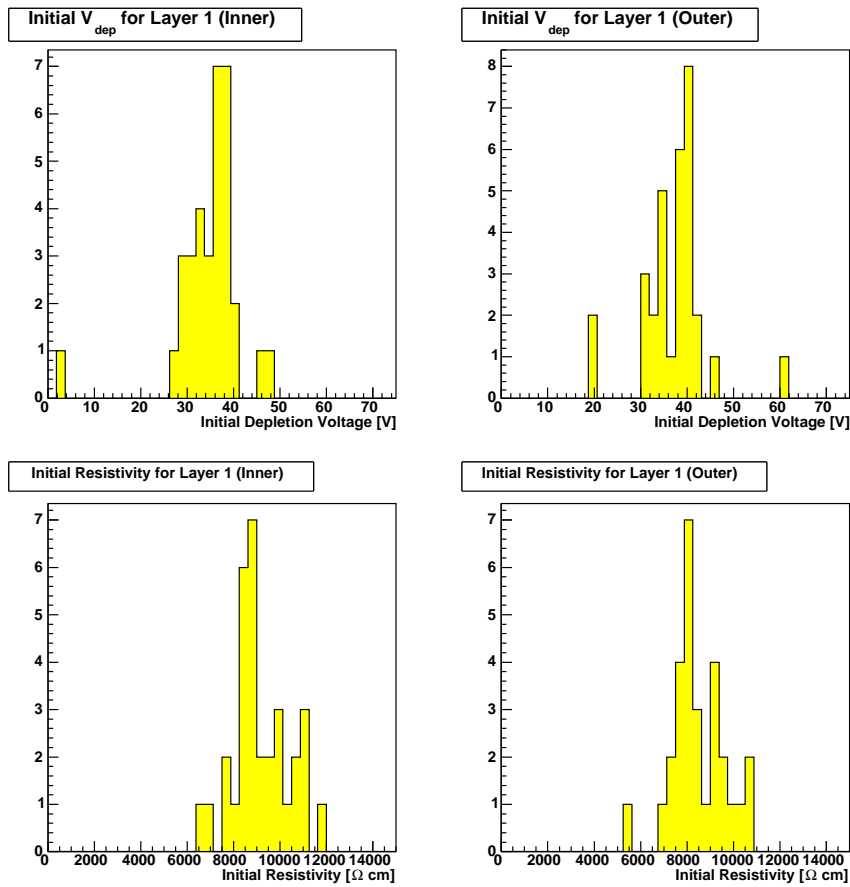


Figure 2: Initial depletion voltages (top) and resistivities (bottom) for the inner (left) and outer (right) sub-layers of SMT layer 1.

radiation exposure of these sensors is to reduce the n-doping concentration of the bulk. Eventually the sensors become p-doped (type-inversion). As the doping concentration decreases, so does the depletion voltage for the sensor. Once type inversion is reached, the depletion voltage begins to rise with the p-doping concentration. Distributions of the initial depletion voltages and resistivities of layer 1 of the SMT are shown in Figure 2. At the time of installation, the Layer 0 modules all had full depletion voltages of 185 V and resistivities of 1970 Ω cm.

2.1 Noise on the n-side

In a silicon sensor with an n-type bulk material that is not fully depleted, the space charge region will be on the side of the n-side strips, while the region near the p-side strips will have no free charge. This will produce significant noise on the n-side that is independent of the applied bias voltage, until the sensor becomes fully depleted. When the depletion voltage is reached, the n-side noise will decrease substantially.

We exploit this behavior to determine the depletion voltage in DS sensors. The method is to measure the n-side noise as the bias voltage is varied, in eleven steps from 0% to 100% of the full

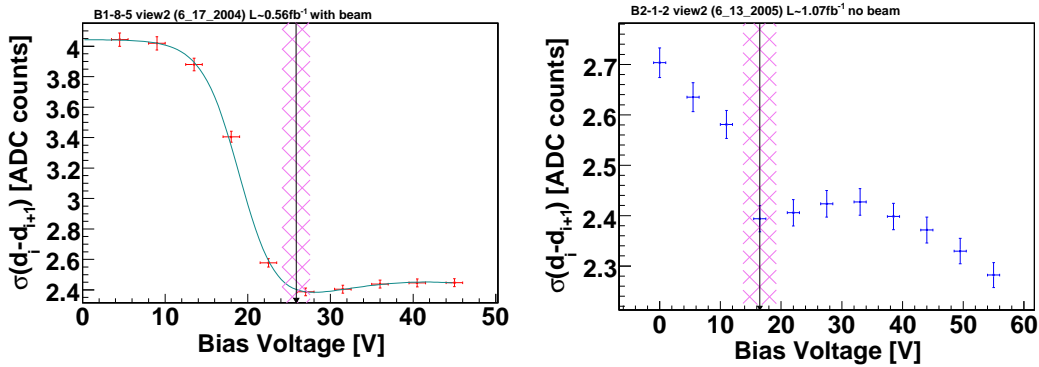


Figure 3: Results of noise scans for example DS (left) and DSDM (right) sensors.

voltage settings. These scans are done both with and without colliding beams in the Tevatron. No dependence on the accelerator state is observed.

The same method may be applied for DSDM sensors, although the noise dependence on the bias voltage appears significantly different in this case. For DSDM devices, the noise decreases continuously as a function of increased bias voltage. In some instances a kink in the curve is observed. This kink, when present, is interpreted as the depletion voltage. Examples of the noise scans for DS and DSDM sensors are shown in Figure 3.

A possible explanation of the DSDM noise behavior may be found in the more complicated structure of these devices [2]. The large stereo angle of the n-side strips on these sensors means that the connections from the strips to the readout chips must cross other strips. The connecting traces are in a second metal layer, separated from the strip implants by a very thin PEVCD (plasma enhanced chemical vapor deposition) insulating layer. Charge build-up in the PEVCD layer from radiation exposure could alter the noise behavior of DSDM sensors [3].

2.2 Charge Collection Efficiency

The second method we use to determine depletion voltages relies on measurements of the charge collection efficiency as a function of the applied voltage. The amount of charge collected when a minimally ionizing particle (MIP) traverses the bulk increases with bias voltage until the sensor is fully depleted. Higher voltages may yield a small increase in charge by decreasing the collection time.

The measurements are made by taking bias scans (as described in Section 2.1) while the Tevatron is delivering collisions. Data is taken without the usual "zero" suppression to provide sideband regions around each track, providing a per-event measurement of the noise. The position of the MIP peak is extracted from a fit of the signal distribution (corrected for incident angle of the track). As shown in Figure 4, the depletion voltage is defined to be the bias voltage for which the signal peak is 95% of the plateau value.

Figure 5 shows the measured depletion voltage as of 30 November 2008. At that date the original silicon sensors had been exposed to 5.4 fb^{-1} of luminosity, while the Layer 0 sensors had integrated only 3.8 fb^{-1} .

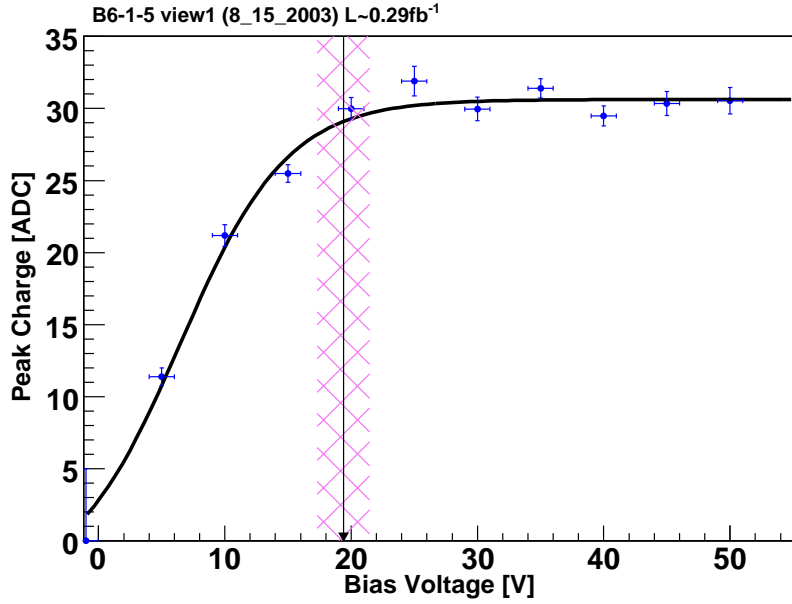


Figure 4: Measurement of the depletion voltage using charge collection efficiency for an example SMT sensor. The points represent measurements of the MIP peak in ADC counts. The curves represent fits of the points to a sigmoid function, while the vertical black line and purple hashed region indicate the depletion voltage (95% of the plateau) and uncertainty.

2.3 Fits and Projections

We use the Hamburg model [1] to translate our measurements of sensor depletion voltages into projections for a delivered luminosity of 8 fb^{-1} . Because annealing processes accounted for in the model are temperature dependent, we use archived data of the sensor temperatures as an input to our fits. Generally, the sensors have been kept at a temperature of 0° C , except for two shutdowns in 2004 and 2006. During these periods, the temperature was raised to 15° C .

The model predicts the depletion voltage of a silicon sensor as a function of a radiation dose measured in 1 MeV equivalent neutrons. To convert from integrated luminosity, \mathcal{L} , to an equivalent dose, Φ , we use the equation:

$$\Phi = \Phi_{1 \text{ cm}} r^p = \alpha r^p \mathcal{L} \quad (2.1)$$

where $\Phi_{1 \text{ cm}}$ is the dose for a sensor at a radius of 1 cm, p gives the radial dependence, and α is an empirical constant. We allow p to float in our fits, and measure a value of -1.33 ± 0.04 . For α we use the CDF Run I value of $2.2 \times 10^{13} \text{ cm}^{-2} / \text{fb}^{-1}$ [4].

Figure 6 shows the results of the fit for a sensor from Layer 1. The points displayed are from the n-side noise studies (black, open points), as well as the n-side and p-side charge collection studies (red and blue points). Because the n-side noise method does not provide a good measurement of the depletion voltage for sensors with a p-type bulk, these points are not used in the fit after type-inversion.

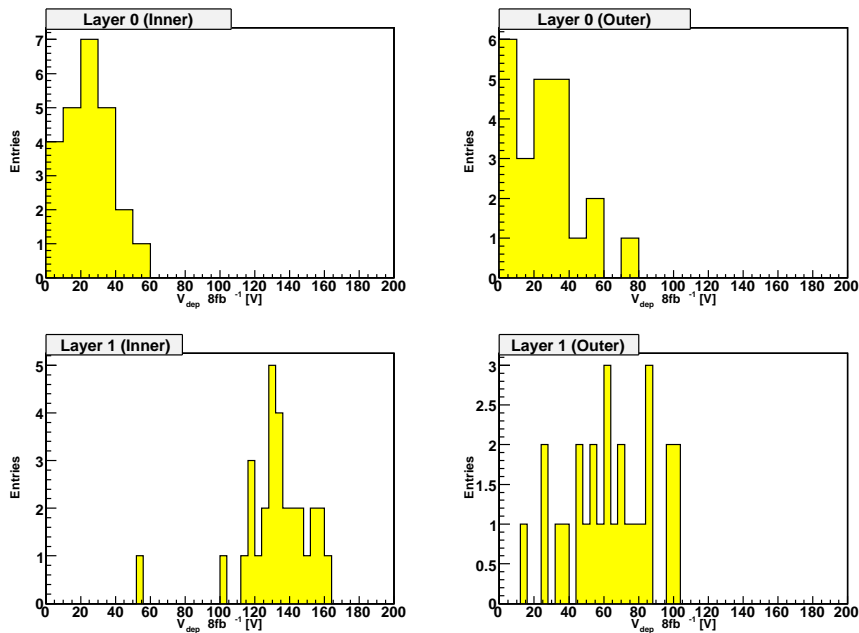


Figure 5: Measured depletion voltages for the innermost DØ SMT sensors at on 30 Nov. 2008. The Layer 0 sensors (top) were installed in 2006 and have been exposed to 3.8 fb^{-1} of luminosity, whereas the inner and outer layers (bottom) have been in place longer and received a dose of 5.4 fb^{-1} .

Figure 7 shows the expected depletion voltages for the Layer 0 and Layer 1 sensors at 8 fb^{-1} . We observe that all sensors in the inner sublayer of Layer 1 have undergone type inversion. Sensors from the outer sublayer are undergoing type inversion at the present time. This explains the large spread of projected voltages for that sublayer (bottom right on the figure): the interpretation of measurements near the type inversion point are ambiguous until subsequent data indicates that the depletion voltage has begun to rise again.

At voltages greater than approximately 150 V, micro-discharge in the oxide layers produces significant noise in the sensors from the original detector. Furthermore, the AC coupling capacitors on the devices cannot tolerate voltages beyond 150 V. Both effects limit the bias voltages that we can apply to the SMT (note that the Layer 0 sensors can function at significantly higher voltages). We currently project that some of the inner Layer 1 sensors will have depletion voltages greater than the maximum tolerable bias voltage by the end of Run II. We expect to be able to fully deplete the remaining sensors at larger radii.

3. Conclusions

The DØ collaboration has an ongoing program to monitor the radiation aging of the silicon microstrip tracker. We periodically measure the depletion voltages of our silicon sensors using both n-side noise and charge collection efficiency studies. We fit the resulting measurements as a function of delivered luminosity to the Hamburg model and make projections of the expected depletion voltages through 8 fb^{-1} . We currently estimate that we may not be able to fully deplete all

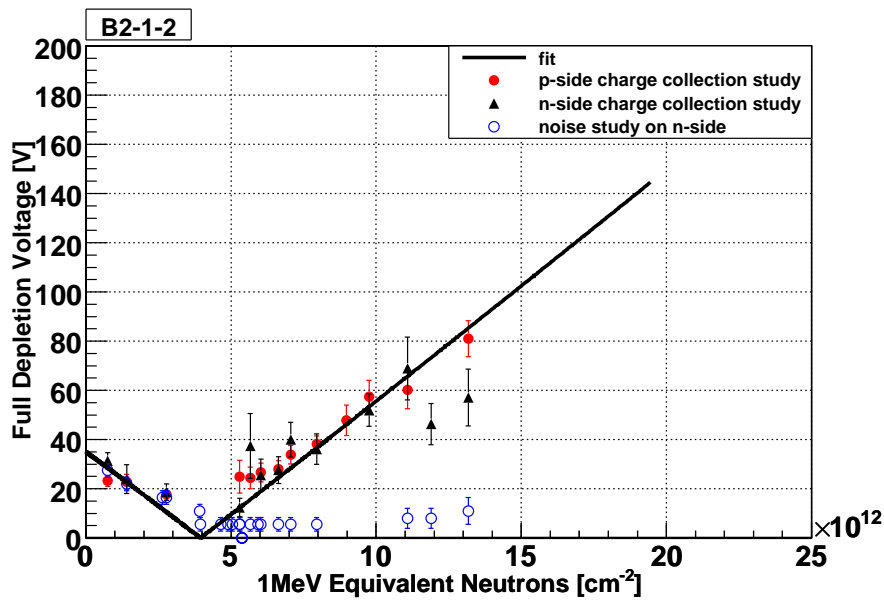


Figure 6: Fit to the Hamburg model for a sensor from Layer 1 of the SMT. The data from the n-side noise studies (black, open points) are not used in the fit after type inversion.

Layer 1 sensors by the end of Run II. However, it should be noted that this situation was anticipated, and was one of the primary motivations for the installation of Layer 0. We should be able to fully deplete the remaining SMT sensors, including Layer 0, through the remainder of the Tevatron run.

References

- [1] M. Moll, PhD Thesis, University of Hamburg, 1999.
- [2] F. Lehner, *The Construction and Performance of the 6-chip Silicon Ladders for the DØ Silicon Main Tracker*, DØ internal note 3846.
- [3] S. Burdin, *DØ Silicon Microstrip Tracker*, IEEE Nucl. Sci. Symp. Conf. Rec., Nov 2005, FERMILAB-CONF-05-506-E [arXiv:physics/0511173]
- [4] J. Matthews, *Effective Silicon Damage Fluences Measured by SVX and SVX'*, CDF public document 3937

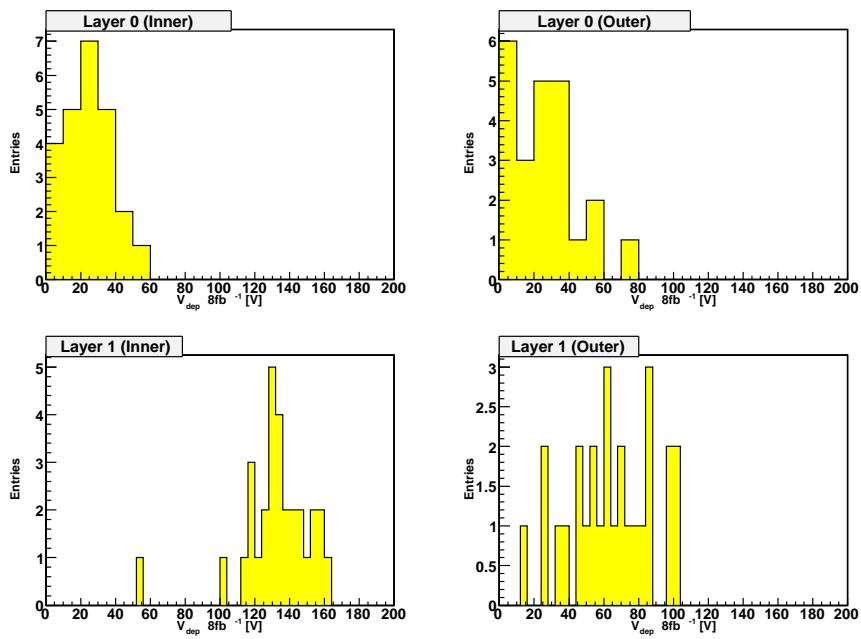


Figure 7: Projected depletion voltages for the innermost DØ SMT sensors at 8 fb^{-1} . The upper left and right plots show the expected depletion voltages for the inner and outer sublayers of Layer 0. The bottom left and right plots show the voltages for the inner and outer sublayers of Layer 1.