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Optimization of the new vertex detector for Belle

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In order to search for the new physics beyond the Standard Model, an upgrade of the Belle detector, so-called the Super Belle detector, will be carried out from 2009. According to the present schedule, it will commence data taking in 2012 with the primary target luminosity, $2 \times 10^{35}/\mathrm{cm}^2/\mathrm{s}$. Then we plan to gradually increase this up to $8 \times 10^{35}/\mathrm{cm}^2/\mathrm{s}$ within a few years operation. For this purpose, we have started the design of the silicon vertex detector including the geometrical configuration, the front-end chip and the choice of a possible technology for a pixel sensor. In this report, we will present the current status of this detector design.

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1. Status of the current Silicon Vertex Detector in Belle

The Belle detector [1] operating at the asymmetric energy e^+e^- collider KEKB [2] is a large solid angle magnetic spectrometer, with the primary aim of studying the *CP* violation in the decays of neutral B mesons, which is prediced in the Standard Model. The energies of e^+ and e^- are 3.5 GeV and 8 GeV, respectively, with the center-of-mass energy corresponding to the mass of the $\Upsilon(4S)$ resonance. Due to the boost of the center-of-mass system of $\beta\gamma = 0.425$, the average distance between the two B meson decay vertices is about 200μm. The key point of this experiment is to measure this distance with good precision. For this purpose, we installed a three-layer silicon vertex detector ("SVD1" [3]), which was composed of double-sided silicon strip detectors ("DSSD"), from the beginning of the experiment. However, SVD1 covers the polar angle range $23^\circ < \theta < 139^\circ$ that is smaller than the tracking central drift chamber (CDC) acceptance. In addition, the VA1 front-end readout chip [4] mounted on SVD1, which is only radiation tolerant to 1 MRad, has been exposed to radiation and the accumulated dose almost has reached the maximum level by the end of 2002.

During the Belle shutdown in 2003, the upgraded detector "SVD2" was installed in the place of the SVD1 and its operation has started in October 2003 successfully. The SVD2 was designed not only to cover the same angular acceptance of the CDC ($17^\circ < \theta < 150^\circ$), but also such that the first layer is as close as possible to the interaction point to reduce the effect of the multiple scattering in the vertex reconstruction. Furthermore, an additional layer was implemented as a forth layer. The layout of the SVD2 is shown in Fig.1 and the details are described elsewhere [5]. The front-end signal processing is performed by the VA1TA chip [4] which has 128 channels and radiation tolerance up to 20 MRad.

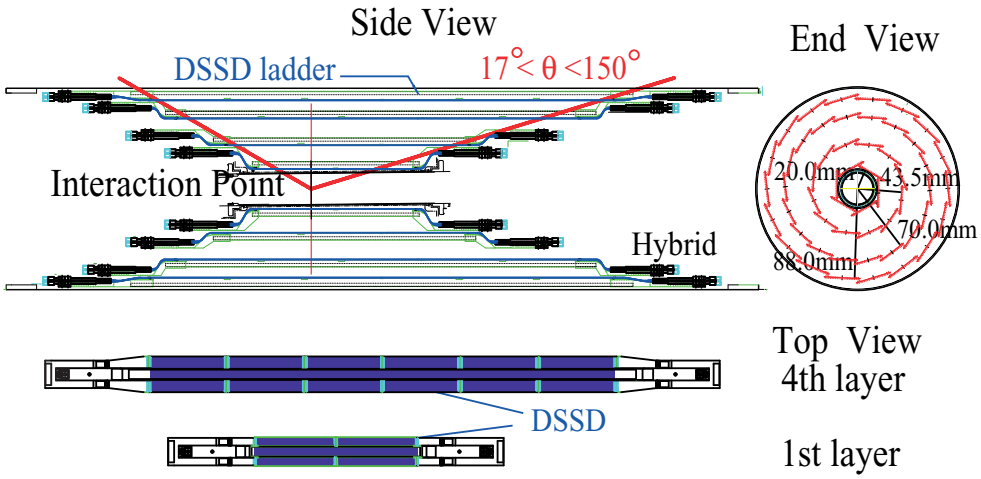

Figure 1: SVD2 design

Since the Belle experiment has commenced data taking in 1999, especially after installation of the SVD2, it has been hitherto operated smoothly. Although the integrated dose of ~800 kRad (since the installation of the SVD2) was reached in 2008 summer, this is much less than a limit of the radiation dose on the SVD2. The performance in reconstruction is also stable. For instance, the

efficiency for matching tracks between the SVD and the CDC has been kept 99% or more during the entire experiment period. Furthermore, from January 2007, the KEKB started the operation of the crab cavity. Thanks to this, we could achive the same level of the peak luminosity with a lower beam current and hold the occupancy in the first layer less than 10%. Due to these facts, we could accumulate the integrated luminosity of more than $\mathscr{L} = 850\,\mathrm{fb}^{-1}$ as of February 2008 and many remarkable results have been presented constantly so far [6], [7], [8].

2. The Super Belle Experiment

In order to achieve more precise measurements which are supposed to be sensitive to new physics beyond the Standard Model, the KEKB accelerator and the Belle detector are planned to be updated to the so-called Super KEKB accelerator and the Super Belle detector, respectively. According to the present schedule for the Super Belle, operation is anticipated to start in the middle of 2012. The primary target luminosity in the early stage is $2\times10^{35}/\mathrm{cm}^2/\mathrm{s}$ and we plan to gradually increase this up to $8\times10^{35}/\mathrm{cm}^2/\mathrm{s}$ within a few years. Because a detector upgrade takes three years according to our past experience, we should start the construction within the fiscal year 2009, that is, one year from now. Since we have to fix the detector configuration and technology choice immediately, we have decided our strategy for SVD upgrade as follows. For running in 2012, we will install an upgraded SVD with strip type sensors and a 1.5 cm radius beam pipe. A pixel sensor with a smaller radius beam pipe can replace the first and second layers as a further upgrade after a few years of operation. The former is defined as "baseline" SVD design and the latter as "ultimate" design in this report.

2.1 Specification of the baseline design

The specification of the geometrical design of the baseline is as follows. The radius of the beam pipe is 1.5 cm. The inner part of the present CDC cannot be operated at a higher luminosity because of the harsh beam background. Therefore we will replace this part with two additional SVD outer layers, which correspond to the fifth and sixth layers. The increased number of layers enables stand-alone tracking with the SVD and improves the tracking efficiency for low momentum particles. Moreover, this enlarged SVD allows an increase in the efficiency for reconstructing K^0_S decays. However, this also leads to a longer sensor, especially for the outer layers. As a result, the noise level will increase. To cope with this, a development of a special readout scheme, for example the "chip-on-sensor" method, is needed to maintain a good S/N performance. Note, however, that this would increase the material budget in the acceptance region. As for the forward and backward parts, the layers could be slanted or have a disk-type shape so that the ladder size and the number of readout channels can be reduced without losing acceptance.

The signals from a strip type sensor should be read out by a front-end chip, which has a short shaping time (~ 50 ns) to reduce the high occupancy induced by the harsh beam background. Since the L1 trigger rate would be very high (~ 10 kHz), a pipeline on the front-end chip is required.

In the following subsections we will show the detailed discussion of the design of the baseline SVD detector.

2.1.1 Requirement for the Front-end chip

The radius of the beam pipe strongly affects the performance of SVD. In particular, the impact parameter resolutions are determined by the radius and the material budget of the beam pipe, the position and the material of the first layer and the position of the second layer.

On the other hand, the closest the sensor is to the interaction region, the highest the expected occupancy is. Since the beam background level in the Super Belle is expected to be $\sim$15 times higher than in the current Belle configuration, the occupancy at the first layer will be a crucial problem. Since the number of fake clusters will increase dramatically and even signal clusters would be deformed by beam backgrounds, the trajectories of tracks reconstructed with fake and/or deformed clusters will be shifted from their true trajectories. Consequently, the hit resolution will deteriorate. Table 1 shows a rough estimation of the occupancy at each layer for the current Belle SVD at a luminosity of $2\times10^{35}/\mathrm{cm}^2/\mathrm{s}$. For simplicity, in this calculation we assume that the occupancy is proportional to the shaping time, the area of each readout channel and $1/r^2$, where r is the radial position of the layer from the interaction point.

Table 1: Estimated occupancy at each layer for the current Belle SVD and the baseline SVD design under a $\sim$15-time higher beam background level than in the current Belle configuration. The units are in %.

layer#	1	2	3	4	5	6
Current	$\sim$100	$\sim$100	15	15	-	-
Baseline	10	3	1	1	$<$1	$<$1

In order to reduce occupancy, finer segmentation of the readout channels is one solution. Further segmentation ($< 50\,\mu$m), however, is technically difficult and would increase the number of the total readout channels. A pixel type sensor, which has a small amount of material and a fast readout speed, has not been developed yet. Another approach is to suppress the overlaid beam background in the signal time-window by reducing the shaping time. In the Belle SVD, the shaping time of the readout chip, VA chip, is about 800 ns. Therefore, assuming a readout chip whose shaping time is 50 ns, we can reduce the occupancy by a factor of 1/16, theoretically. For the readout speed, the VA chip cannot be used even at the outer layers since it needs at least $12.8\,\mu$s to be read out and introduces a dead time fraction of more than 15% at the 10 kHz L1 trigger rate.

Taking these into account, a front-end chip that has both a shorter shaping time ($\sim$ 50 nsec) and a pipelined readout scheme is required for all layers to overcome the higher beam background without degrading the performance. At this stage, the "APV25" chip [9] that has been developed for the CMS Si tracker fulfills the above requirements and is one possible solution.

From the MC study, assuming that the front-end chips of the first and second layers are to be APV25's, the Δz vertex resolution for $B \to J/\Psi K^0_S$ can be maintained at the same level that has been achieved by the current SVD even if the beam background level is six times higher (See Fig. 2). Here, the Δz vertex resolution is defined as the difference between the distance obtained from the two reconstructed B decay vertices and the true distance. Under the 15 times higher beam background, we observed roughly 20% degradation for the baseline design relative to the current SVD. However, this could be recovered by analyzing the recorded pulse shape, which is another remakable feature of the APV25 chip.

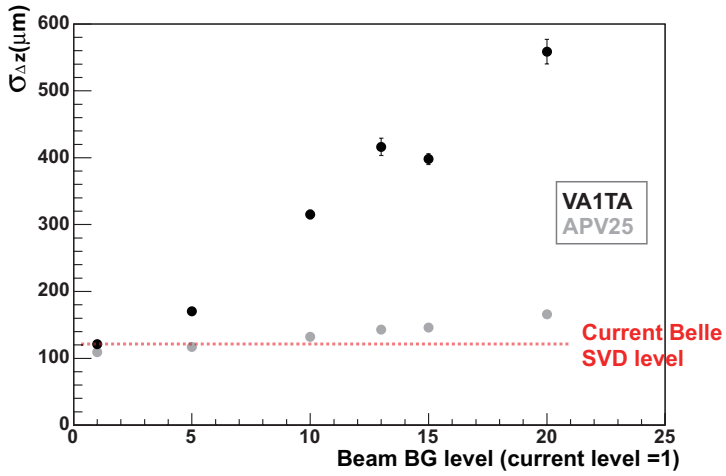

Figure 2: Δz vertex resolution as a function of the beam background level relative to the current Belle background level: APV25 (gray) and VA1TA (black)

2.1.2 Geometrical design

To increase the vertexing efficiency for the K^0_S from the $B \to K^{0*}\gamma$ decay chain, which is one of the most important modes used to explore physics beyond the Standard Model, the SVD volume is enlarged in the radial direction. Due to the expansion of the SVD volume, the detector, especially in the two outermost layers, becomes longer. This leads to an increase of the detector capacitance and leakage current. Consequently, the noise level becomes larger. Furthermore, the shorter shaping time also results in higher intrinsic electronic noise. Because a degraded S/N ratio affects the total performance of the SVD, especially for the events including K^0_S, it is important to evaluate the effect of the poor S/N ratio at the outer layers.

For this purpose, we performed the simulation study using K^0_S in $B^+ \to K^0_S\pi^+$ decays with changing the noise levels in the two outermost layers. Figure 3 shows the efficiency for matching tracks between the SVD and the CDC. It also shows the S/N ratio for all the layers should be better than a third of that in the current Belle SVD, which is roughly 35 for the inner layers and about 16 for the outer layers. Otherwise, the efficiency for matching tracks will degrade. In particular in K^0_S vertexing, we would lose 60% of tracks that decay between the fourth and fifth layers if the noise level is three times higher than in the current Belle SVD [1]. A possible solution is to make use of a relatively established technology, e.g., "chip-on-sensor"(See Fig. 4), which can avoid the ganging of sensors. However, to realize this we need to clarify the material budget of the chips and the cooling systems (the choice of the coolant, the flow rate of the coolant circulation, the material of the cooling pipe and must test the temperature/pressure tolerance, the leackge of the coolant, corrosion, clogging and the connection of the cooling pipe to the outside), the number of readout channels, the support structure and the space for the cabling and so on.

The effect of the additional material is studied with simulation. For physics that aims at *CP* violation, for instance, $B \to J/\Psi K^0_S$, $\pi^+\pi^-$ and D^+D^-, increasing the amount of material in the

[1] To reconstruct K^0_S using its decay products $\pi^+\pi^-$, at least two SVD hits are required for each charged pion track.

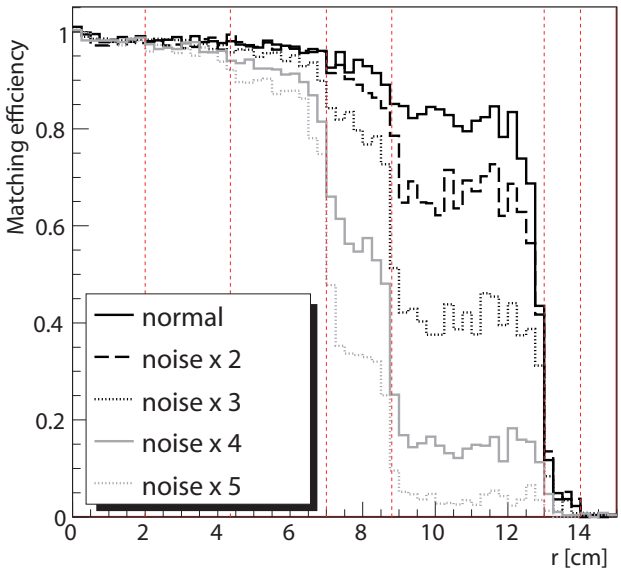

Figure 3: The efficiency for matching tracks between the CDC and the SVD as a function of the K^0_S vertex position in $B^+ \to K^0_S \pi^+$ for different noise levels. If the noise level is three times higher than that of the present Belle SVD (the S/N ratio is around 35 for the inner layers and around 16 for the outer layers), the gain from the extra coverage by the outer layers is reduced by 50%.

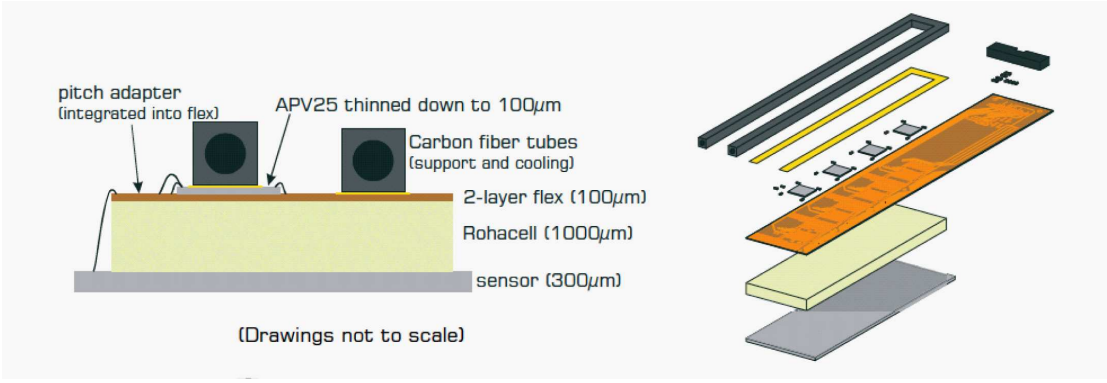

Figure 4: The schematic of the chip-on-sensor technology.

first and second layers degrades the Δz vertex resolution by roughly 10%. Therefore we recommend that the chip-on-sensor should not be adopted for the first and second layers. On the other hand, for the outer layers (the two outermost layers), we have to compromise because the degradation from S/N is more serious than that from the increase in material budget.

Another side effect of the expansion of the SVD volume is an increase of the number of readout channels. Moreover, the chip-on-sensor technology will be applied to maintain the current level of S/N, especially for the outer layers. In this case, the number of readout channels would increase

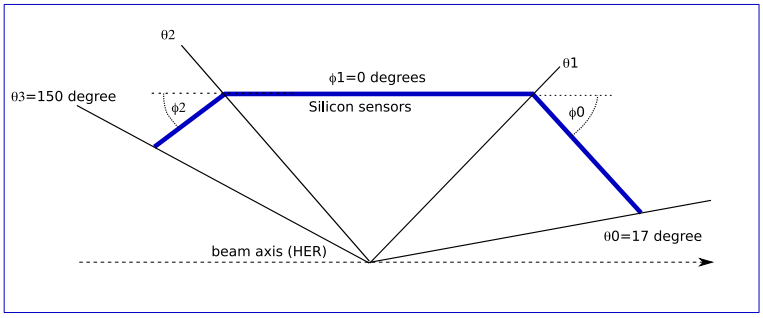

Figure 5: The schematic of a SVD ladder, with slanted sensors in the forward and backward regions with the definition of angles used for the optimization.

drastically. In order to explore the possibility that the number of readout channels in the outer layers can be reduced without degrading the performance, a MC study was carried out with $B \to K^{0*}\gamma$ decay. In this simulation, the z-side strip pitch, which is nominally 73 μm, was increased by a factor of two or four and then the *CP* side vertex resolution was examined. From this study, we conclude that the wider strip pitch seems to be feasible. However, considering the degradation caused by the increased material to maintain the current level of S/N, further degradation from a wider strip pitch is no longer acceptable. As an alternative solution, the introduction of an arch-shaped detector or a slanted detector is recommended.

When the arch-shaped detector or the slanted detector configuration (See Fig. 5) is considered, one can optimize by minimizing the average incidence angle of tracks from the interaction point to the sensor. Thanks to this optimization, we will find a better resolution than the case without an arch-shaped or slanted detector. Furthermore, the total area covered by sensors also can be reduced, which directly reduces the cost. However, if the fifth layer is located at $r = 12$ cm in the optimized design, roughly 8% of K^0_S's would be lost. There is still much room to optimize the arch-shaped or slanted part to optimize the tracking performance, the track matching efficiency between CDC and SVD, the detection efficiency for the K^0_S and the effect of the beam background. This should be clarified before the final decision on the SVD design.

2.2 Specification of the ultimate design

After a few years of operation of the Super Belle detector with the baseline design, a pixel sensor with a 1.0 cm radius beam pipe can replace the first and second layers of SVD with a 1.5 cm radius beam pipe. The location of the first layer will be at 1.3 cm from the interaction point (2.0 cm for the baseline design). In that case, the first layer would be exposed to several MRad/year corresponding to a 33-time higher beam background at maximum and DSSDs can not survive anymore under this severe condition. Therefore we need a pixel type detector with a pipeline readout scheme, especially for the first and second layers. At this stage, there are three possible technology candidates which could be realized within a couple of years. It is required to evaluate these cnadidates and to decide the technology soon. For the outer layers (from the third to sixth layers), we will use the same configuration of the baseline design.

2.2.1 Technology choice

Though there are three pixel type sensors which are applicable for the second stage of the Super Belle experiment, "DEPFET" [10], "CMOS pixel" [11] and "SOI" [12], each of these has advantages and disadvantages. For example, the size of the DEPFET sensor could be as large as $50\,\mu\text{m} \times 75\,\mu\text{m}/\text{pixel} : 215 \times 512$ pixels, which is limited by a wafer size and the thickness would be reduced up to $20-100\,\mu$m depending on the experimental condition. Furthermore the DEPFET is an established technology beacause it has been used in several experiments already. However, the radiation tolerance is tested up to 1MRad which is less than the expected radiation. As another example, the SOI would be tolerant for the radiation up to 30MRad. But its sensor size is limited by the reticle size ($20\,\mu\text{m} \times 20,\mu\text{m} : 128 \times 128$ pixels), which is smaller than our request. And the most crucial disadvantage is that research and development are still in progress. Table 2 shows a summary of the current status of each technology. At this moment, we have not decided the technology. We will have to fix this in parallel with the hardware development.

Table 2: Technology choices for the pixel type vertex detector in the ultimate design.

	DEPFET	CMOS(CAPS/MAPS)	SOI
Material budget	$20-100\,\mu$m (adjustable)	$\sim 50\mu$m (sensitive area $5-10\mu$m)	$50-100\mu$m (could be $\sim \mu$m)
Size	limitex by wafer ($50 \times 75\text{mm}^2$)	limited by reticle ($21 \times 21\text{mm}^2$)	limited by reticle ($21 \times 21\text{mm}^2$)
Power consumption	small (0.5W)	small	small
Radiation hardness (3MRad/yr)	tested < 1 MRad (up to 8MRad)	intrinsic rad. hard (must be > 30MRad)	tested > 30 MRad
10 kHz trigger rate	estimated ~ 1 % ineff.	not proved	not proved
Availability	MPI only (alread used in other exp.)	R&D in progress	R&D in progress

2.3 Summary

Since the beginning of the Belle experiment, the silicon vertex detector has been operated successfully. The observed performace are satisfying and many epoch-making analyses have been done. The operation will be continued in the next fiscal year.

To search for the new physics beyond the Standard Model, an upgrade of the Belle detector will be carried out during three years shutdown (2009-2012). According to the present schedule for the Super Belle, the primary target luminosity in the early stage is $2 \times 10^{35}/\text{cm}^2/\text{s}$ and we plan to gradually increase this up to $8 \times 10^{35}/\text{cm}^2/\text{s}$ with in a few years operation. For the early stage, we will install an upgraded strip-type silicon vertex detector with a 1.5 cm raidus beam pipe ("baseline" design). Then a pixel type vertex detector with a smaller radius beam pipe can replace the first and second layers for the higher-luminosity stage ("ultimate" design). We almost have fixed the baseline design based on the requirements from the physics, the beam background level,

the limitation of the structure and so on. For the ultimate design, though we have not decided the technology yet, we will have to fix this in parallel with the hardware development.

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