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Pixel-based Vertex and Tracking Detectors for ILC

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The ILC vertex detectors (there will be two, one for each of two general purpose detectors) will certainly be built with monolithic or vertically integrated pixel detectors. However, beyond this statement, there is a wide range of options supported by active R&D programmes all over the world. These options are discussed briefly, with indications that many of them have potential for application in other fields, where imaging systems with fast frame rates (typically in burst mode) are needed. Synchrotron radiation facilities, both 3rd generation and (with much more extreme requirements) 4th generation systems, have large overlaps. Regarding tracking systems, the past year has seen the emergence of a conceptual 40 Gpixel tracking system as a candidate to satisfy the ILC conditions. The capabilities of such a system may be unique in delivering a material budget of <0.1 X over the full angular range, as is desired for ILC physics. The special characteristics of a promising pixel-ased system are discussed.

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1.Introduction

The International Linear Collider (ILC) will present considerable challenges in all three major subsystems, tracking, calorimetry and vertexing. These areas were subject to in-depth reviews during 2007; the reports of the review committees can be found at [1].

At ILC, physics requirements demand the capability to reconstruct multi-jet events with highly efficient and precise tracking, as well as reconstruction of photons from π^0s etc in each jet. These events frequently have one or more jets thrown into the forward region, so the requirement of excellent tracking, combined with high transparency for photons, applies as much in the forward as in the central region, down to the limit of ~7^o polar angle. This contrasts with previous '4-π' detectors, for which one could tolerate reduced tracking performance and increased material in the region below the coverage of the central tracker. The desirable upper limit on material is around 0.1 X_0 for the full tracking system. In the Tracking Review held in March 2007 in Beijing, we heard about three options, a TPC, a silicon microstrip tracker, and a low-mass drift chamber. The conclusion from the review committee, which included experts on all these technologies, was that for the first two the material budget goal would be extremely difficult to achieve, while for the drift chamber, the track density in high energy jets would be very challenging. Mulling over these issues, the idea arose of a tracking system based entirely on monolithic pixel sensors. While this would not be feasible today, it can probably be developed to satisfy all the ILC requirements over the next decade. This new concept is discussed in Section 3.

The Vertexing Review was held in October 2007 in Fermilab, where we heard of approximately 10 technology options that might be developed to satisfy the ILC requirements. All are based on some form of monolithic pixel sensor, and all hope to achieve a material budget of ~0.1% X0 per layer, considerably more ambitious than the requirements for the main tracker. This challenging requirement is driven particularly by the need to associate low momentum tracks with their true parent vertex, which is needed in order to determine the 'vertex charge', the charge sign of the leading quark in heavy flavour jets. This goal for the material budget is realistic, given the use of thin monolithic pixel detectors and the fact that the vertex detector is much more compact than the tracker. The options now being studied for the ILC vertex detectors are discussed in Section 2.

One of the concerns associated with all these R&D activities is the uncertainty regarding the ILC timescale. The Vertex 2008 workshop was particularly useful in awakening us to the large overlap between the ILC technology requirements in these areas and requirements for other fields of science. Following after the workshop, this opportunity for synergy gave rise to a proposal for a world-wide inter-disciplinary network activity. At the time of writing, this suggestion has been welcomed by lab directors in the three regions (Rolf Heuer, Young-Kee Kim and Fumihiko Takasaki) who are in the process of appointing a 6-member Coordination Board to organise activities of this Pixel Network Group. It may be that this group, following on the successful example from the ILC accelerator R&D community, will appoint 'topic facilitators', who will be responsible for world-wide networking between the active groups working on each selected topic. So while this report presents the current status of R&D in the context of pixel detectors for ILC, it is hoped that it may also be useful in illustrating points of contact which emerged during discussions at the Vertex 2008 workshop, in which the potential applicability of these sensors to other areas of science became apparent to all present. In a real sense, this workshop provided the 'kickoff meeting' for this interdisciplinary initiative.

2. ILC vertex detector R&D

A number of classes of devices is considered, which can be categorised in roughly increasing order of complexity as CCDs, monolithic pixels (NMOS only), monolithic pixels (full CMOS), the ISIS option (CCD-in-CMOS), the DEPFET (in-house process), and most adventurously, SOI and vertically integrated options. Slides of the talks presented in the Vertex Detector Review provide details [2]. Here we list just a few of the key points for each option, as well as 'possible showstoppers'. The point of this is not to be negative; on the contrary, we have to acknowledge that there are major R&D issues for each technology, and to suggest otherwise would be to provide ammunition to funding agencies which urge reviewers to 'pick winners'. While this could be seemingly more cost effective, it would be most unfortunate to discourage R&D in the one option which might eventually prove to be the winner. Even if it were possible to rule out one of the current suggestions for the ILC, there are other application areas in which it might be a winner (as has already happened with CCDs, DEPFET and certain MAPS architectures). The best approach by far is to leave it to the R&D groups and their funding agencies to take the decisions to continue support, or down-select, or change direction, on the basis of their detailed understanding of all the issues. Over the past few years, some ideas have indeed been dropped (eg the macropixel/micropixel hybrid) and this type of healthy

internal adjustment will doubtless continue as the world-wide R&D activities evolve, sustained by the information network which constantly extends our vision.

Building on the 307 Mpixel SLD vertex detector, one approach is to continue with the CCD technology. However, this presents a basic problem, namely the accumulated background through the 1 ms ILC bunch train, which could lead to excessive pixel occupancies, particularly on the innermost layer. Within the boundaries of this technology, groups are pursuing two possible solutions.

The column parallel CCD (CPCCD) approach permits fast transfer of signal charge (50 MHz row clocking) to a readout chip with independent parallel processing of the signals from each column (20 μm pitch). This approach allows the detector to be read out at 50 μs intervals, 20 times during each bunch train, thereby reducing the background to a tolerable level. A disadvantage is the high power during the bunch train, leading to serious concerns about the additional material associated with local capacitors and power distribution systems.

The fine pixel CCD (FPCCD) approach lives with the higher background associated with once-per-train readout, and compensates for the higher hit density by smaller pixels (5 μm, a reduction in area by a factor 16). Furthermore, by implementing closely spaced pairs of layers, mini-vectors can be found which permit reasonably efficient suppression of the background hits, since these come mostly from low energy pair electrons from beamstrahlung photons produced at the IP. Double layers will inevitably imply a somewhat increased material budget, which is particularly critical for the innermost layer. A possible showstopper would arise if the final focus option for the machine (eg the Low-Power option), combined with a somewhat reduced suppression factor for pair electrons, leads to an unacceptably high hit density on the innermost layer.

Moving beyond CCD technology, the next step in complexity is monolithic active pixel (MAPS) devices, where the front-end signal processing is done within the pixel. The simplest form is the 3T architecture, in which the signal is collected on a reverse-biased diode which is directly connected to the gate of the signal-sensing source follower circuit. Given the component densities possible with deep submicron (DSM) CMOS, additional electronics can be accommodated within a 20 μm pixel, for example a comparator or logic for correlated double sampling (CDS). However, with this architecture, one is restricted to NMOS transistors only, since PMOS devices would compete with the charge collecting diode, leading to systematically

reduced MIP detection efficiency for parts of each pixel. The MIMOSA approach retains the simple pixel functionality, and places full CMOS logic for ADCs and data sparsification on each row along the long edge of the ladder. This 'row-parallel' approach (as opposed to column parallel, which implies readout at the short ends of the ladder) is needed in order to achieve the required frame readout rate during the bunch train. This architecture is limited to 'frame-rate' CDS, and is hence susceptible to low-frequency pickup during the signal integration time of ~25 μs. This represents a possible showstopper, depending on noise levels during the ILC bunch train.

Another approach that satisfies the restriction of NMOS transistors only, is the Continuously Active Pixel (CAP) architecture, which implements a string of storage capacitors in each pixel, thereby achieving time slicing through the train, possibly ~10 slices, where the limit is set by increased noise as the capacitor dimensions are reduced. A possible showstopper is inadequate pickup immunity due to charge-to-voltage conversion during the noisy bunch train.

Three approaches are being pursued which aim to liberate the pixel functionality to full CMOS, while preserving full efficiency for MIPs. One of them involves a novel twist to the CMOS triple-well process, while the others take advantage of the deep p+ shielding implant that was developed for enhanced pixel performance by FillFactory in the early '90s.

The deep n-well approach collects signal charge on the n-well that houses the NMOS transistors for the analogue circuitry in the CMOS triple well process. This allows in-pixel data sparsification and time-stamping with ~30 μs precision. Although this is the largest n-well in the pixel, there are others that house the in-pixel PMOS transistors, and they inevitably compete for signal charge. The goal is for ~15 μm pixels with binary readout, for which full MIP efficiency may be achievable, but this has to be demonstrated, and inefficient regions within each pixel would constitute a showstopper for this approach.

The chronopixel architecture envisages a shielding p+ implant over most of the pixel area, allowing uninhibited use of CMOS circuitry for the charge sensing, comparator (with effectively full CDS) and binary readout of sparsified data. The goal is for 10 μm pixels, which with binary readout would deliver adequate precision even on Layer 1, but this will require 45 nm feature size, assuming this to become affordable for small-volume scientific devices on the ILC timescale. A possible showstopper might be an excessive power requirement for such fine

pixels each incorporating such complex logic, in the context of a gas-cooled compact detector system.

The ISIS approach also protects most of the pixel circuitry from collection of signal charge by means of a deep p+ layer, with small holes for the charge transfer from the epi layer to the photogates on a pitch of about 20 μm. The signal charge collected by each photogate is transferred at 50 μs intervals along a linear register (a CCD structure) that contains 20 storage elements. At the end of the bunch train, when the beam-related RF pickup has died down, the transfer continues at a leisurely pace, tipping each stored charge onto the very low capacitance of a typical buried channel CCD charge sensing circuit (source follower, reset FET and row-select transistor). Full CDS is implemented for each charge-to-voltage conversion, and this coupled with the low readout speed and the quiet electrical environment between bunch trains, should guarantee excellent noise performance. The readout of one frame can take as much as 10 ms, after which the next signals in the storage register are ready for transfer. The most likely showstopper is the combination of CCD and CMOS processing features in one device. While this is a trend within the industry for scientific imaging devices, there could be particular challenges such as the transfer of the small MIP signal charge through the tail of the deep p implant, at the first transfer from the photogate into the CCD register.

The DEPFET is another architecture which breaks away from standard CMOS processing, but in this case the special features have been developed in a dedicated in-house production facility, and so are more under the control of the design team. In this approach, the signal charge is stored in the silicon bulk, forming an internal gate. Complete clearing of the charge results in precise time-correlated determination of the signal (true pixel-level CDS). It uses column parallel rolling-shutter readout, reading row pairs synchronously in order to achieve the required frame rate. A possible showstopper is associated with the need for additional steering and signal processing chips. With such a complex system, the overall speed requirements may be difficult to achieve, when implemented on full-size ladders.

The most advanced design concept for this application is the silicon-on-insulator (SOI) or (even more adventurous) the vertically integrated (VI) technology. In both cases, the charge collection layer comprises a separate wafer, so its properties (resistivity etc) are chosen to best match those requirements. The charge collection pixels are each connected to one or more layers of electronics. In the VI approach, the sequential electronic functions (analogue front-end, digitisation, sparsification and readout) may be carried out on physically separate layers,

each 10 μm or less in thickness. If the desired processing goes beyond the capabilities of a monolithic device, or if the implications regarding feature size are too expensive (as may be the case for the chronopixel) escaping into the 3rd dimension, as offered by the VI approach, becomes attractive. The current suggestion is for small pixels (~10 μm square) with binary readout. At present, one is far from establishing the feasibility of such a system at the 4 Gpixel level, with possible concerns regarding mechanical stability of large multi-layer sandwiches operating at high power levels. However, it is impressive to see what 30 years ago was called the Z-plane technology now realised in practice. The functionality is reminiscent of the signal processing at the back of the retina, and lends itself to all sorts of parallelism in terms of pattern recognition (clusters, track segments etc) with potential for highly sparsified data.

Where are we heading with this large array of technology options? The general consensus in the ILC community at the time of the review was that one would develop full-sized prototype ladders for each, and evaluate them in test beams by about 2012. Choosing which to use in ILC vertex detectors would of course be for the then-developing collaborations in conjunction with the peer review process. Given the plan to have two large detectors, there would be room for two technologies to be chosen. However, it was argued plausibly during the review that one might choose a different technology for Layer 1, given the much higher background at small radius, ameliorated by the possibility of more aggressive cooling and cabling than for the outer layers. So there might be as many as four technologies finding a home in ILC. Furthermore, as explained in the next section, there may be a home for yet another pixel technology for the outer tracking system.

Given the events of Black December (2007) in the UK and USA, it is clear that not all these technologies are likely to have full ladders in test beams on the required timescale, but there are at least two escape routes for the groups concerned. One is to rely on time as contingency. The ILC approval may be delayed as a knock-on from the timescale for first results from the LHC, or for other reasons. Even if ILC is approved promptly, some detector technologies may elect to be considered for future upgrades, giving them the opportunity to continue development beyond 2012. Others may ease the burden of producing large prototypes by being incorporated into real detectors in the near-term future, such as MIMOSA for the STAR experiment at RHIC, DEPFETs for SuperBelle, and detectors for IXO (the International X-ray Observatory, descendent of XEUS), or for 3rd or 4th generation SR light sources. Given the strength of interest in advanced pixel detectors for many areas of science, one can be confident that on the timescale for which technology choices need to be made for ILC vertex

detectors, a great deal more will be known about the relative merits of these options than is currently available.

3. ILC Silicon Pixel Tracker (SPT)

So far, pixel detectors in HEP experiments have been restricted to vertex detectors, where the area coverage has been relatively small. In this environment, the advantages of unambiguous space points on tracks, intrinsic to pixel detectors, and their unparalleled performance in areas of high track density such as the core of jets, is universally recognised. Moving out in radius, given the need to minimise material, and the concerns previously mentioned as to whether more conventional tracking technologies will be able to satisfy these requirements, it is worth considering whether an all-pixel tracker is a realistic option. It appears to be so. Firstly, as regards layer thickness, the same approaches as for vertex detectors, for example ladders made with a silicon carbide foam substrate to which thin (~50 μm) monolithic pixel detectors are adhesive bonded, appears to permit large scale ladders of thickness <1% X_0, with adequate stiffness. However, this of course needs to be verified by detailed simulations and the construction of large prototypes. 5 layers, given a unique space point in every layer, will more than suffice to provide standalone track finding. Having independent track finding in the tracker and in the vertex detector is extremely desirable, partly to compare one with the other when reaching for the last percent or so in efficiency, partly for redundancy in case of failure of one or more ladders, and partly to allow for tracks from long-lived parents which are born beyond the vertex detector.

50 μm pixels with binary readout will be sufficient, and to push for better precision than 50/sqrt(12) = 15 μm would be unrealistic, given the systematic uncertainties in the geometrical stability of a lightweight barrel structure of the dimensions needed (up to 2.5 m diameter and 3.4 m length). The most obvious obstacle to realising such a tracker is the pixel count (~40 Gpixels, in contrast to 0.31 Gpixels for the SLD vertex detector, and ~1 Gpixels envisaged for the ILC vertex detector. However, given the trends in focal plane sizes for astronomy [3], such a system will be the norm by about 2020. Manufacturers of imaging chips for the scientific market are already gearing up for such large-scale production.

The second obstacle is how to design devices with 50 μm pixels that will be fully efficient for MIP detection. Due to considerations of power dissipation, yield, data volume, etc, one really would like to avoid being pushed to smaller pixels just in order to be efficient. Such large pixels have been developed with high efficiency for CCDs, which provides one possible

technology option. CCDs are relatively sensitive to damage by ionizing radiation, but at the tracker radii, conventional large area CCDs would be a safe option under normal running conditions. However, in the event of any kind of accident with the machine, it would be possible to irreparably damage such a detector with radiation levels well below the tolerable limit for a MAPS detector. Given the cost and schedule implications of serious damage to the tracking system, this poses an unacceptable risk. Instead, we suggest a study of a large-pixel MAPS system.

A simple option that looks promising is sketched in Fig 1. Each pixel comprises a large area photogate, subdivided into rings with a potential step between them, so that signal collected in one ring will make its way by a combination of drift and diffusion, to smaller and smaller radii, till it is collected on the transfer gate. This 'funnel' was suggested to us by Greg Deptuch of Fermilab, but in the meantime we learned that e2V have already made such a structure for confocal microscopy, where it works well. Within the transfer gate, we envisage a very small sense node (reverse biased diode) with reset transistor, sensing transistor and row-select transistor, for a conventional rolling shutter readout between bunch trains.

Preliminary back-of-envelope calculations [4] suggest that such a detector would have extremely low power dissipation, and the hit densities, integrating background through the bunch train, would be acceptable everywhere except for the very forward disks at small radii, a small fraction of the overall area coverage. However, it could be that detailed track reconstruction studies will establish that some time slicing during the train is needed. If so, the approach sketched in Fig 2 can be considered. In stead of transferring from the transfer gate to the output node, the signal charge is preserved in the buried channel of the sensor, and transferred into the serial register, just as in the ISIS option for the vertex detector. The example shows 10 time slices, but this could be adjusted according to need. Of course, as in the vertexing ISIS, the elements of the funnel would need to stop short of this register, and the region of silicon below the register would need to be provided with a deep p+ implant, to shield the register from direct collection of signal charge. The signal charge from particles traversing this region would be efficiently collected into the funnel by a combination of drift and diffusion, slightly less direct than from the rest of the pixel. No problems of reduced detection efficiency are expected.

For an N-element register, the associated time sliced images imply reading the detector N times during the 200 ms inter-train period, but this is still a very leisurely readout situation, with very acceptable power dissipation for a gas-cooled tracker.

4. Conclusions

All the technical requirements for ILC may be achievable in the time available, but it is difficult to obtain sustained R&D funding for such distant goals. Meanwhile, there are closer targets needing similar performance. Users of 3rd generation SR systems frequently resort to aluminium blocks to reduce intensity due to rate limitations in their detectors. Faster detectors would allow higher throughput of samples on over-subscribed beamlines. 4th generation systems (SSRL, FLASH and the European XFEL) will be even more dependent on such advances. Also X-ray astronomy (XEUS and the U.S. equivalent, now being combined into IXO - International X-ray Observatory) offers contrasting challenges. For these reasons, it may be advantageous for the detector groups to broaden their scientific goals, giving them a range of targets, graded in terms of completion dates and degree of difficulty. Far from diluting the ILC R&D programme, this strategy can strengthen it by allowing it to build on the shoulders of the more modest instruments to be developed for near term projects.

For this approach to work, it seems desirable to enhance the network between groups engaged in R&D for advanced pixel detectors, particularly in the related areas of particle detection (HEP, nuclear physics, electron microscopy) and X-ray detection (for medical, biological, SR and astronomy). To this end, discussions in this workshop led to the suggestion of an international network for R&D in pixel detectors, for which a Coordination Board is now being formed by the directorates of CERN, Fermilab and KEK. There is every indication that this networking activity can be made to work to the advantage of all participants, and it has been warmly welcome d by nearly all the R&D groups.

References

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