

CMOS pixel vertex detector for STAR

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We present development and prototyping efforts directed towards construction of a new vertex detector for the STAR experiment at the Relativistic Heavy Ion Collider (RHIC) accelerator at BNL. The new detector system will extend the physics range of STAR by providing capability for precision measurements of yields and spectra of particles containing heavy quarks. The most precise and central part of the new detector system is a high resolution pixel-type detector (PIXEL) based on the Monolithic Active Pixel Sensor (MAPS) technology. We describe basic PIXEL requirements and selected progress on sensor prototypes dedicated to the PIXEL detector and the detector readout system architecture that has been validated in recent tests of hardware prototypes.

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1. Introduction

The STAR Heavy Flavor Tracker (HFT) upgrade is a new tracking system that will allow for very high resolution vertex measurements. This upgrade is designed to enable the direct topological reconstruction of D and B mesons through the identification of decay vertices displaced from the primary interaction vertex by more than 60 micrometers [1].

The HFT upgrade is intended to consist of three sub-detectors. These sub-detectors are arranged as concentric cylinders to provide full angular coverage. The two outer layers are based on double-sided and single-sided silicon strip detectors and are located at 23 and 14 cm from the center of the beam pipe, respectively [2,3]. The inner-most and the highest precision subsystem of the HFT tracker, referred to as PIXEL, will consist of two layers of Monolithic Active Pixel Sensors (MAPS) at 2.5 and 8 cm average radii. The HFT will significantly enhance the pointing resolution of the Time Projection Chamber (TPC), which is the main STAR detector. Precise vertex reconstruction in high track density events in Au-Au collisions will be possible due to graded pointing resolution from the outside detectors inwards. The PIXEL detector will point at track vertices with a 30 μm distance-of-closest-approach (DCA) resolution.

The physics program and operating environment impose multiple design criteria and make the design of the PIXEL detector quite challenging. We will describe some of these challenges and the approach taken to address them in the following sections.

2. Pixel detector characteristics

Achieving the required high pointing resolution performance requires constraining the amount of multiple-Coulomb scattering by limiting the detector's material budget to a design goal of approximately 0.3% radiation length per PIXEL layer in the sensitive region. The sensitive region is defined by the solid angle coverage of other detector systems is ± 1 in pseudo-rapidity (η) with the first active sensor layer at a radius of 2.5 cm from the beam axis and the second layer at 8 cm radius. The currently envisioned final system design is an array of 40 sensor ladders with ten 2 cm \times 2 cm sensors per ladder and sensor pixel arrays of 1024 \times 1152 pixels resulting in the total pixel count of more than 400 million pixels. The described geometry of the detector and the chosen pixel pitch of 18.4 μm result in the pointing resolution of about $13 \oplus 19$ GeV/p-c μm for perpendicular tracks (p – particle momentum, c – speed of light in a vacuum). It should be noted that the resolution of the detector will be limited by multiple-Coulomb scattering.

To comply with the requirement of low material budget, the PIXEL detector is designed with sensors thinned down to 50 micrometers, carbon fiber mechanical support, aluminum rather than copper conductor readout cables, and cooling system based on air flow. Thinning of silicon devices to a few tens of micrometers is typically available as a standard post-processing technique that has been tested and proven to be reliable [4]. The carbon fiber composite structures used for PIXEL's mechanical support are widely used in vertex detector applications

due to the low mass and high stiffness, combined with a low thermal expansion coefficient. Using aluminum instead of copper for a PIXEL readout cable conductor allows for the reduction of the material budget of a layer by about 0.1% of radiation length. The air cooling system for PIXEL is designed as a closed system, with intake and exhaust located at one end of the detector. This location is compatible with the requirement of quick and precise detector replacement for which the mechanical support is optimized [1]. A conceptual design of the PIXEL detector with its mechanical support structures is presented in Figure 1.

PIXEL will operate in an environment with high track density and is expected to be exposed to radiation that can reach up to 300 krad and 1×10^{13} n_{eq}/cm^2 per year of operation. In this environment, sensors will have to provide detection efficiency above 99 % while operated at 20-30 °C. Short integration time that minimizes both shot noise and pile-up of consecutive events is required. Fast operation of sensors is restricted by the limited power dissipation requirements and necessitates compromises in the sensor design.

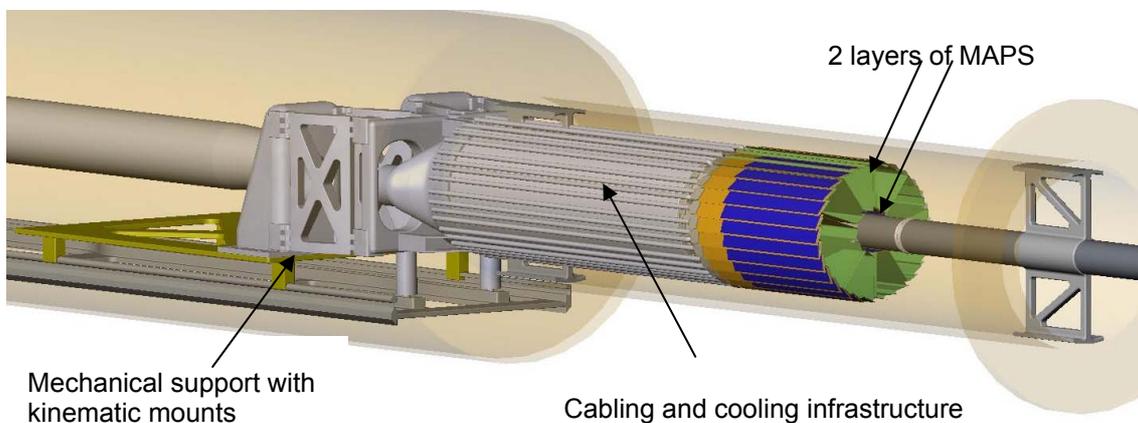


Figure 1 The conceptual design of the PIXEL detector for the Heavy Flavor Tracker. The support structure with kinematic mounts and cabling located in one end of the carbon fiber cone will provide capability for a quick replacement of the detector with a very high accuracy positioning (on the order of $20 \mu m$).

3.Sensor development

The sensor technology chosen for the PIXEL detector is Monolithic Active Pixel Sensors (MAPS). MAPS are constructed using standard commercially available CMOS technology and integrate sensor and readout electronics in one silicon device [5,6]. MAPS operation is based on charge collection from the active volume that is an epitaxial layer typically about 10-15 μm thick. Only a small part of the active volume near the charge collecting n-well/p-epi diode is depleted. The charge generated by ionizing particles is collected from the un-depleted region via thermal diffusion. As the result of the diffusion, the charge spreads over a few adjacent pixels grouped into clusters.

Modern CMOS processes offer small feature sizes that allow MAPS designs with very high granularity. Thin detectors can be obtained by thinning MAPS devices using standard

commercially available thinning techniques applicable in post-processing. High readout speed and on-pixel signal processing offer better performance than in the well established CCDs and, in addition, modern processes inherently offer substantial radiation tolerance. Although, higher readout speeds and radiation tolerance can easily be achieved with Hybrid Pixel Sensors, the overall set of characteristics of MAPS and their achieved performance indicate that this technology is very competitive for charged particle tracking.

The STAR PIXEL detector group is working in collaboration with the CMOS-ILC group at the Institut Pluridisciplinaire Hubert Curien (IPHC) in Strasbourg on the sensor development for the PIXEL detector. The sensor development path follows the development path of the technology as set by the IPHC group, which develops MAPS sensors for various applications.

In this path, the first generation of sensors dedicated to the PIXEL detector was the MimoSTAR series. This generation of sensors featured 50 MHz multiplexed analog readout of parallel sub-arrays processed in a rolling shutter configuration. The prototypes were based on $30\ \mu\text{m} \times 30\ \mu\text{m}$ pixels with a self-biased charge collecting node (a reverse biased charge collecting, n-well/p-epi diode with the operating point defined through a forward biased p+/n-well diode as shown in Figure 2,a) [7]. MimoSTAR2 is a small scale prototype with a 128×128 pixel array. This sensor, tested with minimum ionizing particles and at the integration time of 4 ms, demonstrated the most probable value of signal-to-noise ratio (S/N) of approximately 16 and a mean collected charge of 220 electrons in the central pixel of a cluster. The limited amount of charge collected in a single pixel requires MAPS to exhibit low noise performance at the level of less than 15 electrons. Tests with different prototypes showed that $S/N > 12$ allows for more than 99.5% detection efficiency of minimum ionizing particles with an accidental rate on the order of 10^{-4} - 10^{-5} .

The MimoSTAR2 design has been scaled up to half reticle¹ size and designated MimoSTAR3. The pixel array is 640×320 . The initially low fabrication yield, below 20%, which manifested itself through large number of dead pixels in the middle of the array, was traced back to faulty via connections between different metal layers. This effect was most apparent in the MimoSTAR3 prototype, while smaller prototypes fabricated in the same run preserved high yield even with the same pixel architecture. It was assessed through imaging of selected pixels cross-sections with a transmission electron microscope that vias across the pixel array had the same depth, but metal layers in the center of the array had a slightly larger spacing leading to non-contacting vias between the metal layers. The problem has been attributed to a specific pixel layout where transistors occupy a very small part of the pixel. The pixel layout included a radiation tolerant diode design that eliminated thick oxide from the pixel cell by implementing highly doped active regions [7], and a large surface area of the first metal layer that was used for shielding. These features led to a device layout that is significantly different from standard CMOS devices. This difference most likely affected the manufacturing process and led to an uneven metal layer spacing in the center of the pixel array. The yield issue has been corrected by modifying two production masks. The surface area of the active region in the pixel cell was limited to the vicinity of the charge collecting diode and the surface area of the

¹ A photomask used for lithography in wafer fabrication, typically about $2 \times 2\ \text{cm}^2$ in size.

first metal layer was reduced. In the new fabrication run, the yield was improved to above 80%. MimoSTAR3 is under tests to verify performance and scalability of the design.

The design architecture of the MimoSTAR family limits the integration/readout-time of the final size pixel array to a few milliseconds. To minimize the problem of pile-up of consecutive events at the rate expected for RHIC II luminosities (peak at $8 \times 10^{27} \text{ cm}^{-2}\text{s}^{-1}$) and high particle densities, the detector integration time needs to be reduced to about 200 μs . Parallel outputs that can increase readout speed are limited in number by radiation length and space considerations in the readout cable design. Digital signal transmission from the sensor allows faster readout speeds and will be used in the second generation of sensors dedicated to the PIXEL detector.

The second generation sensor prototype, called Phase-1, will be based on the Mimosas8/Mimosas16 architecture [8], and will contain on-chip correlated double sampling (CDS), fine grained threshold discrimination and fast serial Low-Voltage Differential Signaling (LVDS) outputs. A simplified schematic diagram of a pixel cell is presented in Figure 2, b. The pixel contains a charge collecting node, a simple amplifier, a clamped capacitor for performing CDS and a source follower transistor with a row switch for readout. Each column of pixels ends with a common discriminator located at the edge of the pixel array. The prototype features a 640×640 pixel array of 30 μm square pixels, resulting in a full 2 cm \times 2 cm sensor size. In order to achieve a 640 μs integration time, the sensor will be equipped with four LVDS outputs operated at 160 MHz. This sensor has been designed and recently sent for fabrication. Delivery of wafers of this sensor is expected in the first weeks of 2009. This prototype is intended to be used for construction of an engineering prototype detector with limited coverage that is planned to be deployed at STAR and will allow testing of all mechanical and electronics components needed for the final detector.

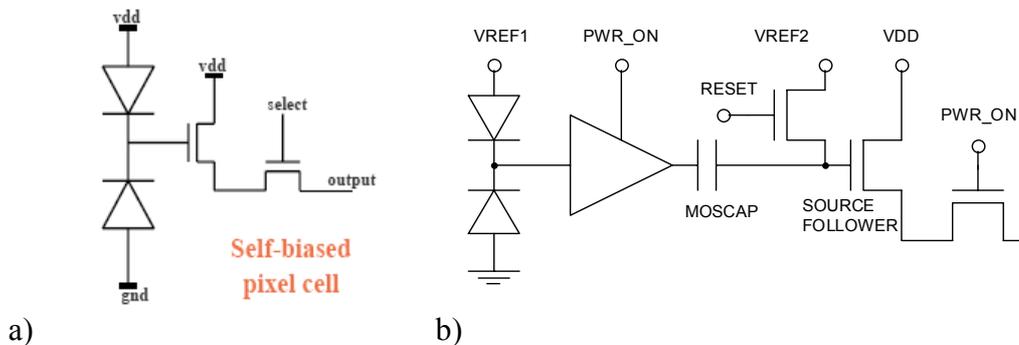


Figure 2 Pixel structures of prototypes dedicated to the PIXEL detector in the MimoSTAR family, (a), and in the second generation of prototypes based on Mimosas8/16, (b).

The final production sensor for the PIXEL detector to be installed in 2011 will feature all of the attributes of the previous prototype plus an on-chip zero suppression circuitry. The on-chip integrated zero suppression circuitry with run-length encoding [9] will reduce data rates and, therefore, it will allow shortening the integration time to approximately 200 μs . It will also allow limiting the number of parallel outputs to two. The pixel pitch for this prototype has been decreased from 30 μm to 18.4 μm to improve radiation tolerance as discussed in [10]. The first prototype of this production design is expected to be available in the 2010 time frame.

4. Readout system development

The PIXEL detector is an upgrade for the STAR experiment and requires the readout system to easily integrate into the STAR environment. The system has to be compatible with the existing trigger and data acquisition system infrastructure. It is also required that the new readout system delivers full detector events for event building at a rate equal to, or greater than, the STAR central detector TPC (a few hundreds of MB/s). This requires that for a 400 million pixel final detector it is necessary to implement data reduction either on-chip or in the readout system. The architecture chosen for the readout system for the PIXEL detector is highly parallel and coupled to the modular structure of the detector, which is based on sensors arranged in ladders.

Development of the readout system for PIXEL is strongly coupled to the sensor development. As more of the functionality is integrated on-chip (in-pixel CDS, binary discrimination), the readout system becomes less complex. The initial development of the PIXEL readout system was optimized for sensors with analog readout. A prototype system was operated with three MimoSTAR2 prototypes read out in parallel. The system featured fast ADCs and a data processing chain implemented in a Field Programmable Gate Array (FPGA) that included: CDS, cluster finding, pixel address encoding, and event building in response to a trigger signal. This early prototype system was successfully operated in the STAR environment as a subsystem of the STAR experiment [11].

For the Phase-1 prototype with binary readout of all pixels, the readout system (RDO) needs to provide zero suppression with address encoding and event forming in response to triggers received from STAR. This will reduce the data flow from approximately 32 GB/s to 240 MB/s assuming a full detector. For the final sensor, zero suppression and address encoding will be implemented on chip, further reducing the complexity of the RDO system.

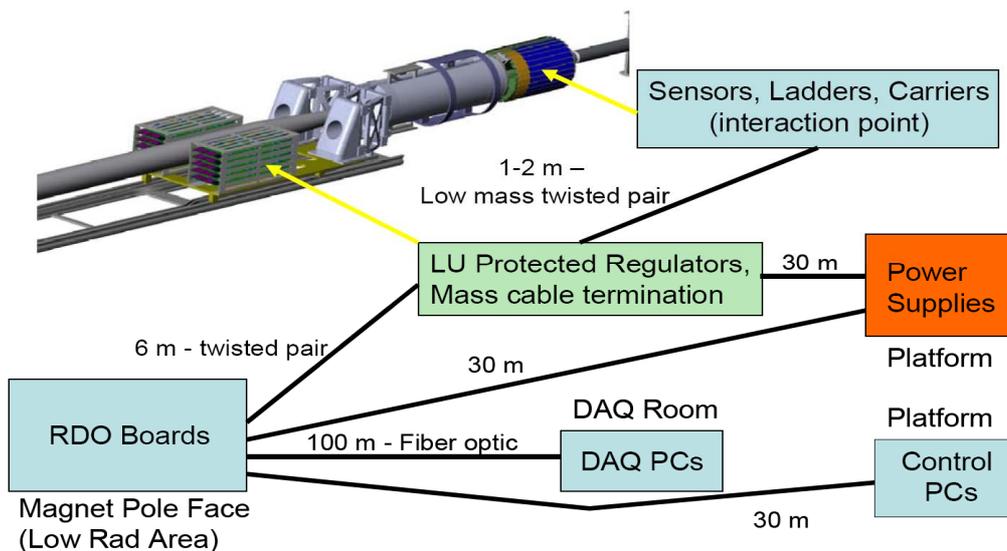


Figure 3 Physical layout of the readout system blocks. There are ten parallel readout chain units in the full system each serving modules of 4 ladders.

The current RDO architecture, designed as 10 parallel and independent RDO chains, is adapted to the Phase-1 prototype and the final sensor. The physical layout of a single RDO chain can be divided into four components: four ladders mounted on a mechanical carrier unit, mass termination board, RDO board, and DAQ PC. Each ladder provides LVDS buffering for output, control, monitoring and synchronization signals. These signals are carried to the power/mass termination board via low mass twisted pair cables (42 AWG), which due to their low stiffness significantly reduce possible distortions into the mechanical structure. The power/mass termination board provides additional LVDS buffering and regulated power with latch up detecting circuitry independently for each ladder. The signals are then transmitted to the RDO boards via robust shielded twisted pair cables (24 AWG). The RDO boards will be located outside of the STAR magnet structure approximately 6 meters away and out of the high radiation environment. A schematic description of the physical layout of the readout system is presented in Figure 3.

The RDO boards are based on a commercially available Xilinx Virtex-5 FPGA development board, mated to a custom motherboard. The latter provides LVDS buffering into the FPGA, the STAR trigger input, and interface for mounting the CERN developed fiber optic Detector Data Link (DDL) [12]. The DDL provides a link between the readout system and data acquisition PCs.

The reliability of the LVDS path has been recently validated with a prototype readout system. Instead of sensors with binary readout, which were not available at the time of tests, LVDS 1-to-4 fan-out buffers were mounted on a mockup ladder built on FR4 PCB (0.031" thick) and sized and routed to resemble the final ladder design. The data path included 1 or 2.3 m fine twisted pair cables and 6 m of a robust twisted pair cable. The data transmission path was calibrated with test signals and the latching time for each LVDS input was adjusted individually in the FPGA using the IODELAY property [13].

Three independent pseudo-random test patterns were sent from the FPGA on the RDO board to the ladder and back to check for data corruption and possible cross-talk. The system was tested with different signaling frequencies, including 160 MHz that is the maximum data rate expected in the PIXEL readout system. The measured bit error rate (BER) at 160 MHz was below 10^{-14} , which fully validates the chosen approach to the system architecture.

5. Status and future development plans

The second generation of sensors developed for the PIXEL detector provides binary readout due to on-chip signal extraction through CDS and binary discrimination. Tests of non-irradiated prototypes indicate good S/N and detection efficiency close to 100%. Initial results of MAPS prototypes tested against ionising and non-ionising radiation are encouraging, but a more detailed study of degradation of the detection efficiency with the accumulated radiation dose as expected in the STAR environment is needed.

The need for building large size prototypes has been emphasised by the yield issues encountered when scaling MimoSTAR2 to MimoSTAR3. It resulted most likely from specific layout characteristics of pixel devices that are significantly different from typical CMOS circuitry. However, it can be expected that PIXEL sensors with digital readout will not be

affected by the same issue due to their more complex pixel layout. The latter includes multiple transistors, which occupy up to 80% of the pixel surface area.

Next milestone for the PIXEL sensor development consists of testing full-reticule size Phase-1 sensors with binary readout, and of using them for construction and testing of the detector engineering prototype. This prototype is intended as 3/10 of the complete detector and will be a test bench for mechanics, electronics, and sensor design prototypes.

The readout system for the PIXEL detector has been recently validated with LVDS readout tests and full readout system production prototypes are being developed.

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