# MIT Haystack / NRAO 4Gbps Status

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In this paper a more detailed explanation on the status of the 4 Gbps data acquisition system and recorder, a joint effort between MIT Haystack Observatory and National Radio Astronomy Observatory (NRAO), is presented. For both NRAO and MIT Haystack Observatory this work is an essential to upcoming scientific experiments where increasing the sensitivity of the instrumentation is critical.

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[1]  Speaker

## 1.Introduction

In this paper we will provide more details on the information presented in the VLBA sensitivity upgrade paper [1] with respect to two specific areas, a new digital backend and the next generation Mark5 system, the Mark5C, that are being jointly developed by NRAO and MIT Haystack Observatory.

### 1.1 RDBE

The second generation DBE uses as its base the Casper *Reconfigurable Open Architecture Computing Hardware* (ROACH) design [2] and is a common hardware platform between both NRAO and Haystack. The major difference between the two systems is only the FPGA binary personality loaded during operations. The ROACH design contains as its centerpiece a single Xilink Virtex 5 FPGA. A seperate PowerPC processor (PPC) runs Linux, e.g. Debian Etch, and is used to control the board. Four CX4 connectors provide a potential 40Gbps bandwidth for connecting them to 10G Ethernet capable device.

In previous presentations and literature, NRAO referred to their systems as the V-DBE and MIT Haystack Observatory as the DBEv2. To avoid further confusion, since both systems use the same hardware platform, both NRAO and Haystack will now refer to the system as the *Roach Digital Backend* (**RDBE**).

As mentioned above, the main difference in the two uses of the RDBE is the FPGA personality developed for operations. MIT Haystack is developing a *Poly Phase Filter Bank* (PFB) personality and the NRAO personality is a baseband convertor (BBC), to replace the existing VLBA equipment for their upgrade.

The Haystack PFB initial design will output a 2Gbps Mark5B emulation mode formatted packet over a UDP/IP data stream with a 32 bit sequence number outside of the VLBI Payload. This design effort serves two purposes. The first is to validate the development efforts in a comparison with Haystacks first generation DBE1, that utilizes the CASPER IBOB reference board and uses a VSI-H output, and the second is to verify the new data communication stack that utilizes a 10G Ethernet interface. The schedule for first light is in the August/September 2009 timeframe.

Follow up efforts will add the VLBI data interface format (VDIF) [3] packet format and enhancements to the capabilities of the FPGA to support both Astronomy and Geodesy.

The command and control application for the RDBE for both NRAO and Haystack will be through a single application that initially supports the standard VSI-S data format. Future versions of the application will include an interface to support remote procedure calls (RPC) over the ssh protocol in support of remote operations [4].

### 1.2 Mark5C

The development of next-generation Mark 5 system, the Mark 5C, will have the capability of recording sustained data rates up to 4096 Mbps via a 10 Gigabit Ethernet daughter card attached to the Conduant Corporation Streamstor Amazon Controller card [5]. The Mark5C

will use the same disk modules as the Mark 5A and Mark 5B, thus preserving existing investments in disk modules.

The data interface for both recording and playback will be 10 Gigabit Ethernet, which is rapidly becoming a widely supported standard. The initial release of the Mark5C will support only the record function over its 10G daughter card. The use of 10GigE interfaces comes with some significant implications, however, the requirements on the data sources to output data streams in a format compatible with the Mark 5C specification [6], e.g. the RDBE. Secondly, data playback through a 10GigE interface is a good match for a rising generation of software correlators. In the interests of backwards compatibility, the Mark 5C will support a mode that writes disk modules in Mark 5B data format that existing Mark 4 correlators can correlate.

The testing and verification of the functionality of the Mark5C, Mark5 memo 076[7], is under way at Haystack. The present version of Mark5C under test has a minimum feature set that supports the ability to record only. The main test of this feature set is that the Mark5C can sustain between 32Mbps and 4Gbps sustained data in Mark5B data format. As new features become available, the testing will continue and regression tests of existing features performed.

The initial release of the command and control application for the Mark5C is July 2009. This application will support write capabilities at 2Gbps using the Mark5B compatibility mode and writing to the Mark5 in bank mode. Bank mode means writing the incoming data stream to a single Mark5 disk module. The official version 1.0, expected later in the year, will support full 4Gbps recording in non-bank mode, meaning writing data to both disk banks simultaneously, and support both the VDIF data format and the Mark5B emulation modes.

## References

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