PROCEEDINGS OF SCIENCE

An ultra fast silicon pixel detector for the NA62 experiment: the Gigatracker

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The beam spectrometer of the NA62 experiment has to sustain high and non-uniform beam rate ($\sim$1.5 MHz/mm^2 in the hot center and 0.8-1.0 GHz in total, hence the name Gigatracker) and should preserve beam divergence and limit beam hadronic interactions. The Gigatracker has to provide precise momentum, time and angular measurements on every single track of the secondary 75 GeV/c hadron beam with a timing precision of 150 ps (rms). To meet these requirements, three hybrid silicon pixel detector stations will be installed in vacuum. An adequate strategy to compensate the discriminator time-walk must be implemented and R&D investigating two different options is ongoing. Two prototypes have been designed in order to have an experimental comparison of the performances: one approach is based on the use of a constant-fraction discriminator followed by an on-pixel TDC, while the other one is based on the use of a Time-over-Threshold circuit followed by a TDC shared by a group of pixels.

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1. Introduction

The NA62 experiment aims to collect $\mathscr{O}(100)$ events of the ultra rare decay $K^+ \to \pi^+ \nu\overline{\nu}$ with 10% background in about two years of data taking at the CERN SPS [1]. The branching ratio of this decay is predicted with high accuracy in the Standard Model: a recent calculation yields $(8.5 \pm 0.7) \times 10^{-11}$, where the uncertainty is dominated by the CKM elements, as reported in [2] and references therein.

In order to keep background under control, NA62 will use highly efficient photon vetoes and particle identification detectors, together with kinematical selections based on the missing mass variable:

$$m^2_{miss} \simeq m^2_K \cdot (1 - \frac{|p_\pi|}{|p_K|}) + m^2_\pi \cdot (1 - \frac{|p_K|}{|p_\pi|}) - |p_K| \cdot |p_\pi| \cdot \theta^2_{\pi K} \tag{1.1}$$

where p_K (p_π) and m_K (m_π) are the kaon (pion) momentum and mass, respectively, and $\theta_{\pi K}$ is the angle between the two tracks.

2. The Gigatracker detector

The beam spectrometer is composed of three hybrid silicon pixel detector stations installed in vacuum (Fig. 1), which will measure the positively charged 75 GeV/c beam particles by means of 300 μm $\times$ 300 μm pixels. The pixel size and the beamline geometry yield to a resolution on the momentum measurement of $\sigma(p_K)/p_K \sim 0.2\%$ and of $\sim$16 μrad on the angles of the kaon track entering the decay region.

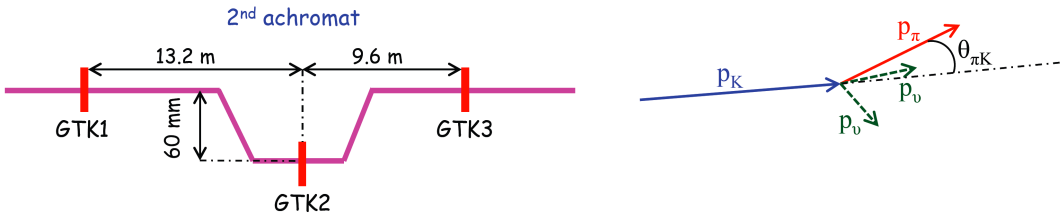

Figure 1: Schematic representation of the GigaTracKer (GTK) system. Deflection of the particles' trajectory due to four dipole magnets, which compose a so-called achromat, is indicated on the left. Kinematic variables characterizing the decay are shown on the right.

The Gigatracker (GTK) system should preserve beam divergence and limit hadronic interactions in the detector and surrounding materials, hence the material budget will be kept to a minimum ($\sim 0.5\%\ X_0$ per station) and the GTK stations will be installed in vacuum. The crucial parameter of this detector is the time resolution of 150 ps (rms) for a single track, which is an unusual requirement for a traditional pixel detector and will allow to associate the daughter particle track to the correct parent kaon.

3. Operation parameters

The dimensions of the NA62 beam at the GTK positions will be of 60 mm $\times$ 27 mm and the particle flux will reach up to 1.5 MHz/mm^2 in the central part. The beam region will be completely covered by a single, fully-active silicon sensor which consists of a 90 $\times$ 200 pixel matrix. The sensor will be flip-chip bonded to ten Read-Out Chips (ROCs), as shown in Fig. 2, each containing a matrix of 45 $\times$ 40 pixels and wire-bonding pads on one of the short edges.

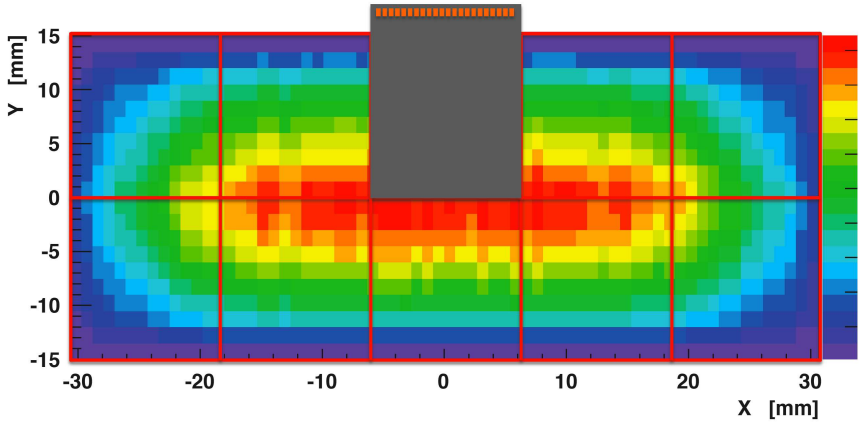

Figure 2: Simulated beam intensity distribution over one GTK station. A schematic of one of the ten ROCs, which will completely cover the sensor area after flip-chip bonding, is shown.

Sensor thickness has been fixed to 200 μm due to material budget constraints: a thinner sensor would reduce the material but would not be compatible with the signal-to-noise ratio required for time resolution. High resistivity sensor wafers (p-in-n) will be processed at FBK-irst (Italy) during summer 2009.

Electrical connections between the silicon sensor and the ROCs will be achieved using the flip-chip bonding technique. The prototyping phase will be different with respect to the production of final assemblies as prototype ROCs will only be available as single dies from a Multi Project Wafer (MPW) run. Therefore special processing and handling tools must be developed for successful bonding during this phase. The production of final assemblies that will be installed for data taking will be done using ROCs available on full size 200 mm wafers. In addition, the target thickness of the final read-out wafers is equal or less than 100 μm in view of the severe material budget requirements.

The expected fluence for 100 days running (a typical run year) is estimated to be $\sim 2 \times 10^{14}$ 1 MeV n equivalent cm^{-2} in the central region of the sensor. This value is comparable to those expected for the LHC trackers over ten years of operation. In order to understand the working point of the detector, irradiations of diodes with fast neutrons and protons have been carried out, in addition to annealing measurements (I-V and C-V) following the expected run scenario. Results show that the most critical parameter in operating the GTK is the radiation induced leakage current on the relatively large sensor, which can be limited by low temperature operation. Currently it is foreseen to operate the detector at a temperature lower than 5 °C. In addition, the estimated power

dissipation of the read-out chips is $\sim$2 W/cm^2. The very low mass of the detector, the necessary operation in vacuum and the need of limiting leakage current increase due to radiation damage demands a very efficient and reliable cooling system.

Different cooling options are currently under study. The first configuration is based on a thin support/heatsink of very high thermal conductivity carbon fiber, coupled to a cooling system surrounding the rectangular beam active area. Micro channel cooling in silicon substrates is being investigated as well. In another option the flip-chip bonded assembly will be installed inside a vessel with thin cylindrical kapton walls (less than 100 μm) where nitrogen is circulated: this solution should provide a quite uniform temperature distribution across sensor area. Thermal modeling, calculations and construction of prototype cooling system are under way.

4. Read-out architectures

The pixel ASICs have a highly complex functionality in order to provide the required time resolution of $\sim$150 ps (rms) per single track. A commercial 0.13 μm CMOS technology has been chosen, with radiation hardening design, in view of its long term availability, high component density, high speed and low power consumption.

Each readout pixel ASIC, in the final version, will comprise arrays of 1800 pixels, for a total of 18k pixels for a single GTK station. The total average data rate per chip is expected to be $\sim$4 Gb/s or more and therefore, due to this huge data transfer rate, high speed serial links will be adopted together with a trigger-less read-out solution, which will reduce the amount of data to be stored inside the chip itself. In addition, the ROCs should achieve an efficiency of 99% or better.

The two main issues that have to be addressed in order to achieve the required time resolution are compensation of the discriminator time-walk and time measurement with such a high channel density. Two small area prototypes, based on different concepts, have been designed to achieve the required performances [3, 4, 5].

4.1 On-pixel TDC option

In this architecture, the time-walk problem is addressed via a Constant Fraction Discriminator (CFD) technique. The discriminated signal is then used to store the value of a time-stamp bus, which is distributed to all the pixels, thus obtaining a coarse time measurement. In parallel, a Time-to-Amplitude Converter (TAC) followed by a Wilkinson ADC is used to measure the timing distance between the comparator output and the next clock rising edge. All these operations are performed inside the single pixel cell (Fig. 3).

This approach requires only one measurement per hit, while it poses challenges on the comparator design. The TAC-based TDC solution requires more digital circuitry on the pixel area, thus potentially creating noise problems. In addition, the pixel area will receive a high radiation dose and has to be designed in order to be radiation tolerant in both total dose and SEU aspects.

4.2 End-of-column TDC option

This option makes use of the Time-over-Threshold (ToT) technique to correct for the discriminator time-walk. Each pixel cell drives a dedicated transmission line to send the digitized

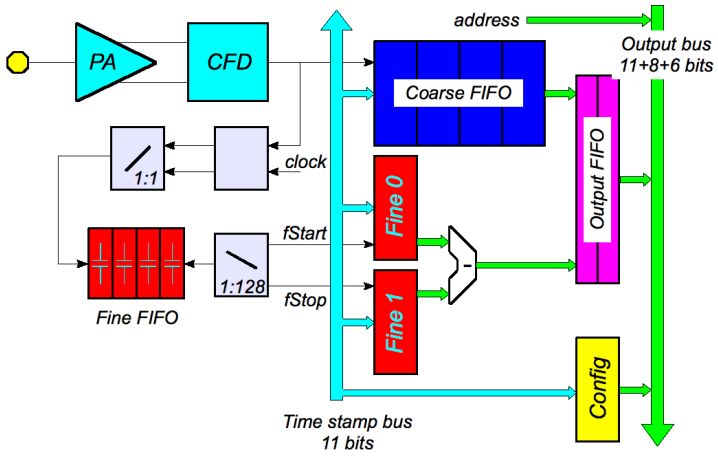

Figure 3: Schematic pixel cell diagram for the “on-pixel TDC" option.

discriminated signals to the End-of-Column (EoC). Special techniques have been adopted to maintain the timing precision of this signal: each pixel output line is realized as a transmission line, driven in current mode, and pre-emphasis is implemented in the line driver in order to circumvent the problem of line resistance. The issue of precise time measurement with high read-out channel density is dealt with a bank of DLL-based TDCs, which receive signals from several pixels (Fig. 4).

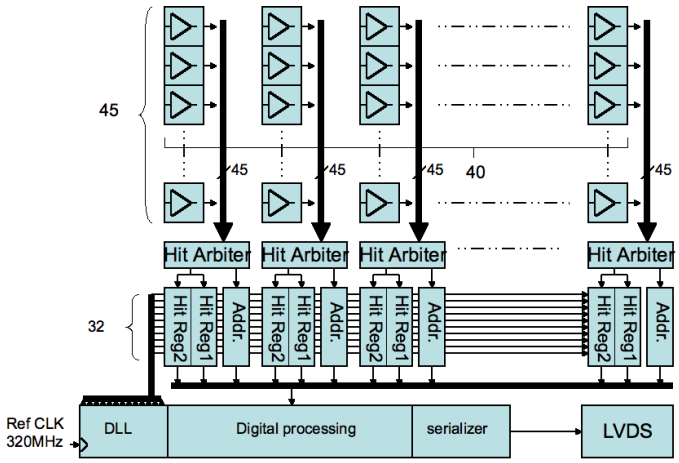

Figure 4: Schematic diagram of the “end-of-column TDC" architecture.

The DLL-based TDC has to be much faster (with respect to the other option) in order to keep dead-time under control, because a single TDC is shared among different pixels. Ambiguities can arise if two pixels which belong to the same TDC are hit close-in-time. Moreover, the TDC bank has to be placed at the EoC and therefore signals carrying the time information have to be transmitted over a well calibrated transmission line in order not to degrade timing information.

Summary

The main features of this detector are the excellent time resolution per single track ($\sim$ 150 ps rms) and the very low material budget. Two prototype read-out ASICs have been developed which integrate TDC circuitry inside each pixel cell or at the end of a pixels' column. Preliminary investigations did not give a clear advantage of one solution over the other, therefore two small area prototypes have been designed in order to have an experimental comparison of the performances. The two prototype chips have been produced in a commercial 0.13 μm CMOS technology and are currently being tested.

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