PROCEEDINGS OF SCIENCE

The Fast Tracker Architecture for the LHC baseline luminosity

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Hadron collider experiments search for extremely rare processes hidden in much higher background levels. Only a tiny fraction of the produced collisions can be stored on tape and an enormous real-time data reduction is needed. This requires massive computing power to minimize the on-line execution time of complex algorithms. A multi-level trigger is an effective solution for an otherwise impossible problem. The Fast Tracker (FTK) [1, 2] has been proposed for high quality track finding at very high rates (Level-1 output rates) for the ATLAS experiment. FTK will use FPGA and ASIC devices in order to complement CPUs. FTK beats the combinatorial challenge with special associative memories, where parallelism is exploited to the maximum level. The associative memories compare the track detector hits to all pre-calculated track patterns at once. The system design is defined and proposed for high-luminosity studies including low-P_T B-physics and high-P_T signatures for Level-2 selections: b-jets, tau-jets, and isolated light leptons. We test FTK algorithms using ATLAS full simulation with WH and Hqq events at $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The reconstruction quality is evaluated comparing FTK results with the tracking capability of an offline tracking algorithm. We show that similar resolutions and efficiencies are reached by FTK. The online use of the whole silicon tracker is necessary to obtain the low fake rate typical of the offline.

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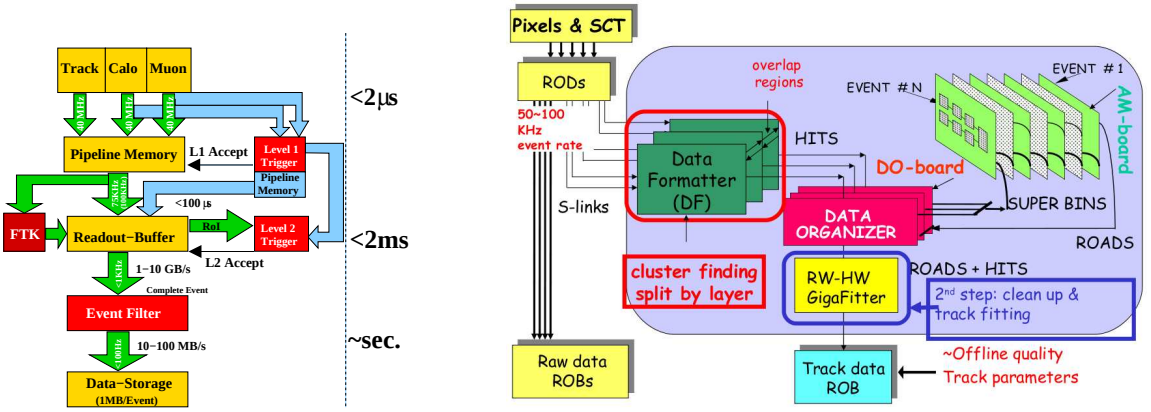


(a) (b)

Figure 1: The left figure shows how the FTK processor is integrated with the ATLAS DAQ system. The scheme on the right shows the connection between the internal elements of the processor.

1. Introduction

The FTK processor[1, 2] is dedicated hardware for on-line tracking. The idea is derived from the successful SVT[3] processor, in use at the CDF experiment. The processor can reconstruct tracks with a momentum above 1 GeV/c, with full coverage in pseudo-rapidity $|\eta| < 2.5$. The track list for an entire event is built for use by the High-Level Trigger [4] (HLT) system.

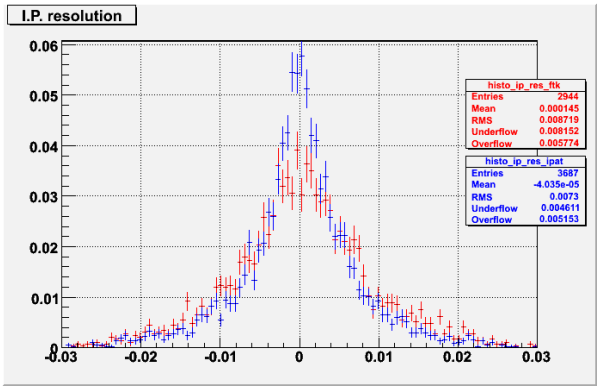
The FTK processor will use the data coming from the 3 pixel layers and the 8 stereo SCT layers in the ATLAS Inner Detector (ID). The data coming from the SCT are clustered by the DAQ boards; the pixel data instead will be clustered within the FTK system. A 2-D clustering algorithm [5] can be implemented using FPGA processors within the FTK processor.

In order to better exploit the parallelism of the algorithm, and to increase the overall input bandwidth to FTK, the ID readout is divided in ϕ-slices called "regions". The number of regions currently used is 8 and each region has a generous overlap with the adjacent ones to avoid inefficiency at the edges. The hardware described next will be replicated for each region. Fig. 1(a) shows the insertion of the FTK processor in the ATLAS DAQ; Fig. 1(b) sketches the internal structure.

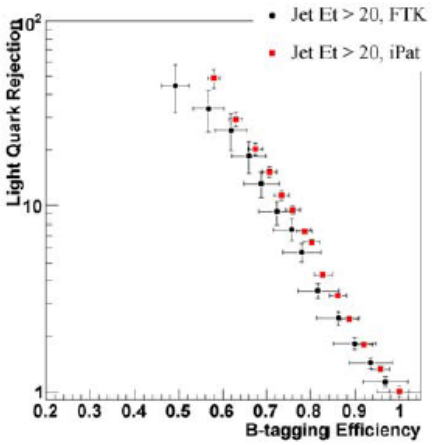
2. Pattern recognition and Track fitting

The pattern recognition employs pre-calculated charged particle trajectories using a coarse silicon detector segmentation: adjacent strips or pixels are merged into Super-Strips (SS) having a size of few millimeters[6]. These low-resolution trajectories, also referred to as "patterns" or "roads", are calculated using the realistic ATLAS Montecarlo simulation, with a suppression of hard scattering and noise effects[6], to avoid the inclusion of very low-probability patterns in the storage bank.

The patterns are stored in Associative Memory (AM) chips [7]. The current technology used at CDF is 180 nm standard cells, containing 2.500 patterns/chip for 12 layer patterns. Different options are under consideration for the new AM chip version. We are currently working on 90 nm



(a)



(b)

Figure 2: The left plot shows the I.P. resolution for WH events at high-luminosity comparing the FTK resolution, in red, with an offline algorithm, in blue. The right plot compares the b-tagging capability obtained using the tracks reconstructed by FTK with Level-2 or offline tracks using the same b-tag algorithm.

R&D to pack 10.000 patterns in a chip, with a possible extra factor of two gain achievable with a custom cell design.

The hits in the 11 SSs belonging to a found road are then converted into sets of 14 full resolution coordinates (each of the 3 pixel layers has two coordinates), providing all possible combinations. For each combination the track parameters are evaluated using 5 scalar products in a linear approximation [6].

In both road finding and track fitting steps the processor finds duplications of the real tracks. To suppress the duplicates the system has two different algorithms: the road-warrior, used to eliminate duplicated roads coming out of the AM, and the hit-warrior, used to suppress duplicated tracks after fitting.

The size of the pattern bank is an important parameter for the system. It establishes the efficiency of the banks, for a fixed SS size. The processor is also able to find and reconstruct tracks with hits in 10 of the 11 layers. This capability increases the efficiency for tracks with a real missing hit and also the overall bank efficiency. With the pattern size[6] used in those studies we obtained an efficiency about 90% for muons with only 8×10^6 patterns in a single region. We also used and compared a 60×10^6 pattern bank. This bank provides a high efficiency even with a limited use of 10/11 matching, but the advantages are negligible compared to the increased cost of the system. The final result of our optimization for pions efficiency is a bank of 25×10^6 patterns for these SS sizes.

3. Preliminary results

The FTK performance was tested first using single muon tracks to verify that the quality of the track parameters is close to those of the offline algorithms. The impact on rare B-hadron decays was already shown [6]; the new studies focus on high-p_T objects.

Fig. 2(a) compares the FTK and the offline impact parameter resolutions for WH events, where the Higgs boson is forced to decay into $b\bar{b}$ or light quarks. This comparison is valid for both samples used (zero and design pile-up). So far, the FTK impact parameter resolution is equal to that of offline with an additional 35 μm added in quadrature. Fig. 2(b) compares light-quark rejection versus b-tagging efficiency for FTK and offline tracks, using the same WH samples without pile-up. The algorithm chosen for this initial study is extremely fast, a simple likelihood ratio using the transverse signed impact-parameter relative to the center of the LHC beam-line. We need a rejection greater than 10 or 20 for a b-tagging efficiency of 50%, which we exceed even with this simple algorithm. We note that FTK will not perform event selection algorithms like b-tagging, but will only provide the tracks to the Level-2 CPU's.

We also studied the efficiency of hadronic τs produced in vector boson fusion events Hqq, with a Higgs mass of $120\,\mathrm{GeV}/c^2$. The results are preliminary and the algorithm is not optimized yet. However we can already conclude that both the efficiency and background rejection of the chosen algorithm[2] are roughly the same when the algorithm runs on offline and FTK tracks. The efficiency is roughly 45% for 1-prong τs and 15% for 3-prong τs at the baseline luminosity. The mistag probability for light quark jets is smaller than 1%.

4. Conclusions

The FTK processor can help the ATLAS HLT trigger algorithms by preparing the list of 3-D tracks in time for Level-2 trigger processing. The track parameters have a quality and an efficiency comparable with offline tracking. The Level-2 processors can request the track information for any region of interest or the entire event and then use all of its available CPU time to run sophisticated algorithms like b tagging, τ identification, and jet reconstruction

The integration with the ATLAS system is done with optical splitters that produce a data stream identical to the usual DAQ. It has already been designed, tested, and passed an ATLAS board review.

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