Readout electronics of 144ch HAPD developed for Belle-II Aerogel RICH system

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For the upgrade of the Belle detector, we are developing a proximity focusing ring imaging Cherenkov detector using a silica aerogel as a radiator (aerogel RICH). A 144-channel HAPD is one of the candidate photo-detectors. Since, a typical gain obtained with the HAPD is about $10^4 \sim 10^5$, which is lower than photo-multiplier's, we need specific electronics to amplify a signal. For this reason, we have been working on ASIC chips for the readout of the HAPD signal. We have measured the performance of new ASIC chips, and have tried to observe the HAPD signal with the ASIC and controlled by the FPGA. From the results, we found the ASIC shows excellent performance to use in the aerogel RICH system, and succeeded to read the HAPD signal with the ASIC and the FPGA.

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1. Introduction

The threshold-type Cherenkov detector with the aerogel radiator (ACC) [1] is used for π/K separation above 1GeV/c in the Belle experiment [2]. However, the ACC does not provide separation for high momentum particles around 4GeV/c in the forward end-cap region. For the Belle-II experiment to upgrade the present detector system, we have been developing a proximity focusing ring imaging Cherenkov counter with an aerogel radiator (aerogel RICH) [3] as a new PID (particle identification) device to improve separation capability in this region. Our target is to provide more than 4σ π/K separation in the kinematical range from 1GeV/c to 4GeV/c.

The requirements to a photo-detector for the aerogel RICH are; (1) sensitive to a single photon, (2) immune to 1.5 T magnetic field, (3) having large effective area, (4) pixelated with resolution 5 $\times$ 5 mm^2, (5) coverage of end-cap region (2×2 m^2, 10^5 channels). As one of the candidates, we have been developing a 144-channel Hybrid Avalanche Photo Detector (HAPD) in a collaboration with Hamamatsu Photonics K. K. (HPK).

2. 144-channel Hybrid Avalanche Photo Detector

Fig1-(a) shows the structure of a 144-channel multi-anode HAPD. Photons enter from the entrance window and generate photo-electrons from the photo-cathode. Photo-electrons are accelerated by a high electric field ($\sim$8kV) inside the vacuum tube, and enter into the avalanche photo diode (APD). In these processes, a total gain of HAPD is from 10^4 to 10^5. In the case of the 144-channel HAPD [4], four APD chips are placed in a 2×2 array. Each APD chip is divided into 36 channels with 4.9×4.9 mm^2 pixel size (Fig1-(b), (c)).
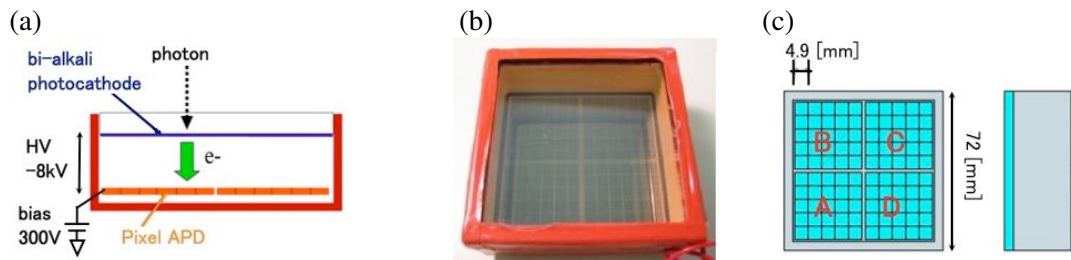

Figure 1: (a)Structure of a 144-channel multi-anode HAPD. (b)Photograph of 144ch HAPD. (c)Schematic drawing of 144ch HAPD.

3. ASIC for readout of 144-channel HAPD

The requirements to the front-end electronics for the 144-channel HAPD in the Belle-II aerogel RICH system are; (1) high gain and low noise amplifier, (2) high density front-end electronics (100k channels), (3) possible to connect to the Belle-II DAQ system. Since only the ASIC (Application Specific Integrated Circuit) can meet these requirements, we have been working on an ASIC for readout of the 144-channel HAPD since 2003. Two types of ASIC chips, refer to as S-series and SA-series, were produced so far.

An S-series chip includes a preamplifier, a shaper and a variable gain amplifier, followed by a comparator for the digitization of analog-signals to on/off hit information, and a shift register for

pipelined readout. The specifications of S-series [4] are as follows; the target noise level is 1200 e^- with an input capacitance of 80pF, which is equivalent with HAPD capacitance. An amplification of the variable gain system is adjustable from 1.25 to 20, and its shaping time can also be selected from 0.3 to 2.0 μs. The threshold voltage is common for all channels (18channel/1chip), but the offset can be adjusted for each channel. Therefore, we can set appropriate threshold level for each channel.
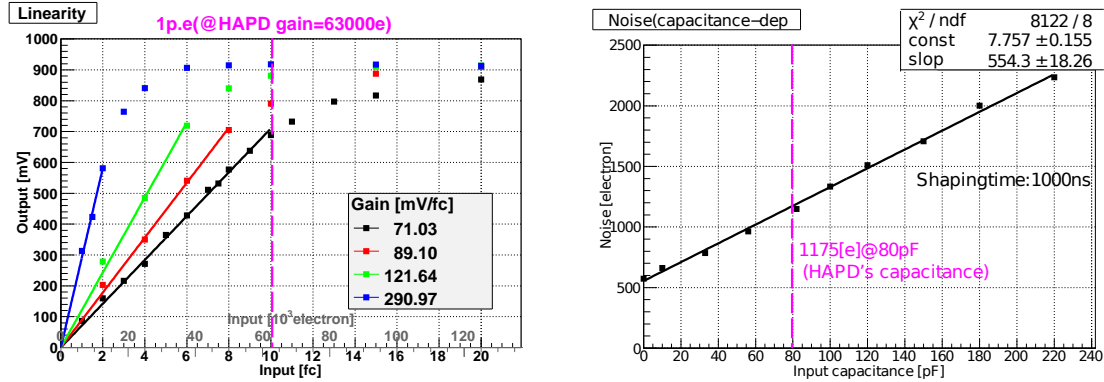
Figure 2: Performance of SA01. Linearity of preamplifier at each setting of 4-step gain (left). Capacitance dependence of noise at setting shaping time to 1000ns (right).
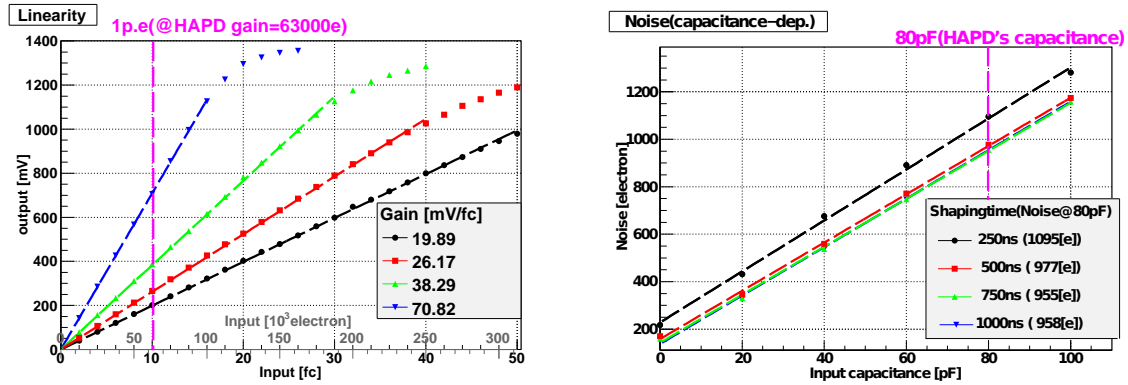

Figure 3: Performance of SA02 (simulation). linearity of preamplifier at each setting of 4-step gain (left). Capacitance dependence of noise at each setting of 4-step shaping time (right).

The SA-series have being developed as the more flexible type based on experiences from S-series. The main change from S-series is that the digital part (shift register) is dropped out to match the Belle-II DAQ scheme, and that only one amplifier is included. Therefore, an SA-series chip consists of a 4-step variable gain preamplifier, a 4-step variable shaping time (250, 500, 750, 1000 PS) shaper, and a comparator. The chip production is done at the MOSIS using TSMC CMOS 0.35 μm process. An SA01 (1st version of SA-series) chip has only 12 channels, and the performance is shown in Fig2. The gain of the preamplifier is about 71, 89, 122, 291 mV/fC, and the noise level is 1175 e^- with 80pF capacitance. This performance is enough to detect single photo-electron. However, output signal from the SA01 is already saturated even at single photo-electron signal of 63000 e^- (i.e., an HAPD gain of 63000). As an upgrade from SA01, we are developing SA02 (the

2nd version of SA-series) whose gain is decreased to 1/4 of the SA01 to avoid saturation at single photo-electron signal. In the SA02, the number of channels is increased to 36. Fig3 shows the SA02 performance in Spice simulation. The SA02 has good dynamic range around single photo-electron signal, where its noise level is less than 1100 e^- at any setting of shaping time. The performance will be examined after the chips are delivered.

4. System test with HAPD, ASIC and FPGA

We plan to use FPGA (Field Programmable gate array) for the digital part removed from SA-series chips. We have a new test board equipped with three ASIC (SA01) chips and one FPGA chip (Fig4-(a)). Since the number of channels in an SA01 is 12, this board can handle 36 channels of HAPD (corresponding to one APD chip of HAPD). We connected this board to HAPD, and checked its performance. Fig4-(b) shows hit counts in a channel for 100 LED clocks when we irradiate a LED light to a single HAPD channel, with varying threshold level of ASIC. We found the distribution clearly separated between pedestal, single photo-electron and two photo-electron peaks. Fig4-(c) shows hit counts for all channels for 100 LED clocks when we vary the irradiation point of LED, and set threshold voltage to 4σ noise level. We can see clear hits except for 5 channels bad due to ASIC or HAPD. These results show successful readout of the HAPD signal using the developed ASIC chip and the FPGA chip.
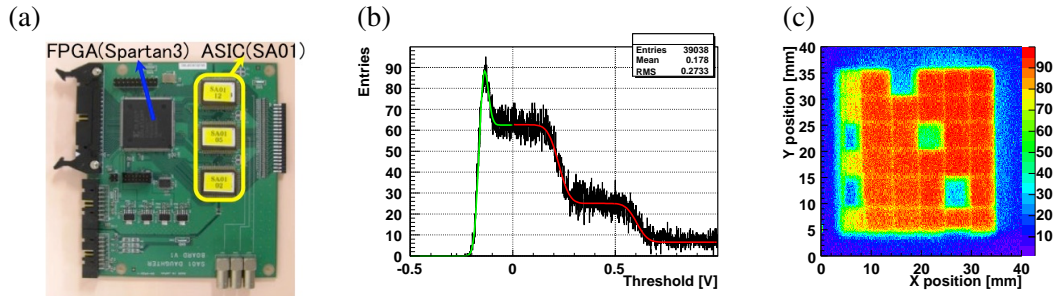
Figure 4: Readout of HAPD with ASIC, FPGA. (a)Photograph of the test board. (b)Result of threshold scan (fit with gaussian (green) and triple error function (red)). (c)Result of 2-dimensional scan.

5. Summary

We have developed the readout electronics for the 144-channel HAPD for the Belle-II aerogel RICH system. The new ASIC chip has sufficient performance to detect single photo-electron signal from HAPD and we have succeed to readout the HAPD signal using the ASIC and the FPGA.

References

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