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CCDs in High Energy Physics

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CCDs have been used as pixel detectors for ionising particles in High Energy Physics since the 1980s. After briefly reviewing the operating principles and historic uses of these devices, I will discuss their advantages and disadvantages with respect to other technologies in future HEP applications, and describe R&D towards their possible application in vertex detectors at a future linear collider.

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1. Introduction

Charge Coupled Devices (CCDs) were invented in 1969 as charge storage registers[1], but their potential as an imaging devices was immediately recognised. The significance of this invention, beginning the development of solid-state imaging devices, was recognised in the award of the 2009 Nobel Prize.

CCDs[2] are normally implemented in silicon as a series of parallel polysilicon electrodes (gates) on top of a p-type epitaxial layer, separated from it by a thin layer of insulating oxide. When different voltages are applied to the gates, free electrons in the epitaxial layer will be gathered and held under whichever electrodes provide a local potential maximum. By changing the voltages (clocking) the stored charge may be moved from one electrode to the next. In a three-phase CCD every third electrode is electrically connected, ensuring that the charge can be moved in the required direction. It is also possible to make a two-phase CCD, where the direction of charge transfer can be set by varying the doping profile under each gate.

If the electrons are allowed to reach the oxide, charge may be lost due to trapping. To avoid this, an n-type implant is added to the epitaxial layer under the oxide, moving the potential maximum a few hundred nanometres below the silicon/oxide interface. This implant can be made in the form of n-channels, creating electrically isolated columns running in the direction perpendicular to the gates. A 2D array of pixels is thus created by the intersection of the n-channel columns with rows defined by the gates.

When a CCD is used as an imaging device, free electrons are created in the epitaxial layer by the absorption of photons (e.g. optical imaging) or the passage of a minimum ionising particle. These electrons gather in the potential maximum of the n-channel under the closest high-biased gate. During readout, the charge is clocked out of the imaging area along each column in parallel. In a conventional CCD, upon reaching the periphery of the device the charge from each column passes into the elements of a serial register, also implemented as a single column CCD. Between each clock cycle of the parallel imaging area, the entire serial register is clocked out to the output node. This scheme requires a single amplifier and readout circuit, but is limited by the speed of the serial clock. For high speed or large area devices, multiple output nodes can be used.

2. Use in High Energy Physics

The first use of CCDs in HEP was by the ACCMOR Collaboration[3][4]. Two sensor planes immediately downstream of a copper target each consisted of a single CCD with an area of approximately 1 cm^2. The low occupancy and high resolution of the 22 μm$\times$22 μm pixel devices proved a powerful tool in identifying the products of charmed hadron decays.

The SLD experiment at SLAC used four layers of CCDs in its vertex detector. The first generation CCD-based detector VXD2[5] consisted of 480 square centimetre-sized CCDs with a total of 120 million pixels, and was replaced in 1995 by VXD3[6] with 96 large active area (80 mm$\times$16 mm) CCDs and a total of about 300 million 20 μm$\times$20 μm pixels. In VXD3 the sensors were thinned to approximately 150 μm and attached to 400 μm thick beryllium substrates, resulting in a material budget of only 0.4% X_0 per layer in the active region.

ACCMOR and SLD demonstrated the successful use of CCDs for precision vertexing. Alternative pixel detector technologies are now available, but CCDs retain some advantages. The imaging area has no active components and functions as a large capacitor, so the power dissipation and cooling needs in the sensitive volume are low. Wafer-scale devices are readily available from industry, and suppliers have the capability to provide thinned sensors: astronomical CCDs, for example, are normally supplied with all of the sub-epitaxial bulk silicon removed to provide the optimum efficiency for back-illuminated operation. These factors allow the design of extremely lightweight detectors. An additional advantage is that the charge storage is almost impervious to electromagnetic pickup or interference.

The limitations of CCDs derive from the same features. Large area devices are very difficult to operate at high frame-rates, as high clock speeds and corresponding large currents become prohibitive. Additionally, transporting charge over large distances results in sensitivity to the density of traps. Exposure to damage-inducing radiation fluxes will increase the trap density, resulting in non-uniform gain and a decrease in the signal-to-noise ratio[7]. This effect can be reduced by maintaining the CCDs at cryogenic temperatures, but this increases operational complexity and the possibility of thermo-mechanical problems.

In comparison to other candidate pixel technologies, the radiation intolerance and relatively low-speed operation rule out the use of CCDs in LHC vertex detectors. They may well be favoured in precision experiments, however, as the requirements for low power and material budgets are combined with lower radiation and interaction rates.

3. CCDs at the ILC

The International Linear Collider (ILC)[8] is a proposed future facility with e^+e^- collisions at $\sqrt{s} = 500 - 1000$ GeV. Its main goal will be the precision study of new physics discovered at the LHC, utilising the relatively clean lepton collider environment. Many of the priority physics channels[9] will require extremely good heavy quark flavour and τ identification, so high-precision, low mass gigapixel vertex detectors with are essential. This will include the requirement that there is no additional material for cooling in the active volume, so the power dissipation will have to be low enough to allow cooling by gas. The target for the total amount of material is 0.1% X_0 per layer, equivalent to about 100 μm of silicon. The radiation environment and interaction rate are sufficiently low that the use of CCDs appears feasible, if challenging.

Although the rate of primary interactions at the ILC will be low, the density of the particle bunches will be such that field-field interactions will produce large numbers of low energy e^+e^- pairs (beamstrahlung). These particles will not reach the outer detector due to the magnetic field, but will follow spiral trajectories at low radii, passing through the vertex detector multiple times. A single bunch train, consisting of 2820 bunches over a period of 0.95 ms, is expected to result in of the order of 200 hits per square millimetre in the innermost detector layer. Two strategies have been proposed to deal with this.

The first strategy is to integrate the charge collection over each bunch train and read out the sensors in the $\sim$ 199 ms gap between trains. This approach will result in easily-achievable readout and clocking requirements, but will present significant challenges in pattern recognition with such high hit densities and occupancies.

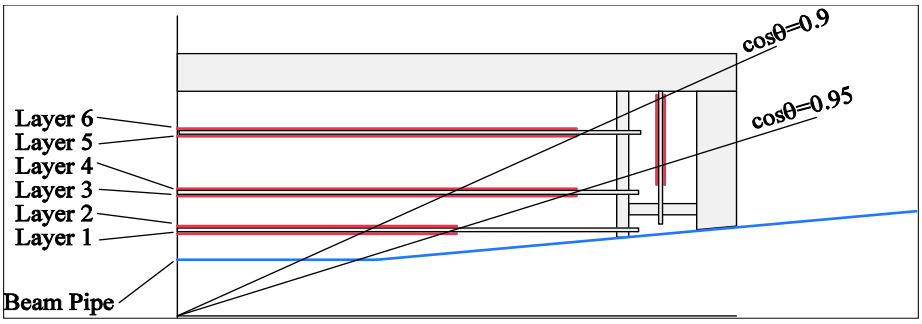

Figure 1: Schematic layout of an FPCCD-based ILC vertex detector showing pairs of sensor layers (in red) separated by 1-2 mm.

The second strategy is to readout multiple frames per bunch train. This can reduce the pattern recognition problem, but will drastically increase the requirements on the clock and readout.

3.1 Fine Pixel CCD

The Fine Pixel CCD (FPCCD) proposal uses the first ILC strategy, integrating over the bunch train[10]. The occupancy will be kept below 1% by using very small pixels: 5 μm $\times$ 5 μm. In order to reduce the probability of hits from beamstrahlung particles from being associated to nearby tracks, the vertex detector will be designed to have pairs of sensor layers attached on either side of rigid substrates, as shown in Figure 1. Hits correlated between the two layers in a pair will indicate a high transverse momentum track and hence be accepted for use in track finding. The low-energy beamstrahlung particle trajectories will intercept the sensor layers at a significant angle in the ϕ direction, and so the corresponding hits in the sensor pairs will be more separated than those from high transverse momentum tracks. Further discrimination can be obtained by rejecting clusters that have a significant extent in ϕ for the same reason.

The FPCCD Collaboration has produced and tested a small prototype sensor with 12 μm $\times$ 12 μm pixel pitch. The design uses a multi-node readout to keep the serial clock speed at 10 MHz.

3.2 Column Parallel CCD

The Column Parallel CCD (CPCCD) approach uses the second ILC strategy, aiming to readout 20 times per bunch crossing with a resulting hit density of only 10/mm^2 in the inner layer. For a 20 μm $\times$ 20 μm pixel detector that is 10 cm long, this will require a parallel clock of 50 MHz, even when read out from both ends. At such rates a serial clock would be impossible to implement, so the CPCCD concept requires a separate amplifier, ADC and readout for each column. This can be provided in the form of an ASIC with inbuilt cluster-finding logic, bump-bonded with 20 μm pitch to the CCD.

Generating a 50 MHz clock signal and distributing it across a 10 cm^2 CCD will be challenging. The peak current required will depend on the clock voltage and the capacitance so both must be minimised, but tens of amps per sensor may still be needed. The device itself will have to be carefully optimised to minimise clock voltage drop and ensure that all pixels efficiently transfer charge.

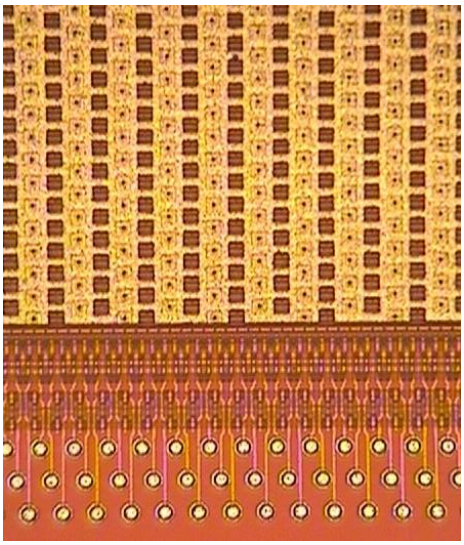

Figure 2: Micrograph of a CPC-2, with the upper clock metal layer clearly visible. The square holes are cut out to match impedance with the lower clock plane which has holes for the upper clock vias. The staggered 20 μm pitch bump bond pads are visible at the bottom of the picture.

The LCFI Collaboration[11] has made progress in CPCCD development, including the prototyping of CPCCDs and readout ASICs, their operation in bump-bonded assemblies and the use of clock voltages significantly lower than those in commercial devices. The latest generation of sensor, CPC-2, is a two-phase device that uses a novel "busline-free" (see Figure 2) approach. The clocks are distributed via metal planes over the imaging area, reducing resistance and improving the uniformity and speed of the clock signal propagation. It also has columns with direct charge outputs as well as those with more conventional voltage outputs, and other novel features.

The CPC-2s manufactured include a variant with an active length of 90 mm (approximately the size envisaged for a sensor in an ILC vertex detector), and a 10 mm-length variant has been shown to have 75 e^- system noise when operated at 10 MHz (Figure 3). High-speed operation was limited by the test system, but reasonable signal-to-noise at 45 MHz has been demonstrated.

The readout ASICs for the LCFI programme were designed at RAL. CPR-2A[12] includes a charge or voltage amplifier plus ADC for each channel (20 μm pitch) and cluster-finding logic. Its operation has been demonstrated bump-bonded to a CPC-2 and in a test mode using a digital input register.

The high speed/high current clock signals in the LCFI test programme were provided by either a custom clock-drive ASIC or via planar air-core transformers implemented on a PCB[13].

3.3 Future Developments

In order to practically operate CPCCDs of order 10 cm^2 at 50 MHz, both the capacitance and minimum clock voltage must be reduced below those of the CPC-2 series. A series of small-scale CPCCDs has been produced to test a variety of advanced features, including shaped channels to reduce the voltage, and raised or semi-open gates to reduce the inter-gate capacitance. Testing of all of the variants is ongoing.

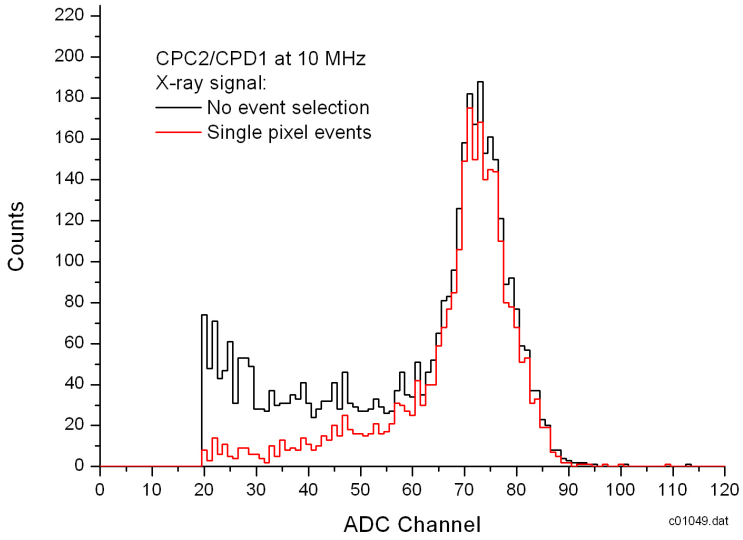

Figure 3: Distribution of single pixel charge in a CPC-2 exposed to an ^{55}Fe X-ray source. The CCD was clocked at 10 MHz using a drive ASIC with a system noise of 75 e^-.

Fabrication processes are now available that allow the same device to use both CMOS and CCD features. A sensor that consists of CMOS-type pixels with an internal CCD register could offer the best solution for the ILC, reducing clocking requirements and providing robust charge collection and storage during the bunch train. Such an Imaging Sensor with In-situ Storage is described elsewhere[14].

4. Summary

CCDs have a proven record as a technology choice for vertex detectors in fixed target and collider detectors. They offer a competitive combination of low mass and low power in the active volume. The use of CCDs at the LHC and some possible future experiments may be limited by radiation tolerance and readout speed, but they are an attractive option for future lepton colliders such as the ILC. The FPCCD and LCFI collaborations have been pursuing R&D for CCD use at the ILC, concentrating on reducing occupancy and incorrect pattern recognition caused by low-energy beamstrahlung electron pairs. FPCCD plan on using small-pitch pixels, correlated hits and cluster shapes, while LCFI plan on a column-parallel readout scheme to allow multiple frames per bunch crossing. Both projects have successfully tested prototypes, but the optimum solution for the ILC may ultimately be a CMOS-CCD hybrid technology.

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