.

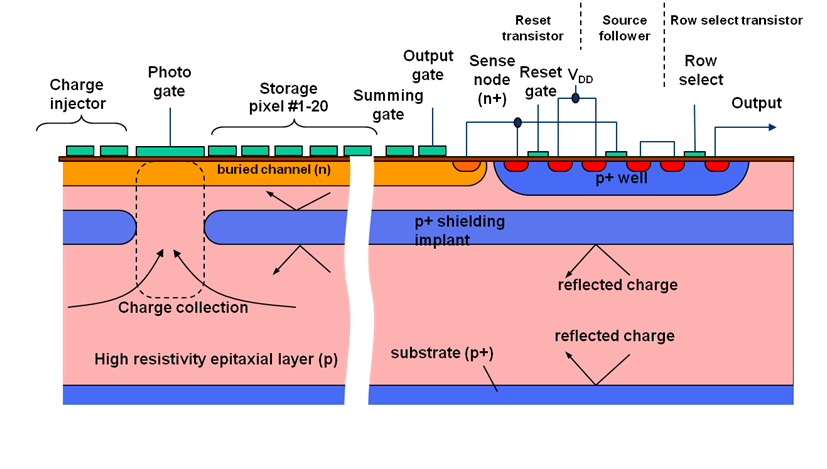


Figure ISIS principle

Image pixel

Physical pixel

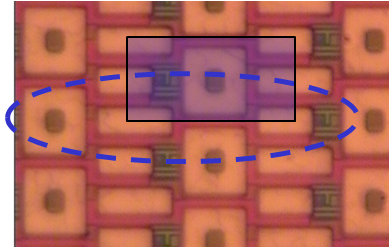


Figure Top view of ISIS2 pixel layout

IDR IG PG SG OG RG RD OD RSEL

OS

SS

IDR: Input drain

IG: Isolation gate

PG: Photogate

SG: Summing gate

OG: Output gate

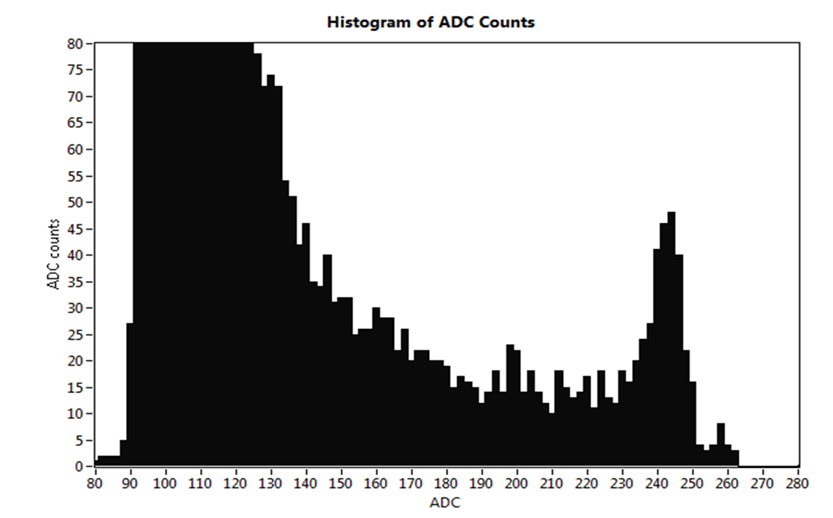
RG: Reset gate

RD: Rest drain

OD: Output drain

RSEL: Row select

Figure Schematic of the test structure



55Fe Kα

55Fe Kβ

Figure Histogram of X-ray on node

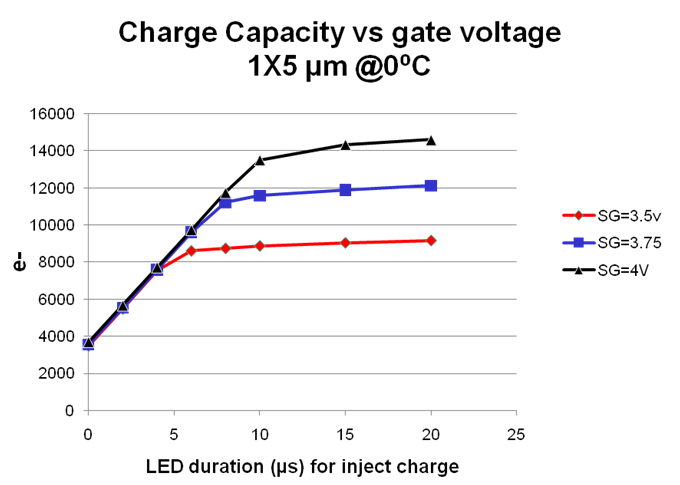


Figure Charge capacity of storage cell

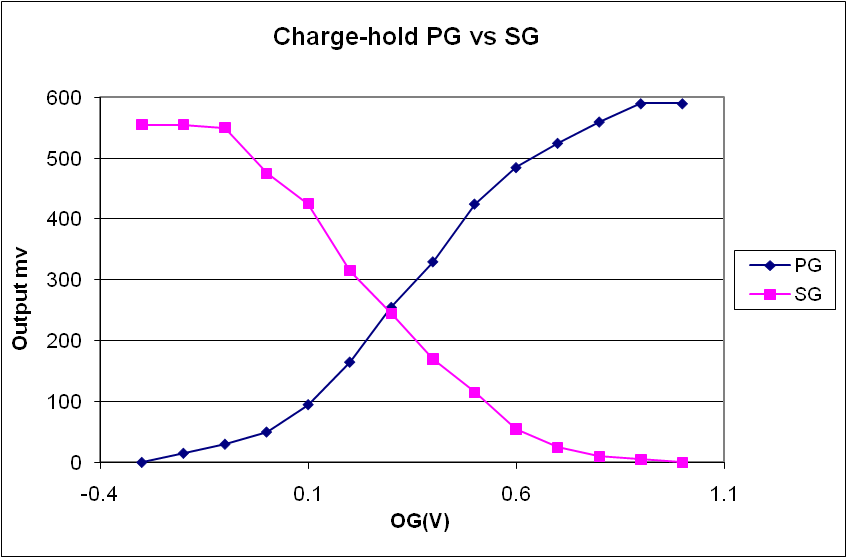
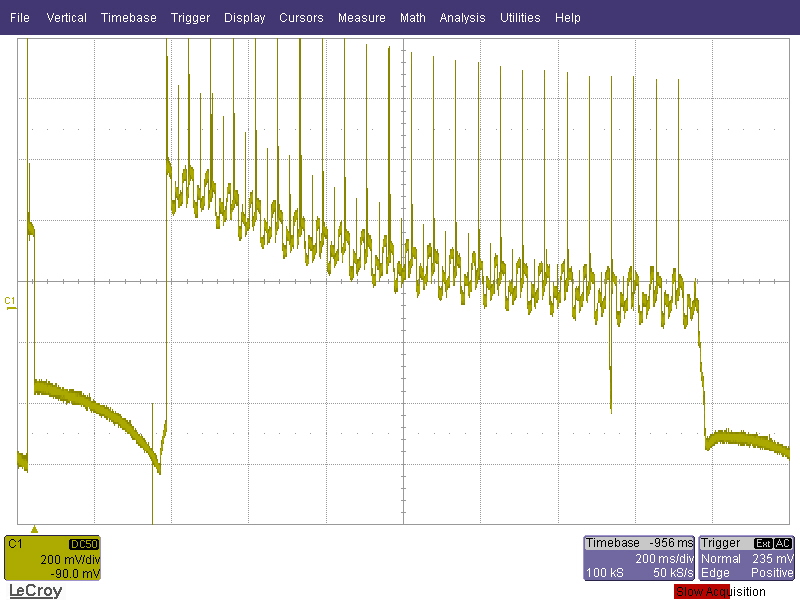


Figure Charge held by PG vs SG with different OG



LED on node

Clock feedthrough and

node reset

Signal on node

Figure LED signal on mainarray

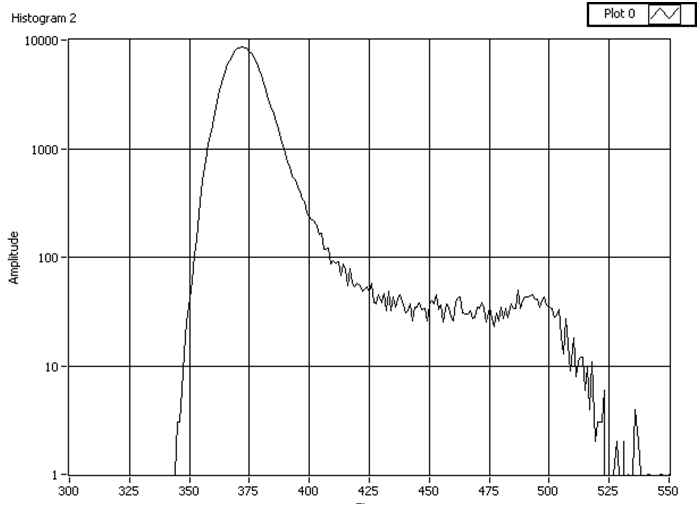


Figure Histogram of x-ray on one storage cell

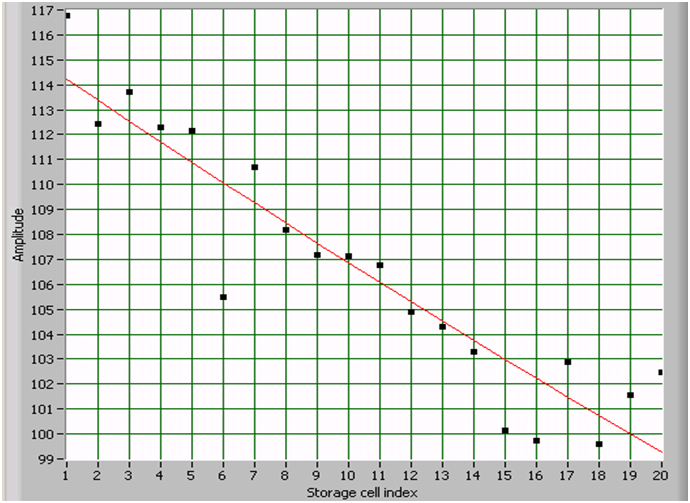


Figure 55Fe signal transferred from storage cells