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The InGrid chip post-processing technology for radiation imaging

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InGrid, the technology used to make CMOS-integrated high voltage electrodes for micropattern gaseous detectors is reviewed in this paper. It is presented in the broader context of CMOS wafer post-processing. This processing platform is briefly described, and recent highlights of this manufacturing approach are brought forward. The InGrid technology facilitates research into radiation imaging detectors with fully integrated electronics.

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1. Introduction

Traditional multiwire proportional chambers have found a downscaling limit at the point where electrostatic forces between the freely suspended wires lead to their excessive displacement (around 1 mm wire pitch [1]). A solution to this downscaling limitation is to fix the electrode wires to a supporting (insulating) structure, such as a foil [2] or a glass plate [3]. As miniaturization offers many advantages for a radiation detection system, such as low mass, low cost per readout channel, and high rate capability, it is an area of active research. In recent years a variety of micropattern gaseous detectors were proposed and realized, such as the MicroStrip Gas Chamber (MSGC) [3], Micromegas [4], Gas Electron Multiplier (GEM) [5], and InGrid (see [6] and references therein).

Micropatterned electrode configurations allow a direct integration with the front-end readout electronics. Such an approach exploits the benefits of microfabrication technology [7]: superior dimensional and alignment control, high purity materials, and low-cost mass manufacturing. In this regard, the InGrid (Integrated Grid) concept can thus be seen as the gaseous equivalent of the CCD- and MAPS-type[1] radiation imaging detectors [8][9]. This technology forms the basis of the GridPix and GOSSIP concepts presented elsewhere [10][11].

CMOS post-processing is a broad and very active field of academic and industrial research. This paper will first present a selection of recent advances in the field. The focus is on novel electronic components, integrated optics, and visible light imaging. Like the microsystems brought forward in [12] they can be considered exemplary of the typical technological possibilities of today, and of the application domains where wafer post-processing is rooting. To maintain focus, the paper only discusses true monolithic solutions. All hybrid-assembly approaches such as die-stacking are left out of the discussion.

The paper continues to review the main achievements in the InGrid technology research since its start in 2003. The choice of materials and building plan is motivated, key experimental results are summarized, and an outlook is presented.

2. CMOS post-processing

A previous review paper by the author [12] discusses how CMOS microchips can be post-processed to enhance their functionality. CMOS (Complementary Metal Oxide Semiconductor) technology is at present the most used and most versatile microelectronic platform. By post-processing on CMOS, we can use the regular supply chain of CMOS chips and add new functions on top. This is most effectively done by silicon wafer post-processing, although in some cases such as rapid prototyping, single-chip post-processing can be more practical. Key to success is to keep the underlying CMOS intact during post-processing. The processing possibilities are therefore limited, particularly by a temperature limitation around 400-450 °C.

Since the article mentioned above was written, a wide range of novel post-processing successes were reported in literature. Below, a selection of technological highlights is presented. These cases show the potential and achievements of post-processing in different application domains.

[1] CCD: Charge-Coupled Device. MAPS: Monolithic Active Pixel Sensor.

2.1 Novel electronic components

CMOS-post-processing can first of all alleviate some existing limitations of CMOS itself. Although the basic technology offers unprecedented (digital) computing performance at low cost and low power consumption, the building blocks of CMOS electronics exhibit a relatively poor analog performance. Typically, in standard-CMOS a capacitor, inductor or resistor will have non-ideal performance in the electrical domain, and may show a too high dependence on manufacturing variations and ambient temperature. A large technological effort is therefore devoted to high-performance passive components, integrated in or above the backend of CMOS chips. Higher-quality passive components are often offered in so-called process options, being extensions to the baseline (standard) CMOS process, at additional cost.

High-quality capacitors are available from several CMOS foundries as a process option in the CMOS backend, normally using a high-k dielectric film sandwiched in between two metal layers [13]. Precise and temperature-stable resistors also require some additional fabrication steps in the interconnect (see e.g. [14]). Inductors fabricated in the standard metallization layers of IC's can fulfill the needs of many analog-RF designers. A rather common extension of modern CMOS processes is a top-metallization layer of a few-micrometer thick copper, which is instrumental in the achievement of good inductor performance (as a result of the low wire resistance). Still such inductors are limited in quality factor to a few tens in the GHz range [15]. Post-processed inductors should have an edge, but to date do not exhibit a significant performance advantage over the well-engineered CMOS-integrated solutions (see [15],[16] and references therein).

A very promising new development is in the field of integrated resonators [17] [18]. High-quality mechanical resonators are being proposed for application as frequency reference signals (as a potential replacement of quartz oscillators), and within analog filters. The state-of-the-art integrated oscillators show excellent performance in the laboratory, with quality factors well over 1,000. They have a significant potential in the wireless communication domain.

2.2 Integrated optics

With optics and microelectronics as two of the pillars of the Digital Revolution, their fusion into electro-optical microsystems is a very active research domain [19]. This field is generally termed silicon photonics. A host of optical functions have been successfully manufactured using silicon-based planar technology. Furthermore, many examples of optical devices are developed explicitly with CMOS compatibility in mind (see e.g. [20][21][22]). It is generally agreed that the one missing ingredient for a widespread integration of optical and electronic functions is a CMOS-based (or silicon-based) light source. Semiconductor lasers and diodes normally emit light through radiative electron-hole recombination. This is difficult to enforce in silicon, because of its indirect band gap and the subsequent long radiative lifetime of carriers compared to competing (non-radiative) recombination processes.

The direct growth of direct-bandgap semiconductors, such as GaAs and GaN, on silicon may solve this issue [23]. Other recently proposed solutions include a silicon Raman laser [24] and an epitaxial germanium LED [25]. One step further would be to use plasmons rather than photons on the surface of a chip [26]. This may eventually lead to higher integration densities, especially when electrically pumped plasmon sources can be integrated [27].

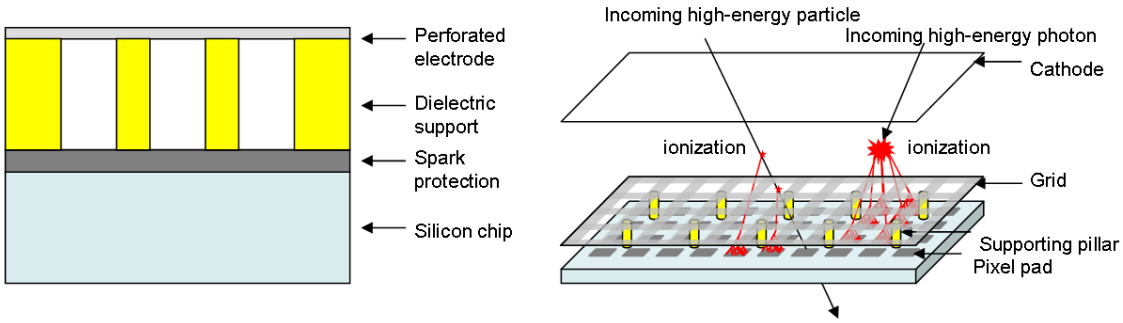

Figure 1: Left: the three key layers constituting InGrid on a chip: from bottom to top, a spark protection layer, a dielectric support structure, and a perforated conductor acting as a high voltage 'grid' electrode. Right: the detector configuration for radiation imaging using this microsystem.

2.3 Visible light imaging

The CCD and CMOS-APS sensors have recently revolutionized photography. Digital image recording is an economic and efficient alternative to silver halide technology. These image sensors are the result of vast research into many alternative hardware implementations. The CMOS-APS sensor can be regarded as a CMOS-post-processed microsystem, as lenses and color filters are added on top of (sometimes standard) CMOS [12].

In recent years, several APS-like image sensors have been proposed where the sensor element, converting light to an electrical signal, is positioned above the metallization layers. In regular CCD and CMOS-APS sensors, the sensing element is inside the silicon, next to the transistors. Hence, it competes for space with the pixel electronics. By stacking the sensor, more transistors can be designed-in per pixel without a loss of sensitivity. That is, if the post-processed sensors achieve a similar signal-to-noise ratio for incident light.

Such monolithic sensors have been fabricated in amorphous silicon [28], and in copper-indium-gallium-selenide technology [29]. Both these semiconductors are commonly applied in solar cells. Their fabrication on substrates has been well developed, and they offer high radiation tolerance.

3. Status of the InGrid microsystem

Compared to the novel CMOS-based microsystems mentioned above, the InGrid concept is relatively simple. By planar technology, a Micromegas is fabricated over a chip, kept in place by dielectric spacer material. It uses only 2 or 3 mask steps and 2 or 3 well-known materials. As a bonus, no packaging is needed, because the chips are directly mounted into a gas volume. Important manufacturing considerations are the relatively large vertical dimensions and the high voltages. The process technology for InGrids is detailed in [6].

The basic configuration of an InGrid is sketched in Figure 1. The CMOS microchip is first covered with a spark-protection layer. This high-ohmic layer prevents a spark from injecting large amounts of charge into the chip on a nanosecond time scale. As the charge will accumulate on the surface instead, the electric field will locally drop, effectively quenching the spark.

Experience has been obtained with this type of layers in resistive plate chambers (see e.g. [30]), and e.g. in MSGCs [31], where CVD-deposited diamond-like carbon films are employed. In our

devices, we chose for amorphous silicon and non-stoichiometric silicon nitride films. These films are more commonly applied in the semiconductor industry. Both layers have shown to successfully suppress the spark-induced damage, that originally led to sudden death of the detectors. A thickness between 3 and 20 μm is utilized.

The second layer is a dielectric support structure. Its height is typically 50 μm; with Micromegas research it was found that such a distance between the grid layer and the sensing electrodes, the gas gain in the detector is only weakly dependent on the precise distance [32]. This relaxes the manufacturing tolerances. However, in comparison to standard integrated-circuit technology, a height of 50 μm is enormous. Equipment optimized for microchip fabrication is not well suited for depositing such thicknesses. Apart from this practical constraint, residual stress may become a factor of concern.

SU-8 shows little stress, and is easily deposited in thicknesses between 2 μm and 3 mm. Moreover, it has found widespread use as a permanent construction material in a host of microsystems [33]. The choice for SU-8 has enabled rapid prototyping. Standard lithography is used to pattern it; and the undeveloped film is used as a temporary underlayer for the electrode deposition.

The top layer acts as a field-shaping electrode equivalent to a Micromegas foil. It draws little current in normal operation, so it may be high-ohmic. In practice, the choice of materials here is particularly limited by the underlying SU-8. The electrode deposition should not affect the SU-8 layer. Many material depositions will lead to radiation or heat generation, leading to crosslinking of the SU-8 and hence a loss of the intended pattern. This may be a motivation to replace SU-8 with a different dielectric in the future.

For the top layer, all experimental results reported by us are obtained with (pure) aluminum, with a thickness around 1 μm. InGrid production attempts with other materials have consistently shown that aluminum is easier to work with, because of its good adhesion, ductility and ease of wire bonding. Silver and copper seem viable alternatives [34], but these metals are more prone to corrosion.

The layer thicknesses can be chosen with a relatively large degree of freedom. They are determined by the deposition details. The entire structure is solid from beginning to end, with the membrane only being released at the very last process step. This implies that this Micromegas electrode does not need to be self-supporting (contrary to normal Micromegas foils). Therefore, very open geometries and very thin membranes could be applied without an excessive risk of deformation. Figure 2 presents an example of such a very open geometry.

The technology mentioned above can be employed to produce a variety of grid arrangements. Layers of SU-8 and aluminum can be stacked multiple times. The alignment of such layers is routinely done with high accuracy. Application of a multitude of electrodes can improve the overall gas gain, reduce the ion feedback, and lead to a faster signal [35].

In previous articles, the basic functionality of InGrid detectors has been shown. The device is capable of imaging X-ray conversions, minimum ionizing particle tracks (in 3 dimensions), and near-UV light, with good efficiencies. In these investigations, the Medipix family of microchips and the co-developed readout infrastructure have been instrumental [36][37][38]. For the InGrid technology to find application in particle physics experiments, a custom integrated circuit may have to be developed, to cope with high data rates. The circuit architecture may be chosen similar to pixel detector readout chips developed for the LHC-experiments ATLAS [39] and CMS [40]. The

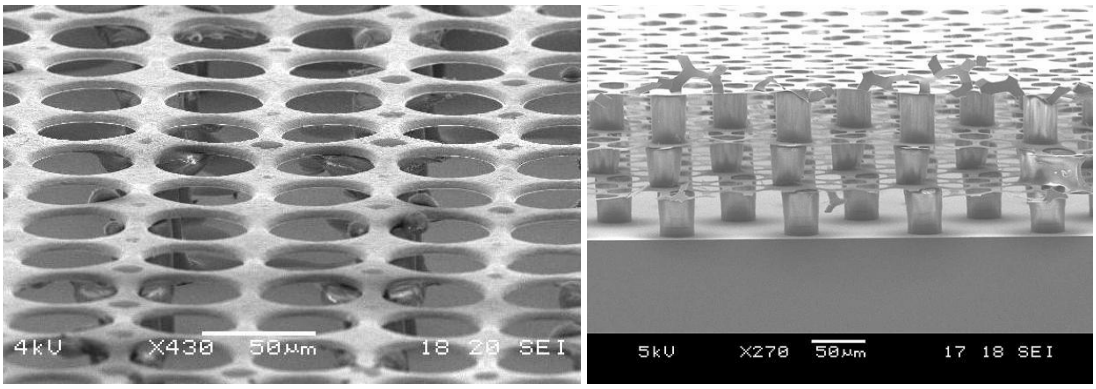

Figure 2: Left: an InGrid with relatively wide openings [34]. The top electrode is electroplated copper with an overall thickness of 5 μm. Right: three stacked grids on a dummy silicon wafer, showing the feasibility of multiple electrode stacking. SU-8 and pure aluminum are used. The irregular front edge of the grids is an artifact of the SEM sample preparation.

lower bias current and input capacitance in InGrid detectors allow a frontend with lower input noise and lower power. A custom-designed electrostatic discharge protection circuit might be advisable on each pixel for robust detector operation.

4. Conclusions

In this article, recent advances of CMOS post-processing technology are highlighted. In the application domains of analog electronics, visible light imaging, and integrated optics, breakthroughs have been reported. Wafer post-processing thus is gaining ground as a technology platform for novel microsystems. The InGrid detector is exemplary of the potential of CMOS post-processing in radiation imaging. Its status is reviewed in this paper, with a focus on the manufacturing.

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References

[1] F. Sauli, *Applications of gaseous detectors in astrophysics, medicine and biology*, CERN-PPE/92-47 (1992).

[2] M. J. Neumann and T. A. Nunamaker, *Modification of the Charpak chamber with foil supported conductors*, IEEE Trans. on Nucl. Sci. 17(3) (1970) 43.

[3] A. Oed, *Position-sensitive detector with microstrip anode for electron multiplication with gases*, Nucl. Instr. and Meth. A263 (1988) 351.

[4] Y. Giomataris, P. Rebourgeard, J. P. Robert, and G. Charpak, *MICROMEGAS: A high-granularity position-sensitive gaseous detector for high particle-flux environments*, Nucl. Instr. and Meth. A376 (1996) 29.

[5] F. Sauli, *GEM: A new concept for electron amplification in gas detectors*, Nucl. Instr. and Meth. A386 (1997) 531.

[6] V. M. Blanco Carballo et al., *A radiation imaging detector made by postprocessing a standard CMOS chip*, IEEE El. Dev. Lett. 29(6) 585.

[7] M. J. Madou, *Fundamentals of microfabrication*, CRC Press, Boca Raton 2002.

[8] J. D. E. Beynon and D.R. Lamb, *Charge-coupled devices and their applications*, McGraw-Hill, London 1980.

[9] V. Re, *Status and perspectives of deep N-well 130nm CMOS MAPS*, J. Instr. 4 (3) (2009) P03005.

[10] H. van der Graaf, *GridPix: An integrated readout system for gaseous detectors with a pixel chip as anode*, Nucl. Instr. and Meth. A580 (2007) 1023.

[11] E. N. Koffeman, *GOSSIP: gaseous pixels*, Nucl. Instr. and Meth. 582 (2007) 858.

[12] J. Schmitz, *Adding functionality to microchips by wafer post-processing*, Nucl. Instr. and Meth. A576 (2007) 142.

[13] C. H. Chen et al., *A 90nm CMOS MS/RF based foundry SOC technology comprising superb 185 GHz f_T RFMOS and versatile, high-Q passive components for cost/performance optimization*, Proc. IEEE IEDM (2003) 39.

[14] H. S. Bennett et al., *Device and technology evolution for Si-based RF integrated circuits*, IEEE Trans. El. Dev. 52 (7) (2005) 1235.

[15] D. Yang et al., *A 65-nm high-frequency low-noise CMOS-based RF SoC technology*, IEEE Trans. El. Dev. 57 (1) (2010) 328.

[16] L. Gu and X. Li, *On-chip embedded toroidal solenoid inductors and transformers formed by post-CMOS micromachining techniques*, Micr. Eng. 85 (2008) 697.

[17] J. T. M. van Beek et al., *Scalable 1.1 GHz fundamental mode piezo-resistive silicon MEMS resonator*, Proc. IEEE IEDM (2007) 411.

[18] W.-L. Huang, Z. Ren, Y.-W. Lin, H.-Y. Chen, J. Lahann, and C. T.-C. Nguyen, *Fully monolithic CMOS nickel micromechanical resonator oscillator*, Proc. IEEE MEMS 2008, p. 10.

[19] L. Pavesi, *Will silicon be the photonic material of the third millenium?*, J. Phys.: Condens. Matter 15 (2003) R1169.

[20] L. Colace, G. Masini, G. Assanto, H.-C. Luan, K. Wada, and L. C. Kimerling, *Efficient high-speed near-infrared Ge photodetectors integrated on Si substrates*, Appl. Phys. Lett. 76(10) (2000) 1231.

[21] J. S. Levy, A. Gondarenko, M. A. Foster, A. C. Turner-Foster, A. L. Gaeta and M. Lipson, *CMOS-compatible multiple-wavelength oscillator for on-chip optical interconnects*, Nature Photon. 4 (2010) 37.

[22] L. Razzari, D. Duchesne, M. Ferrera, R. Morandotti, S. Chu, B. E. Little and D. J. Moss, *CMOS-compatible integrated optical hyperparametric oscillator*, Nature Photon. 4 (2010) 41.

[23] A. J. Steckl, J. H. Park and J. M. Zavada, *Prospects for rare earth doped GaN lasers on Si*, Materials Today 10 (7-8) (2007) 20.

[24] O. Boyraz and B. Jalali, *Demonstration of a silicon Raman laser*, Optics Express 12 (21) (2004) 5269.

[25] X. Sun, J. Liu, L. C. Kimerling, and J. Michel, *Room-temperature direct bandgap electroluminesence from Ge-on-Si light-emitting diodes*, Optics Lett. 34 (8) (2009) 1198.

[26] R. Zia, J. A. Schuller, A. Chandran, and M. L. Brongersma, *Plasmonics: the next chip-scale technology*, Materials Today, 9 (7-8) (2006) 20.

[27] R. J. Walters, R. V. A. van Loon, I. Brunets, J. Schmitz and A. Polman, *A silicon-based electrical source of surface plasmon polaritons*, Nature Mat. 9 (2010) 21.

[28] N. Moussy et al., *A highly reliable Amorphous Silicon photosensor for above IC CMOS image sensor*, Proc. IEEE IEDM (2006) 5.6.

[29] O. Matsushima et al., *A high-sensitivity broadband image sensor using $CuInGaSe_2$ thin films*, Proc. IEEE IEDM (2008) 267.

[30] P. Fonte, N. Carolino, L. Costa, Rui Ferreira-Marques, S. Mendiratta, V. Peskov, and A. Policarpo, *A spark-protected high-rate detector*, Nucl. Instr. and Meth. A431 (1999) 154.

[31] B. Boimska, R. Bouclier, M. Capeáns, W. Dominik, G. Million, L. Ropelewski, F. Sauli, A. Sharma, and T. Temmel-Ropelewski, *Progress with diamond over-coated microstrip gas chambers*, Nucl. Instr. and Meth. A404 (1998) 57.

[32] Y. Giomataris, *Development and prospects of the new gaseous detector "Micromegas"*, Nucl. Instr. and Meth. A419 (1998) 239.

[33] P. Abgrall, V. Conedera, H. Camon, A.-M. Gue, and N.-T. Nguyen, *SU-8 as a structural material for labs-on-chips and microelectromechanical systems*, Electrophoresis 2007, 28, 4539.

[34] V. M. Blanco Carballo, *Radiation imaging detectors made by wafer post-processing of CMOS chips*, Ph.D. thesis, University of Twente 2008.

[35] Y. Bilevych, V. M. Blanco Carballo, M. Chefdeville, M. Fransen, H. van der Graaf, C. Salm, J. Schmitz, and J. Timmermans, *TwinGrid: A wafer post-processed multistage micropatterned gaseous detector*, Nucl. Instr. and Meth. A610 (2009) 644.

[36] X. Llopart, M. Campbell, R. Dinapoli, D. San Segundo, and E. Pernigotti, *Medipix2: A 64-k pixel readout chip with 55-μm square elements working in single photon counting mode*, IEEE Trans. Nucl. Sci. NS-49 (5) (2002) 2279.

[37] D. San Segundo Bello, M. van Beuzekom, P. Jansweijer, H. Verkooijen, and J. Visschers, *An interface board for the control and data acquisition of the Medipix2 chip*, Nucl. Instr. and Meth. A509 (2003) 164.

[38] T. Holy, J. Jakubek, S. Pospisil, J. Uher, D. Vavrik, Z. Vykydal, *Data acquisition and processing software package for Medipix2*, Nucl. Instr. and Meth. A563 (2006) 254.

[39] L. Blanquart, J. Richardson, K. Einsweiler, P. Fischer, E. Mandelli, G. Meddeler, and I. Peric, *FE-I2: a front-end readout chip designed in a commercial 0.25-μm process for the ATLAS pixel detector at LHC*, IEEE Trans. Nucl. Sci. 51 (4) (2004) 1358.

[40] H.Chr. Kästli, M. Barbero, W. Erdmann, Ch. Hörmann, R. Horisberger, D. Kotlinski, and B. Meier, *Design and performance of the CMS pixel detector readout chip*, Nucl. Instr. and Meth. A565 (2006) 188.