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The Pixel Trigger System for the ALICE experiment

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The ALICE Silicon Pixel Detector (SPD) data stream includes 1200 digital signals (Fast-OR) promptly asserted on the presence of at least one pixel hit in each of the detector readout chips. This unique capability among the LHC vertex detectors allows the SPD to contribute to the first level trigger decision, improving background rejection in pp interactions and event selection in heavy-ion runs. The ALICE Pixel Trigger System receives from the SPD a 76.8 Gb/s data stream on 120 fibers. It extracts from it the Fast-OR signals (12 Gb/s) and processes them, delivering the results to the Central Trigger Processor. The overall latency of these operations is 830 ns. Various trigger algorithms can be implemented and processed in parallel. The Pixel Trigger System is now installed in the ALICE experiment and has been extensively used. This article describes the crucial features of the system. Measurements made during the testing and commissioning phases are discussed. Results from the operation of the SPD with the Pixel Trigger System during the cosmic runs and the LHC injection tests are presented.

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1. Introduction

The Silicon Pixel Detector (SPD) is the innermost detector of the ALICE experiment [1][2][3] at the CERN Large Hadron Collider (LHC) [4]. The SPD is a double layer barrel pixel detector [1][5]. It is constituted of 120 modules (half staves) staggered on a carbon fiber support structure, 40 on the inner layer and 80 in the outer one. The average radial distances of the two layers from the beam axis are $r = 39$ mm and $r = 76$ mm. The total length of the barrel is 400 mm. Each half stave includes two 200 μm thick silicon pixel sensors with 256×160 pixels measuring 50 μm ($r\phi$) by 425 μm (z). The two sensors are bump bonded to 10 readout pixel chips operating at $1/4$ of the LHC bunch crossing frequency, i.e. at ∼10 MHz.

Each of the 1200 front-end chips provides a digital Fast-OR output [6]. The Fast-OR output is asserted within 300 ns from a particle hit in any of the 32×256 (8192) pixel channels of the chip. The Fast-OR signals allow the detector to be operated simultaneously as a high resolution ∼10 Mpixel detector and as a low latency binary pad detector with 120 channels of 13×14 mm^2 effective size.

A Multi Chip Module (MCM) [7] on each half stave provides bias and control signals for the pixel chips and implements the communication interface to the off-detector electronics in the control room. Timing, trigger and control signals are received by each MCM via optical fibers. The transmission of data to the control room is also on optical links. The 10 Fast-OR bits of each half stave are continously transmitted by the MCM every 100 ns, together with feedback signals. A readout sequence of the pixel hits is initiated only after a positive trigger decision and the procedure is controlled by the MCM.

The ALICE Pixel Trigger System (PIT) has been implemented to allow the use of the Fast-OR signals in the ALICE first level (Level 0) trigger decision. For the proto-proton interactions program this allows to implement minimum bias trigger conditions, improving background rejection. Moreover, trigger conditions for rare events based on high multiplicity and on topological conditions (jets) are possible. Selection of events with large impact parameter using the Pixel trigger is foreseen for the research program with heavy ion collisions. All of the algorithms that have been investigated until now are based on topology or multiplicity of Fast-OR signals [8]. They can be implemented as boolean logic functions of the 1200 SPD Fast-OR signals.

The design, earlier developments and implementation details of the Pixel Trigger System have been previously published [9][10]. In the following we review the system as it is presently installed in ALICE. Some laboratory integration tests and measurements made before the installation are presented. Finally, we discuss the commissioning and the first operation of the Pixel Trigger System with the SPD in the ALICE experiment.

2. The ALICE Pixel Trigger System

2.1 Integration with the SPD detector, readout system and Central Trigger Processor

Fig. 1 is a system diagram showing the interconnections between the SPD, the readout electronics, the Pixel Trigger System and the Central Trigger Processor (CTP). The main system clock (40.08 MHz) and the trigger commands are distributed to all subsystems by the CTP via the local Timing Trigger and Control distribution network (TTC) [11]. The CTP and the PIT electronic

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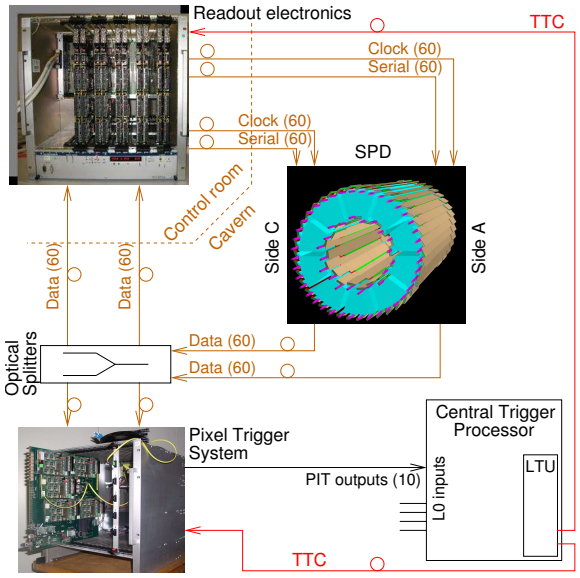

Figure 1: Simplified diagram of the control, readout and trigger connections between the Silicon Pixel Detector, the SPD readout electronics, the Pixel Trigger System and the Central Trigger Processor in the ALICE experiment.

crates are located in the experimental cavern, close to the ALICE apparatus. A limited space of only one standard 9U VME crate is available for all the electronic boards of the PIT. The SPD readout electronics is located in a control room $\sim$100 m far from the detector. The readout data fibers coming from the detector are connected to 120 passive optical splitters. One of the output branches forwards data to the readout electronics while the second one is connected to the Pixel Trigger System. This is totally decoupled from the readout electronics. The amount of data transmitted by the SPD is of 76.8 Gb/s during readout and of 38.4 Gb/s during idling. The bandwidth of the Fast-OR data is of 120×10 bits $\times$ 10 MHz $= 12$ Gb/s.

The Pixel Trigger System extracts the Fast-OR signals from the SPD stream and collects them into a Processing FPGA in which they are processed with fixed latency. Several logic functions can be implemented in parallel and the future evolution of the trigger algorithms is supported by reconfiguring the processing device from the control room. The result of each of the algorithms, updated every 100 ns, is a single bit trigger primitive. Up to ten primitives are transmitted simultaneously to the ALICE Central Trigger Processor where they can contribute to the first level trigger decision, based on inputs from several ALICE detectors. The total output bandwith of the Pixel Trigger System is 100 Mb/s.

The SPD on-detector electronics takes up to 375 ns to transmit the Fast-OR signals. The propagation delay on the fibers from the detector to the PIT is $\sim$225 ns and the serialization and deserialization latency is 125 ns. The transmission of the results to the CTP requires 30 ns. The PIT electronics takes only 75 ns to extract and process the Fast-OR signals. The overall latency from the particle interactions in the detector to the arrivals of the algorithm results to the CTP is less than 830 ns.

Positive trigger decisions are transmitted from the CTP to the readout electronics by the TTC link and relayed to the SPD half staves. A readout sequence is then initiated by the MCMs

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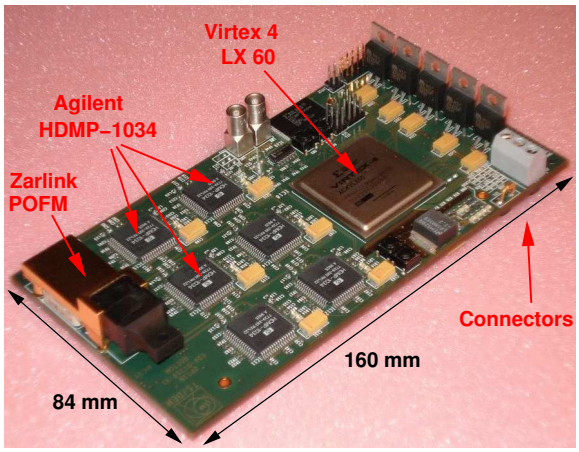

Figure 2: A photograph of the OPTIN board. The Parallel Optical Fiber Module, six deserializer ASICs and the FPGA are shown. Other six deserializer ASICs are on the bottom side of the board.

and the pixel hit data are transmitted back to the readout electronics on the data fibers.

2.2 The Pixel Trigger electronics

The Pixel Trigger System electronics is constituted by ten optical receiver boards (OPTIN) and one processing motherboard (BRAIN). The ten OPTIN boards connect as mezzanine boards on the BRAIN, five on each side.

Fig. 2 shows one of the receiver boards. The receiver boards deserialize the data and extract the Fast-OR signals from the data flow. Each OPTIN board implements 12 channels and receives data from 12 half staves. The OPTIN board is equipped with a twelve channels parallel optical fiber receiver module, twelve G-Link deserializer ASICs [12] and a 60k logic cells FPGA[1]. The components are densely arranged on both sides of a 160×84 mm^2 12-layer printed circuit board. The primary data path in the OPTIN includes blocks to extract, mask and time align the Fast-OR signals from the twelve modules. The 1200 Fast-OR signals extracted by the ten OPTINs are transmitted every 100 ns to the processing unit on the BRAIN board using $2\times$ time multiplexing (Double Data Rate transfer) on ten parallel buses, for a total of 600 striplines. The high degree of parallelism is required to satisfy the stringent requirement on latency.

The BRAIN electronic board (400×360 mm^2) hosts the Processing FPGA[2]. Fig. 3 shows a photograph of the BRAIN board with OPTIN boards plugged on two of the five locations on the visible side. Fig. 4 shows the Pixel Trigger electronics partially inserted into the hosting crate, prior to installation in the ALICE experimental area.

Several processing algorithms can be implemented in parallel in the Processing FPGA and the maximum number is limited by their complexity and by the available logic resources. Ten LVDS lines are used to transmit the results to the CTP, thus limiting to ten the number of algorithms that can be used simultaneously for the experiment. All algorithms implemented in the firmware up to now complete in one clock cycle (25 ns).

[1] Xilinx Virtex 4 LX60.

[2] Xilinx Virtex 4 LX100, 960 user I/O pins and 110592 logic cells.

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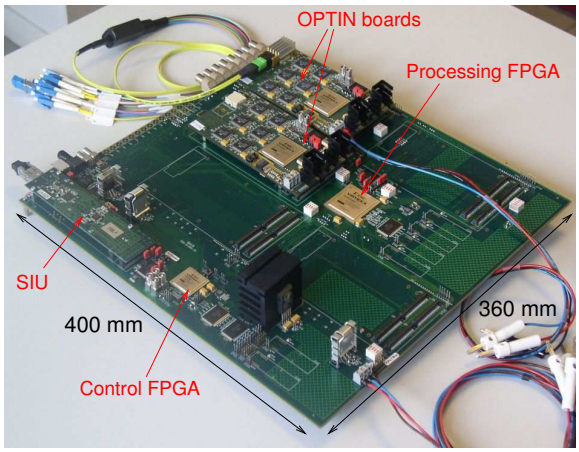

Figure 3: A photograph of the BRAIN board. The Processing and Control FPGA are indicated. OPTIN boards are connected on two of the five visible locations. Five other locations are on the other side of the BRAIN board. The ALICE DDL-SIU mezzanine board is also visible.

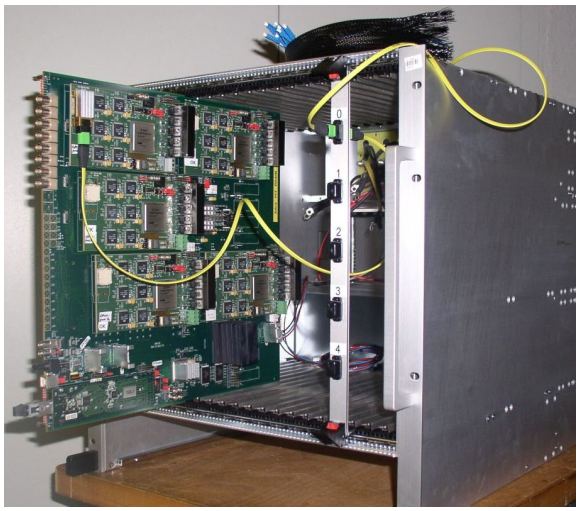

Figure 4: The Pixel Trigger System crate. The electronics board are partially extracted from the crate. Five OPTIN boards are connected on the visible side of the BRAIN board. One of the ten optical fiber fan-in cables and one optical patch panel are also shown.

The Control FPGA on the BRAIN board provides the control and communication functionalities. It manages a 32-bit shared bus that interconnects all the FPGA devices of the system as shown in Fig. 5. The custom bus protocol is a simplified version of the PCI protocol. The Control FPGA acts as the bus master, while the OPTIN boards FPGAs and the Processing FPGA are the target devices replying to the read and write transactions governed by the master. Parity checking and acknowledgement are performed in hardware for each bus transaction.

The ALICE Detector Data Link (DDL) is used as communication layer between the computer and the electronics [13]. The DDL Source Interface Unit (SIU) front-end board is the DDL interface on the BRAIN board. It is connected to the Control FPGA that acts as a bridge between the the DDL link and the board shared bus. The Pixel Trigger System is remotely controlled by a

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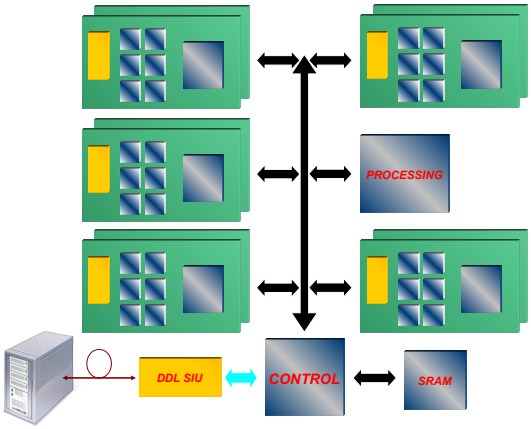

Figure 5: Schematic diagram of the custom communication bus. The Control FPGA is the bus master. It bridges the Pixel Trigger bus with the ALICE Detector Data Link interface, allowing control from the remote computer.

custom software driver executing on a dedicated computer [14]. The driver uses the hardware functionalities to check the integrity of each bus transaction, thus providing a highly reliable control layer.

3. Laboratory tests and measurements

3.1 Fast-OR data path Bit Error Rate tests

Bit Error Rate (BER) tests were done on the full data path of Fast-OR signals to qualify the integrity of the data receiving and processing chain. The setup used for these tests is schematically shown in Fig. 6. A hardware emulator of one half stave was used as data source. The emulator included a Pseudo Random Bit Sequence (PRBS) generator, an emulator of the MCM data protocol, a serializer chip identical to the one used on the MCMs and a laser transmitter. The optical signal was attenuated to operate in limiting conditions and fed into a 1×16 optical splitter. One OPTIN board was connected to one of the slots of the BRAIN. Twelve of the sixteen fibers were connected to the OPTIN using the same optical fan-in cables installed in ALICE. The twelve channels of the OPTIN were therefore receiving exactly the same optical signal. The optical power at the output of each fiber was 18.5 dBm with 50% Optical Modulation Amplitude, only 0.5 dBm above the minimum operating power required by the optical receiver module on the OPTIN.

The Fast-OR signals were extracted and transferred to the Processing FPGA. A set of bit comparators implemented in the Processing FPGA compared the data words received on pairs of channels. With this approach it was not necessary to reconstruct the transmitted word at the receiver end. The test was repeated on all the OPTIN boards in turn and connecting them onto different slots. Table 1 summarizes the results of the tests. In all cases no word errors and therefore no bit errors were observed. In a typical run the upper boundary on the Bit Error Rate was less than 8.1×10^{-13} at 99% confidence level [15]. No bit errors were detected even during two trials lasting ten times longer.

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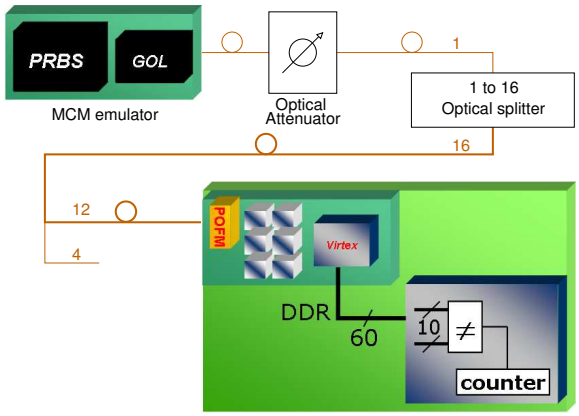

Figure 6: The experimental setup used for the Fast-OR Bit Error Rate tests.

Table 1: Fast-OR Bit Error Rate tests results. The typical test was made on eight OPTIN boards and lasted 1.5 hours. The entry labeled with Max refers to longer tests made on two OPTIN boards. BER upper bounds are evaluated at 99 % confidence level.

	Hours	N_{bits}	Errors	BER
Typical	1.5	5.7×10^{12}	0	$< 8.1 \times 10^{-13}$
Max	17.8	7.7×10^{13}	0	$< 6 \times 10^{-14}$

3.2 Control Bus Bit Error Rate tests

Dedicated tests were performed to qualify the custom control architecture. The software driver wrote, read back and checked blocks of random data from all the target devices on the Pixel Trigger System bus. The test was made on the system after installation in the cavern. A typical test lasted $\sim$15 mins and more than 6×10^8 bits were transferred during these runs. For two OPTIN boards the tests lasted about 12 h and a total of 3×10^{10} bits were exchanged in these cases. No bit errors were detected in all the trials. These tests qualified the reliability and robustness of the full control chain including the Alice DDL interfaces, the optical link, the communication interface blocks in the Control FPGAs and in the other eleven FPGAs of the system as well as the custom protocol of the shared bus and the Pixel Trigger System driver software.

4. First operation in ALICE

Table 2 describes the ten algorithms that were selected for the first production release of the Processing FPGA firmware. Nine of them are based on multiplicity. Thresholds can be programmed via software on the number of Fast-OR signals active on the inner, on the outer or on both SPD layers. One of the ten outputs is dedicated to coincidence algorithms. The coincidence logic can be programmed selecting from a set of predefined geometrical combinations.

The Pixel cosmic trigger requiring two simultaneous hits, one on the top half and one on the bottom half of the SPD outer layer, was extensively used during the commissioning of the SPD detector and of the ALICE experiment. Fig. 7 shows the SPD online monitoring display with a cosmic ray event. The cosmic trigger rate ranged from 0.09 Hz to 0.12 Hz depending on the number of active SPD modules. This was well in agreement with the results of a Monte Carlo simulation

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Table 2: Pixel trigger algorithms selected for the first release of the Processing FPGA firmware. N_I is the number of Fast-OR active on the inner layer, N_O is the number of Fast-OR active on the outer layer, N_{I+O} is the total number of active Fast-OR. Independently programmable thresholds (th) and offsets (ΔN) can be set for each algorithm.

Algorithm	Logic
Minimum bias	$N_{(I+O)} \geq th_{(IO,mb)}$ AND $N_I \geq th_{I,mb}$ AND $N_O \geq th_{O,mb}$
High Multiplicity 1	$N_I \geq th_{I,hm1}$ AND $N_O \geq th_{O,hm1}$
High Multiplicity 2	$N_I \geq th_{I,hm2}$ AND $N_O \geq th_{O,hm2}$
High Multiplicity 3	$N_I \geq th_{I,hm3}$ AND $N_O \geq th_{O,hm3}$
High Multiplicity 4	$N_I \geq th_{I,hm4}$ AND $N_O \geq th_{O,hm4}$
Past Future Protection	$N_{I+O} \geq th_{I+O,pfp}$ AND $N_I \geq th_{I,pfp}$ AND $N_O \geq th_{O,pfp}$
Background 0	$N_I \geq N_O + \Delta N_I$
Background 1	$N_O \geq N_I + \Delta N_O$
Background 2	$N_{I+O} \geq N_O + th_{I+O,bnd}$
Cosmic	Programmable coincidences

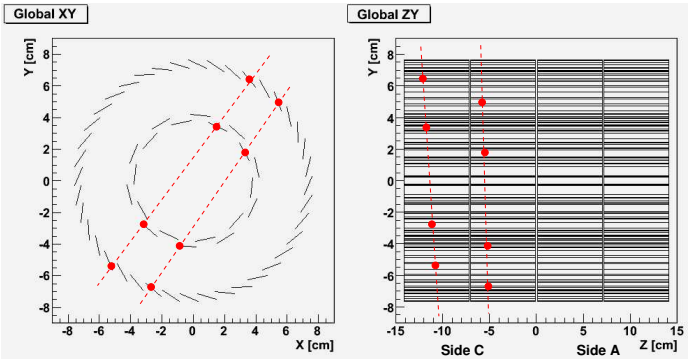

Figure 7: Cosmic ray event recorded by the SPD triggered by the Pixel Trigger System. Two muon tracks are visible, each generating four hits in the two layers.

of the detector including the measured muon flux in the ALICE cavern. The SPD cosmic trigger is the highest purity ($\sim 99.5\%$) cosmic trigger for the ALICE experiment.

The recorded cosmic ray data proved extremely useful for the commissioning of the SPD, of the Inner Tracking System combined with the ALICE Time Projection Chamber and for the tuning of the detectors geometry in the offline reconstruction software. More than 65000 events with at least 3 hits clusters in the SPD and more than 35000 with at least 4 were recorded to date, as well as several events with showers developing in the TPC and traversing the SPD with high occupancy.

Starting from August 2008 a number of beam injection tests were made at the LHC, in the section of the collider preceding the ALICE cavern. The beam was dumped either at the end of the transfer line or just before reaching the ALICE cavern. The SPD was operated together with the Pixel Trigger System during all these tests and several high occupancy events were recorded due to particle showers from the beam dump. Fig. 8 shows an example. The recorded events contain long straight tracks developing parallel to the beam axis for several centimeters in the 200 μm thin active volume of the silicon sensors. Some tracks in these events cross the gaps between adjacent

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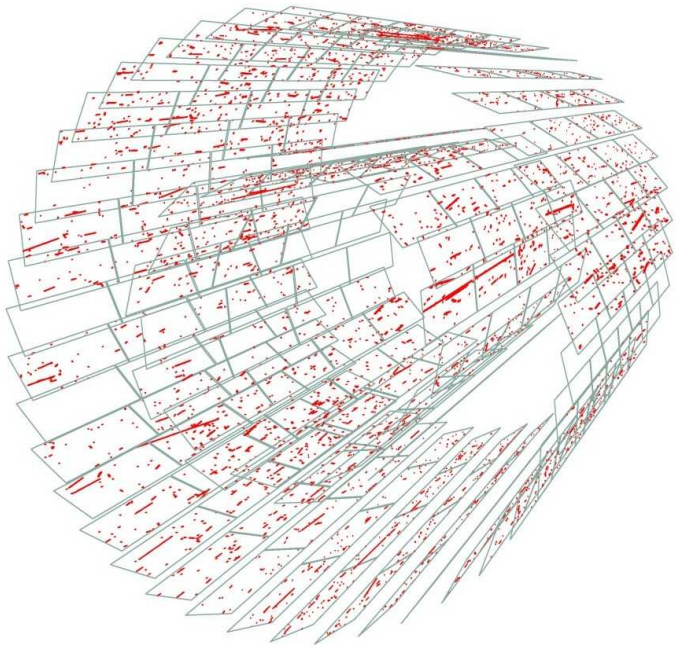

Figure 8: Event display of one of the events recorded during LHC beam injection tests. This three dimensional rendering shows the SPD silicon sensors and the recorded pixel hits.

sensors and adjacent readout chips. The injection tests were also used to commission the ALICE trigger system. The time alignment of the various trigger detectors benefited from the high purity and time accuracy of the SPD Level 0 trigger, used as the absolute time reference for the alignment.

Candidate beam-gas interaction events were also recorded during further LHC commissioning activities, including the first capturing and circulation of beams in September 2008, before the damage to the collider occurred.

5. Conclusion

The 1200 front-end chips of the ALICE Silicon Pixel Detector feature a low latency Fast-OR output that can be used for triggering purposes. The Pixel Trigger System allows to include the Fast-OR outputs in the first level (Level 0) trigger decision of the ALICE experiment.

The Pixel Trigger System is a very compact electronic system with a parallel data flow architecture. It includes original developments and satisfies challenging requirements at the board and at the system level. The system has been thoroughly qualified after production with several laboratory tests. The Pixel Trigger System has been installed and commissioned in the ALICE experiment in June 2008 and it has been operated since then.

Events related to beam dumping or beam-gas interactions were recorded during the first LHC injection and beam circulation tests. ALICE is the only LHC experiment that will include the vertex detector in the first trigger decision from startup.

The pioneering self-triggering functionality of the ALICE SPD proved extremely useful during the testing and commissioning of the detector and later for the entire ALICE experiment. The two key elements enabling this functionality are the pre-processing of trigger primitives on the front-end

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chips and the availability of large bandwidth data collection and real time processing capabilities on off detector programmable electronics. Different circuit solution can be used for the circuitry on the front-end and the next generation of pixel readout chips will probably implement some form of trigger primitive generation similar to the SPD Fast-OR. The need to collect the trigger primitives in large, radiation sensitive FPGAs, poses constraints on the location of the off detector trigger electronics. This can have various implications on system aspects like the overall trigger latency and experience shows that these should be evaluated since the early phases of the design of the experiment.

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