

Hybrid pixel detector in the PANDA experiment

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The hybrid pixel detector is the innermost part of the tracking system of the PANDA experiment. Good spatial resolution, capability to manage a huge amount of data, due to the high interaction rate and the absence of the trigger signal, limited material budget, due to the particle momentum starting from few hundreds of MeV/c, particle identification using energy loss measurement and radiation hardness are the major features. To cope with these requests, a complete R&D program is in progress to study and design a custom detector, always based on the standard hybrid technology, but with thin epitaxial silicon sensors and readout developed by 130nm CMOS technology. Dedicated mechanical structures, using new materials, and cooling system are under study too. The detector layout description and results concerning first prototypes are reported.²

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1. Introduction

PANDA [1] is one of the main experiments foreseen at the new FAIR [2] facility at GSI, in Darmstadt. The apparatus will be installed on the antiproton High Energy Storage Ring (HESR).

The main physics goals will be: precision spectroscopy of the charmonium states, establishment of gluonic excitations, search for modifications of meson properties in the nuclear medium and precision gamma-ray spectroscopy of single and double hypernuclei.

To achieve this physics program PANDA apparatus has to be characterized by a coverage extended nearly to 4π solid angle, vertex reconstruction and good particle identification performances. A characteristic aspect of the experiment is the triggerless data acquisition system to manage an average number of $2 \cdot 10^7$ antiproton proton annihilations/s, meaning that hit identification, digitalization and data sparsification must be made locally since a continuous data transmission of all events will be implemented

In particular, the core of the apparatus is the Micro Vertex Detector (MVD), based on both pixel and microstrip silicon sensors [1], which is envisaged for the detection of charged particle hits with a resolution that yields an overall spatial resolution accuracy better than the characteristic decay lengths of the involved charmed mesons ($123 \mu\text{m}$ in the case of D^0) as well as those from kaons and hyperons. Energy loss measurement is mandatory to help the particle identification. Owing to particle momentum spectrum starting from few hundreds of MeV/c, limited material budget is requested, only a few % of a radiation length. Besides the detector has to cope with a fluence of about $5 \cdot 10^{13} \text{ n } [1\text{MeV}_{\text{eq}}]/\text{cm}^2$, estimated per year considering 6 months of data taking, for antiproton-proton interaction and incident antiprotons with 15 GeV/c momentum.

Furthermore, studying the hybrid pixel detector, particular care is requested to design the mechanical support structure of the MVD, like innovative solution for electronics power dissipation.

A custom solution for the front-end chip, developed in 130nm CMOS technology, using the Time-over-Threshold (ToT) technique [3] to implement the energy loss measurement is underway.

At present, the second reduced scale prototype (ToPix_v2) has been completely tested both for electrical functionalities and radiation damage. Meanwhile first hybrid assemblies with thinned epitaxial sensors were tested using radioactive sources, showing good performances [4]. Displacement damage test of some silicon diodes with neutrons from nuclear reactor has been performed, showing annealing effects on the high resistivity epitaxial silicon material used for these first prototypes.

2. Hybrid pixel detector

The MVD layout has been optimized to manage the PANDA requirements. It is composed by four barrels, the two innermost ones made of pixels, and the two outermost ones made of

double sided silicon strips. They are arranged around the interaction point, where there is the junction between the beam pipe and the target pipe. Six disks based on pixels are placed in the forward region along the beam pipe, the last two surrounded each by a ring of double sided silicon strips. In figure 1 a sketch of the MVD detector is presented.

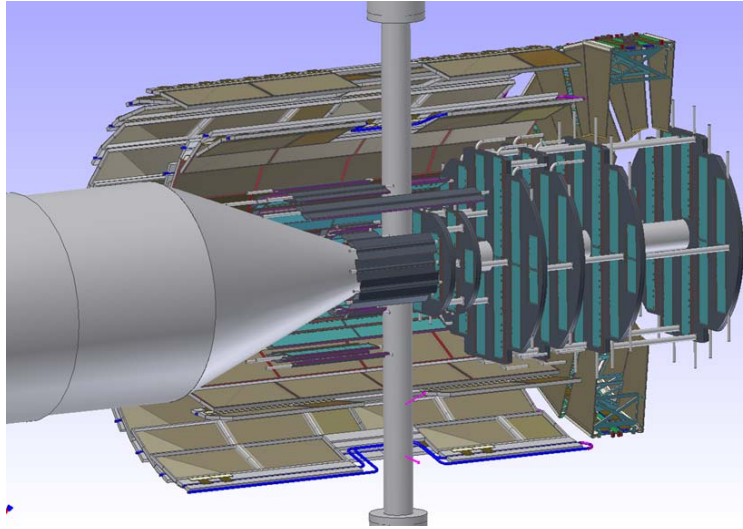


Figure 1: MVD detector around the beam pipe. The innermost pixel barrel is completely visible, the second pixel barrel and the two double side strips barrels are partially drawn to allow the six pixel disks visible. The last two pixel disks are surrounded by double side strips ring.

The hybrid pixel detector foresees pixel of $100\ \mu\text{m} \times 100\ \mu\text{m}$ size. The readout chip size ($13.8\ \text{mm} \times 11.2\ \text{mm}$) has been defined by the coverage optimization of the forward disks. The total number of readout chips for the whole pixel detector will be 824, each equipped with 12760 pixel readout cells. The total coverage of the detector requires about 10.5Mpixel, with a partition of about an half on the barrels and an half on the forward disks.

A hybrid pixel module is a stack consisting of tiled readout chips, directly connected by bump bonding to the same epitaxial sensor. On the other side of the sensor the bus for signal and power routing is glued and on the top a controller chip is arranged to communicate with the readout chips. Hybrids modules with a different number of readout chips (2, 4, 5 and 6) are needed in the detector; they are completed by controller chips that serve small sets composed by two or three ToPix with the possibility of daisy chain to save on cables. For barrel layers two 6-chip modules will be in chained configuration to keep low the number of cables in the active region. A preliminary sketch of the smaller module, made by two readout chips, is presented in figure 2.

2.1 MVD general mechanics

An external carbon fiber structure holds up the MVD (figure 3). In particular, this cylindrical frame supports directly the strips barrels and the conical structure arranged around the beam pipe at which the two pixel barrels are hooked up in a cantilever mode.

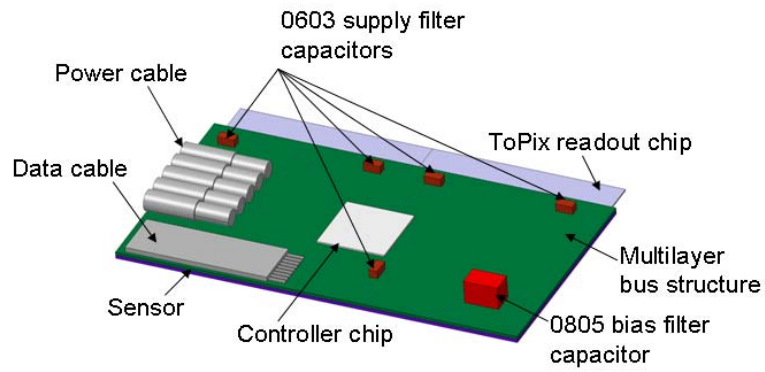


Figure 2: 2-readout chip module.

All the disks are arranged in a cantilever mode using an independent frame for allowing the insertion of this part inside the barrel structure and the positioning with respect to the external frame by the side opposite to the cone. All the system is split by two along the vertical plane.

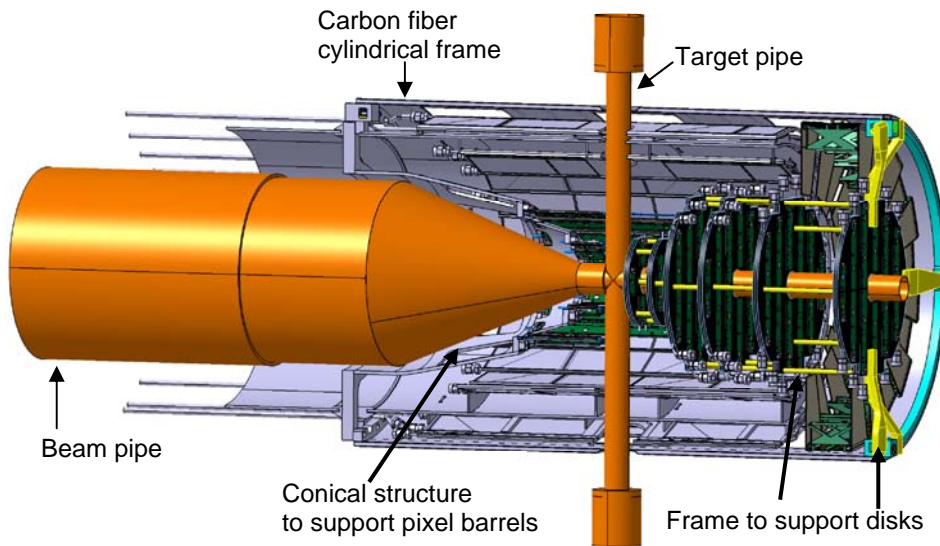


Figure 3: MVD drawing. Around the cross between the target pipe and the beam the MVD is arranged with its barrels and forward disks.

2.2 Pixel disk

By a preliminary design two slices of carbon foam glued together embedding cooling capillary make a pixel half disk (figure 4).

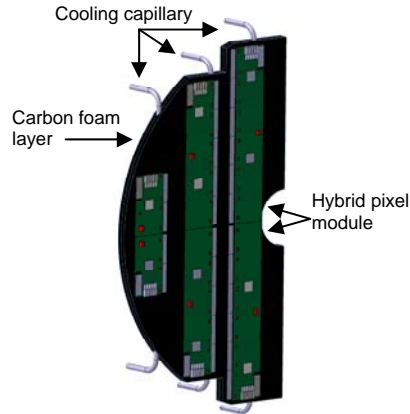


Figure 4: Half disk of the hybrid pixel detector

The hybrid pixel modules will be glued to both sides of the half disk in an alternate configuration to obtain the best coverage.

2.2.1 Pixel disk prototype

To study such solution a first prototype has been built (figure 5a). Six resistors, simulating readout chips with 1 cm² area, have been glued on both side of a structure composed by two slices of carbon foam, with a 4 mm thickness, glued together embedding cooling pipes made of the MP35N Ni-Co alloy (2 mm external diameter, 1.84 mm internal diameter) [5].

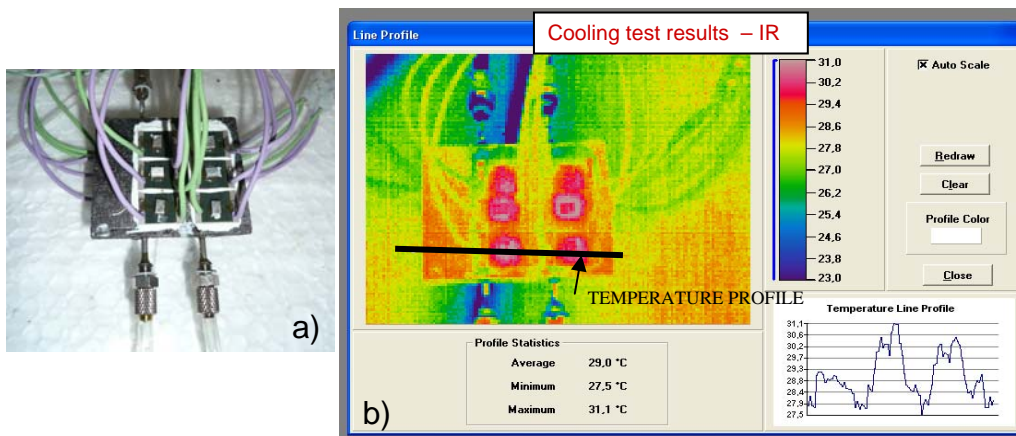


Figure 5: a) Prototype for studying the disk cooling system. b) Temperature map as obtained by a Infra Red picture.

Each resistor dissipates 1 W/cm^2 and the carbon foam is the Poco-HTC, that is graphite material with a high thermal conductivity developed at ORNL [6], the cooling fluid is water with a 18.5°C input temperature. In figure 5b a temperature map using an Infra Red photo camera is reported as result of a cooling test. The maximum reached temperature is about 31°C , an acceptable value for our project.

2.3 Pixel stave

Each stave of the pixel barrel foresees a hybrid pixel module glued to a carbon foam substrate supported by a Ω shaped structure, made of carbon fiber, including cooling pipe. In figure 6 is reported an example of stave.

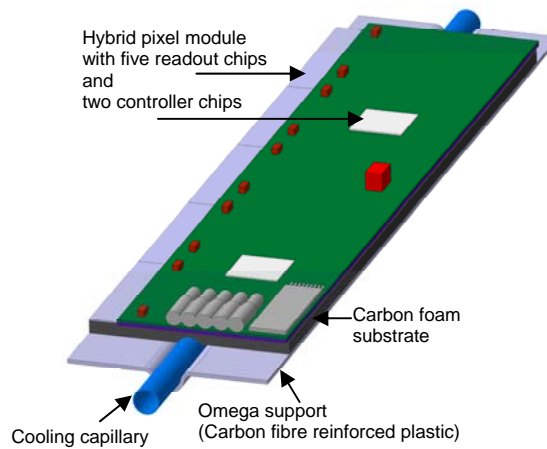


Figure 6: Example of stave for the pixel barrel

3. Front End Electronics

ToPix is the custom ASIC under development for the pixel readout and the specifications are: area of the order of 1 cm^2 , $100 \mu\text{m} \times 100 \mu\text{m}$ readout pixel cell, input range from 1 fC up to 100 fC , noise level $< 0.032 \text{ fC}$, energy loss evaluation within a dynamic range of about 12 bits measured by the ToT method, self triggering capability with a time measurement resolution better than 6 ns rms . The expected maximum event rate per cm^2 is $\sim 12.3 \text{ MHz}$ and the expected maximum data rate per chip is about 800 Mbit/s , taking into account a peak luminosity of $3.5 \cdot 10^{32} \text{ cm}^{-2} \cdot \text{s}^{-1}$.

3.1 ToPix_v2

ToPix_v2, [7][8] designed by 130 nm CMOS technology, is a reduced scale prototype equipped with 320 pixel readout cells arranged on four columns. Each readout cell ($100 \mu\text{m} \times 100 \mu\text{m}$ size) incorporates the analog and digital electronics necessary to amplify the detector

signal and to digitize the charge information at low power by the Time over Threshold (ToT) technique.

The circuit includes a charge sensitive amplifier with a feedback circuit based on a capacitor characterized by a constant discharging current, then the triangular shape signal feeds the comparator with a tunable threshold by a 5 bit DAC circuit. The time for which the signal is higher than the threshold is the ToT information, proportional to the charge from pixel sensor. At both the leading and trailing edges the time stamp is latched in two different 12 bit registers and the information is sent out from the cell when the readout phase starts.

The registers are based on the first level of DICE (Dual Interlocked storage Cell) architecture [9] in order to test this architecture to Single Event Upset effects. The chip circuit doesn't include enclosed structures and the layout foresees input pads on the chip perimeter for connecting external sensors by wire bonding technique with selectable input polarity.

3.1.1 Results of the characterization

Systematic tests [7] were performed both for electrical and radiation damage characterization of ToPix_v2. The measured average gain is 152 ns/fC with the deviation $\sigma = 6$ ns/fC, and thanks to the good linearity, even when the preamplifier is saturated, a high dynamic range ($1 \div 100$ fC) is achieved. The noise of the analog part is 0.025 fC, while the overall noise is about 0.032 fC (200 electrons) including the quantization error. The electrical functionalities were measured using the internal circuit for calibration purposes implemented in the chip layout.

Then one readout channel has been connected by using wire bonding technique to an epitaxial pixel ($125 \mu\text{m} \times 325 \mu\text{m}$, $50 \mu\text{m}$ thick) (figure 7) and a test with a ^{241}Am source has been performed.

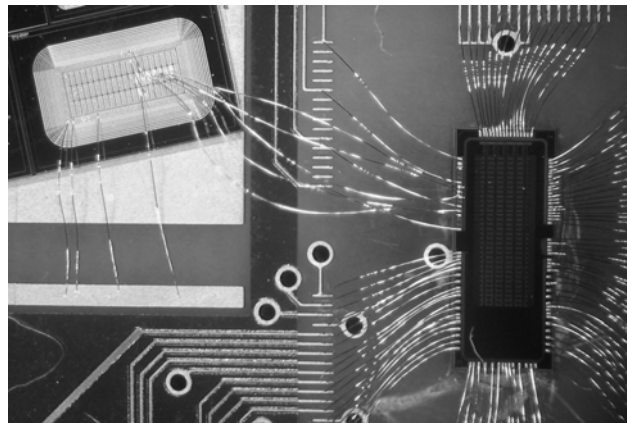


Figure 7: ToPix_v2 prototype (on the right) wire bonded to his testing board. Some pads are wire connected to pixel devices (on the left).

In figure 8 the 60 keV gamma rays signal has been reconstructed using the ToT information, with the noise $\sigma \sim 915$ electrons. The noise figure well agrees with simulations when the parasitic capacitances of the bonding pad and of the wire bond are properly taken into

account. In fact, the amplifier in this channel is connected to a standard wire bonding pad and the associated protection diodes have an extracted parasitic capacitance of 0.5 pF. An extra contribution in the range of 0.2÷0.4 pF is expected from the long interconnection between the chip and the sensor. Therefore the total capacitance is about 4 times higher than the one calculated for the final assembly (200 fF), where the chip will be mated to the sensor via bump bonding.

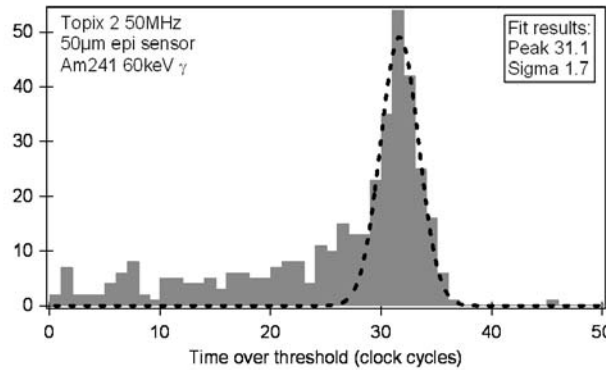


Figure 8: 60 keV gamma rays detection by 50 μm epitaxial pixel (125 μm x 325 μm sizes) connected with wire bonding to ToPix_v2.

TID (Total Ionizing Dose) test was performed at CERN using X rays and a ~ 400 rad/s dose rate up to a 35 Mrad integrated dose, it was followed by a 100°C annealing phase. The baseline variation, for the analog signal, was within 3%, the noise variation was $\sim 20\%$ and the average gain value increased twice. These last higher values can be explained taking into account that the leakage current in the constant current discharge circuit is of the same order of magnitude of the discharge capacitor current (few nA). The solution could be either to design the transistors in the sensitive circuit using enclosed structures or to increase the discharge current.

Single Event Upset (SEU) test has been performed investigating the radiation hardness of the DICE architecture, applied in the 12 bit configuration register of each readout cell. Preliminary analysis, taking into account the hadronic environment of the PANDA experiment, gives an expected average number of $\sim 6 \cdot 10^{-9}$ SEU bit $^{-1} \cdot \text{s}^{-1}$.

4. The epitaxial devices

Three n-epitaxial layer thicknesses were deposited on standard Czochralski (Cz) substrate wafers by ITME (Warsaw) and their characteristics are shown in table 1.

The Cz substrate parameters were equal for all wafers: n+ conductivity type, Sb dopant, 525 μm thickness, and 0.01÷0.02 Ωcm resistivity.

The wafers were processed by FBK-ITC (Trento) using ALICE pixel sensor masks provided by INFN-Ferrara. The sensor masks include full-size and single-chip sensors (the

ALICE pixel size is $50\mu\text{m} \times 425\mu\text{m}$) together with the usual range of test structures including simple diodes. The thinning of the sensor wafers and the bump-bonding to ALICE pixel readout chips were performed by VTT (Finland). The target thicknesses for the sensor wafers were chosen to be 100, 120 and $150\mu\text{m}$ respectively for the 50, 75 and $100\mu\text{m}$ epi layers, respectively Epi-50, Epi-75 and Epi-100.

Epi layer	Thickness	Resistivity
Epi-50	$49 \pm 0.5 \mu\text{m}$	$4060 \Omega\cdot\text{cm}$
Epi-75	$73.5 \pm 1 \mu\text{m}$	$4570 \Omega\cdot\text{cm}$
Epi-100	$98 \pm 2 \mu\text{m}$	$4900 \Omega\cdot\text{cm}$

Table 1: Thickness and resistivity of the epitaxial layers

A first test of displacement damage was performed using neutrons from the nuclear reactor (TRIGA MARK II) in Pavia (Italy) at the LENA laboratory to study the leakage current and the full depletion voltage.

The measurement of the I-V and C-V trends for different diodes have been carried out before and after irradiation as a function of the equivalent fluence and specifically with the following values: $5.13 \cdot 10^{13} \text{ n [1MeV}_{\text{eq}}\text{]}/\text{cm}^2$, $1.54 \cdot 10^{14} \text{ n [1MeV}_{\text{eq}}\text{]}/\text{cm}^2$ and $5.13 \cdot 10^{14} \text{ n [1MeV}_{\text{eq}}\text{]}/\text{cm}^2$ respectively corresponding to about 1, 3 and 10 years of PANDA lifetime, as maximum expected values. Then a careful annealing phase at $60 \text{ }^\circ\text{C}$ started and full depletion bias voltage and leakage current characterization have been performed many times during this period two months long. The full depletion voltage is evaluated from the intersection of the two extrapolated lines in the capacitance-voltage characteristic.

4.1 Results

The damage constant α is estimated as $\alpha = \Delta J/\Phi$. ΔJ is the difference between the diode volume current before and after the irradiation, both measured once the full depletion bias voltage has been reached. Φ is the corresponding equivalent fluence. The radiation damage parameter defined above is $\alpha = 7.6 (\pm 0.3) \cdot 10^{-17} \text{ A/cm}$ for all diodes.

The diode volume current for the three epitaxial thicknesses measured at full depletion bias voltage increased by 6 order of magnitude in the case of the irradiation fluence corresponding to 10 years of PANDA reaching the final value of $\sim 4 \cdot 10^{-2} \text{ A/cm}^3$, and it was halved already at the first measurement performed after 10 days of annealing phase. The reached high volume current corresponds to a leakage current of 40 nA/pixel , assuming a pixel volume of $100 \mu\text{m} \times 100 \mu\text{m} \times 100 \mu\text{m}$, which is the baseline choice for the PANDA MVD. The front-end electronics has a leakage compensation scheme designed to withstand a leakage current of 60 nA with a baseline shift smaller than 2mV .

The full depletion bias voltage is less than 7 V before the irradiation for all epitaxial diodes under test and it reached $\sim 22 \text{ V}$, 50 V , and 89 V respectively for Epi-50, Epi-75 and Epi-100 diodes after an irradiation fluence corresponding to 10 years of PANDA lifetime. Corresponding to the highest irradiation, the full depletion bias voltages, normalized to $50 \mu\text{m}$ thickness, as a function of the annealing time are reported in figure 9. Full depletion bias

voltages relative to 1 and 3 years of PANDA lifetimes show similar trends with lower values during the annealing phase.

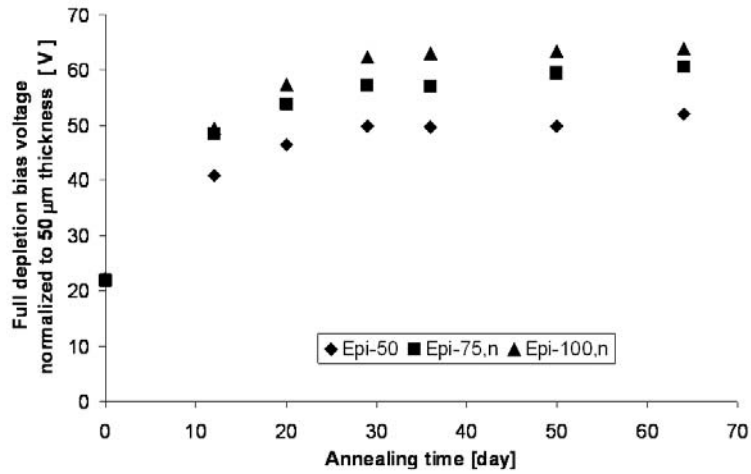


Figure 9: Annealing behaviours of the full depletion bias voltages as a function of the time for the 3 diodes irradiated at about $5.03 \cdot 10^{14}$ n [$1 \text{ MeV eq}/\text{cm}^2$]. The rhombus corresponds to a diode Epi-50, the square to a diode Epi-75, and the triangle to a diode Epi-100.

All bias voltage values are normalized to the $50 \mu\text{m}$ thickness. The values reported at time zero are the voltages of irradiated diodes measured before the annealing phase.

5. Conclusion

The custom pixel hybrid detector study for the PANDA experiment is ongoing. The second pixel readout ASIC prototype by 130 nm CMOS technology has been completely tested. In spite of satisfactory electrical performances, the analog part of the readout pixel cell has to be still improved to avoid large variation of noise and signal gain as a consequence of TID test. The DICE architecture has to improve in radiation tolerance characteristic to limit the SEU effects even if a triple redundancy architecture can be avoided with layout area saving.

Thin epitaxial silicon sensors are under study for radiation damage behavior. In particular, the epitaxial layer resistivity has to be investigated for the full depletion voltage optimization, with respect to short and long annealing periods.

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