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Development of low-mass, high-density, hybrid circuit for the silicon microstrip sensors in high track density environment

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We have fabricated a low-mass, high-density, hybrid circuit for the silicon microstrip sensors in high track density environment, such as the ATLAS silicon microstrip detector upgrade toward the super LHC project. A technology of copper-polyimide flexible circuit board and carbon-carbon reinforced material was applied to the hybrid. The weight of bare flex circuit for the hybrid is 1.91g. By using button plating techniques for via-holes and through-holes, a considerable weight reduction of 1.18g has been achieved compared with an usual plating. In this paper, a detail description for hybrid circuit is presented with a module design. Electrical test results of the front-end chips on the hybrid are also discussed.

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1. Introduction

Recent silicon microstrip detectors are designed to incorporate VLSI chips on the detector to readout the signals and communicate with the outside data acquisition system. The hybrid, the base for the VLSI chips and related circuit components, is required to be low mass to reduce multiple coulomb scattering effects for precision tracking. The proposed silicon strip detector at the super LHC experiment [1] includes a short strip silicon detector system in order to cope with the high track density. The system has about 10,000,000 readout channels. In order to minimize the number of hybrids, a circuit reads out 2 segments of strips with two rows of readout chips; one row at each edge. Thus, the density of readout chips is quite high, 20 chips on a hybrid in this application. We designed and fabricated a new hybrid, applying a technology of copper-polyimide (Cu/PI) flexible circuit board and carbon-carbon reinforcing material which have been developed and adopted for the present LHC ATLAS silicon strip detector (SCT [2]). This report is focused on the electrical performance of the hybrid.

2. Module components

Fig. 1 shows a module design for the barrel SCT upgrade toward the super LHC experiment. It is a double sided module, which can give 3D space points. The double sided module is made of an upper and a lower single sided sensor, a central baseboard and 4 separate hybrids. These hybrids are bridging over the sensor area with air-gap.

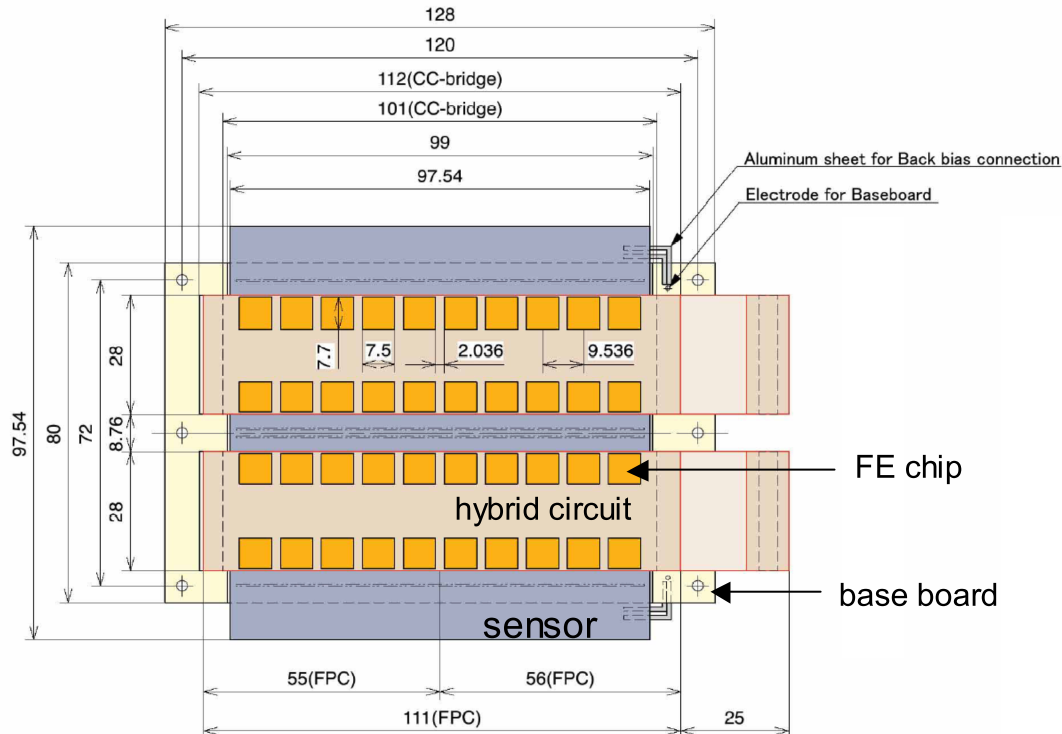

Fig.1 Module Design. Dimensions are in mm.

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The n-in-p type strip sensors [3] have been developed to cope with a fluence up to 10^{16} 1-MeV n_{eq}/cm^2. They have 4 segmentations for the requirement from hit occupancy. Each segment has 1,280 strips with 74.5μm pitch and about 24mm length. The sensor size is 97.5mm × 97.5mm.

The baseboard provides mechanical, electrical and thermal support. We are planning to fabricate modules by using two types of baseboard substrates: thermalized pyrolytic graphite (TPG) and carbon-carbon, and compare each performance. The TPG material has very high thermal conductivity of 1450–1850W/mK in plane, however, is intrinsically friable and easily delaminates. A parylene coating technique is adopted to prevent delamination of the substrate. The baseboard thickness is 300μm. Four Aluminum Nitride (AlN) ceramic facings are attached to the substrate. They have precision holes for the module mounting. The thermal performance of the hybrid and the module is discussed in [4]. The hybrid is described in the next chapter.

3. Hybrid

Fig. 2 shows a photo of the complete hybrid stuffed all components. Each hybrid has 20 front-end readout ASICs (ABCNext [5]), which can handle 128 channels. One module has 80 readout ABCNext chips and 10,240 readout channels. The hybrid provides the full specifications operation of ABCNext chips, including (1) two sets of bus lines for redundancy operation, (2) bypass scheme for a dead chip, (3) various powering schemes and (4) grounding schemes.

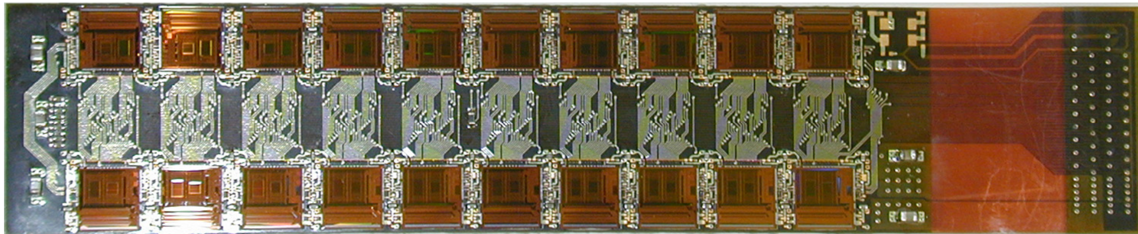

Fig. 2 Complete hybrid stuffed all components.

There are two links in the hybrid. Normal data flow is shown in Fig. 3 (A); the link0 and 1 are shown in blue and green, respectively. Each link handles 10 chips. If there is a dead chip shown in Fig. 3 (B), we can achieve a dead chip bypass scheme via the unusual data path.

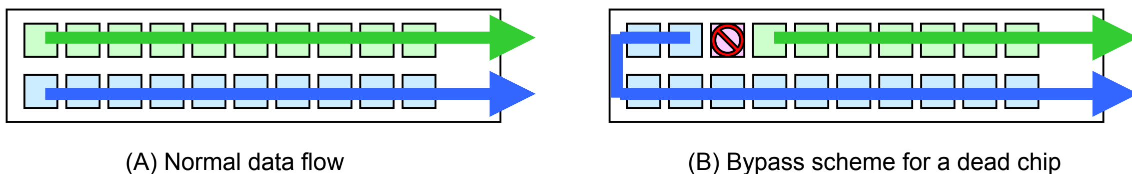

Fig. 3 Normal data flow and bypass scheme for a dead chip.

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The flexible circuit size is 136mm × 28mm. Fig. 4 shows layer structure of the flexible circuit. The starting core for build-up is a double-sided Cu/polyimide (PI) sheet in the middle. A single-sided Cu/PI sheet is glued on each side of the core sheet. The thickness of Cu layer and PI base film is 12μm and 25μm, respectively. In the cable part, the top and bottom copper layers are removed. The total thickness of hybrid part and of cable part is 0.295mm and 0.165mm, respectively. Electrical connections among different layers are realized by either through-holes, penetrating all layers, or laser-cut via-holes between two adjacent layers. All Cu/PI sheets are made with adhesive-less technology. We adopt button plating, which is also called pads-only plating or spot plating. The usual panel plating for via-holes and through-holes, as adopted in the current SCT flexible circuit, is plated to a whole surface. On the other hand, the button plating is plated to a limiting area of the via-hole and through-hole. By using the button plating, a considerable weight reduction of 1.18g has been achieved compared with the usual plating. The weight of bare flexible circuit is 1.91g. The layer 1 and layer 2 include the main circuit patterns for ASICs with redundancy lines. The layer 3 and layer 4 are mainly for the power distribution and grounding, respectively. The detailed description of flexible circuit is found in the reference [6].

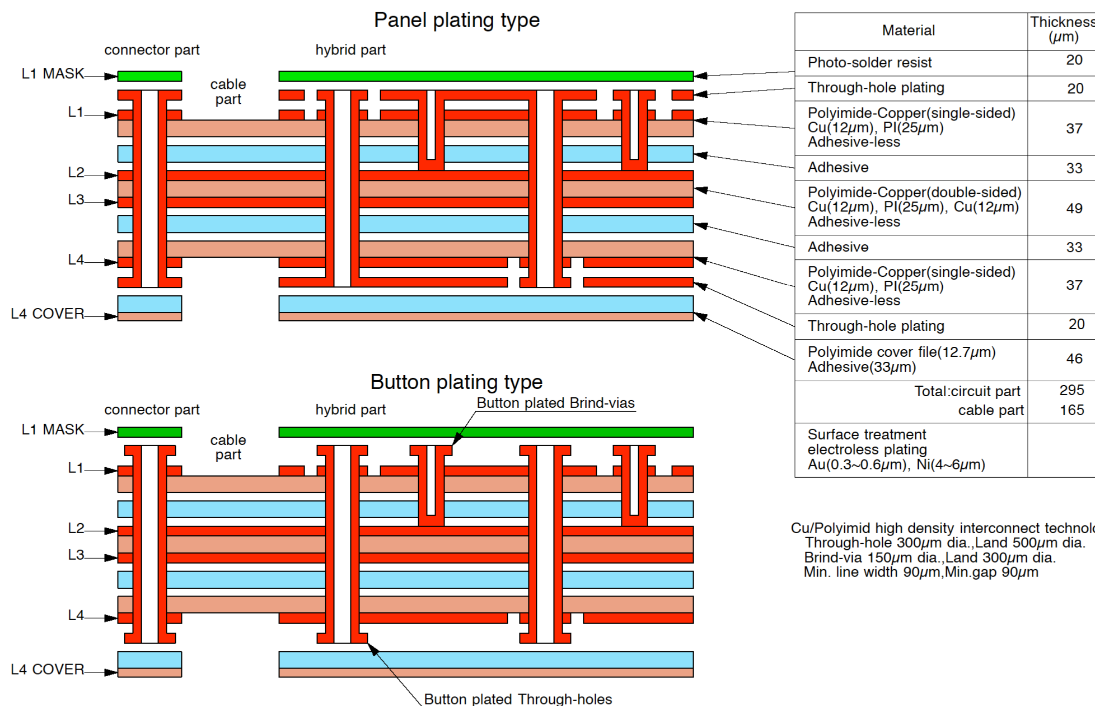

Fig.4 layer structure of the flexible circuit

The hybrid, backed with a 400μm thick and 112mm wide carbon-carbon sheet, is designed to bridge over the silicon sensor avoiding any interference to the sensor surface. The carbon-carbon bridge having large heat conductivity of 670W/m/K transfers the generated heat to the heat sink located at the legs of the bridge. The total weight (excluding electrical components) is 4.25g, having 0.00425 X_0 equivalent radiation lengths.

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4. Electrical Test Results

Threshold scans were performed for injected charges of 1.5, 2.0 and 2.5fC with the internal calibration circuit mounted in the ABCNext chip. In each case a complementary error function was fitted to the data: the mean corresponds to the threshold at which 50% efficiency was achieved for pulses of the designated magnitude and the sigma was a measure of the output noise (in mV). The gain of each channel was calculated from a linear fit to the fit results for the three scans. The output noise from the scan taken with 2.0fC injected charge was divided by the gain to determine the input noise (in fC or ENC: Equivalent Noise Charge). The hybrid was kept at 15°C in a climate chamber. Fig. 5 and 6 show a typical gain and noise distribution versus channel number, respectively. Quite uniform distributions for gain and ENC were obtained. The average gain and ENC were found to be about 100mV/fC and 400e, respectively. These results were consistent with design values. There was no difference by having button plating or not.

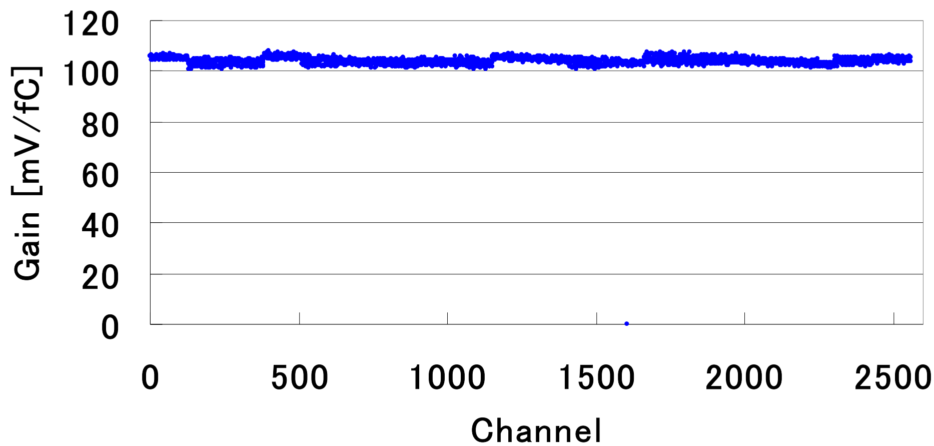

Fig. 5 Gain distribution.

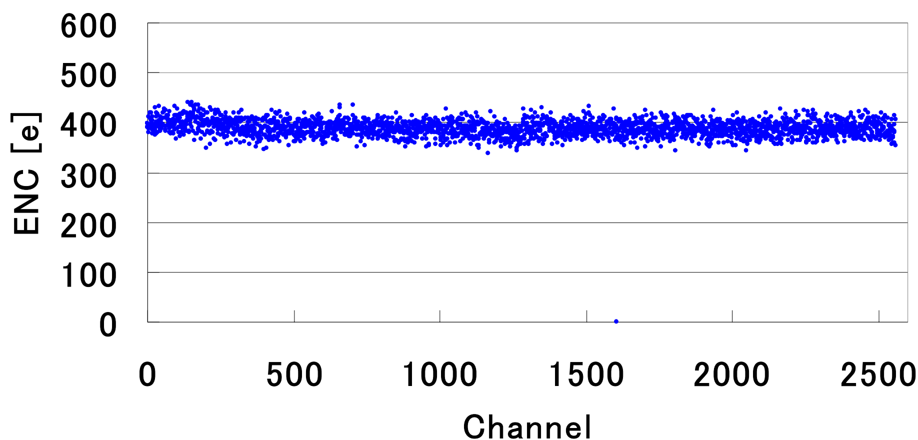

Fig. 6 Noise distribution.

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In order to investigate a change of ENC with a detector capacitance, we connected the input of amplifiers to several different external capacitors, and measured the resulting ENC. Fig. 7 shows the ENC measurement results. The detector capacitance range was measured [7] and was found to be in between 2.5pF and 9.8pF. The ENC measurements with external capacitors were performed at three sites independently [8] and the results were found to be in agreement.

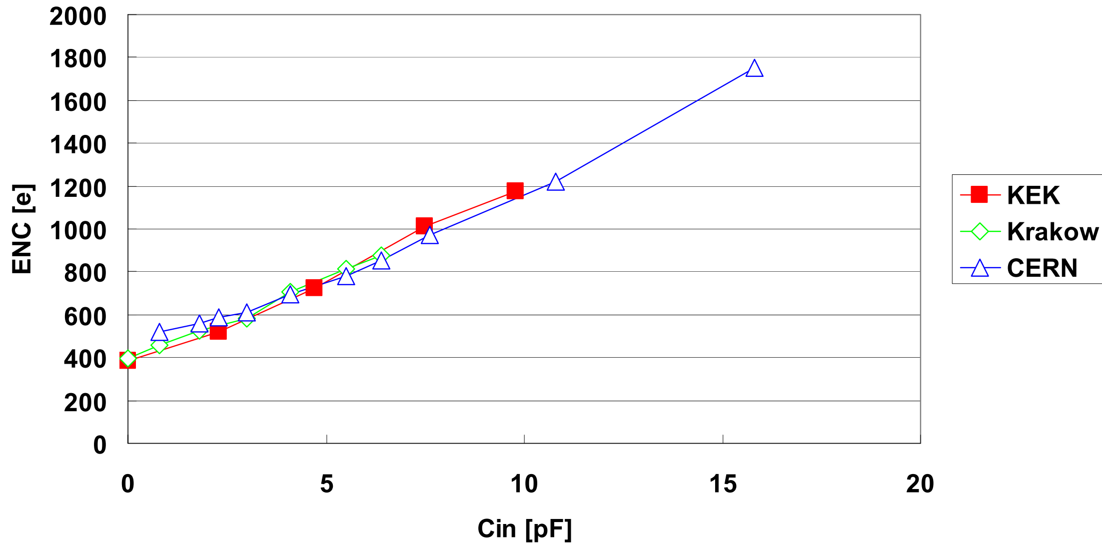

Fig. 7 Noise evaluation for detector capacitance

5. Summary

We have fabricated a low-mass, high-density, hybrid which provides the full functionality of the ABCNext chips. The weight of bare flex circuit for the hybrid is 1.91g. By using button plating techniques for via-holes and through-holes, a considerable weight reduction of 1.18g has been achieved compared with an usual plating. The electrical tests on the hybrid level are mostly completed.

We are planning to build and test 4 modules at Geneva and KEK sites. In the summer of 2010, all of the 8 modules will be installed in a realistic support structure at Geneva site.

Acknowledgements

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