PROCEEDINGS OF SCIENCE

Simulation of a Floating Gate Device in standard CMOS process for Dosimetry application

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The use of floating gate devices for storing digital information is well known. More recently, these devices have been proposed for analogue applications and for use in radiation detection. In this case, the charge generated in the SiO_2 due to the ionizing radiation is collected by the floating gate by virtue of the electric field generated by the charge stored in it. This in turn changes some electrical characteristics of the device that can be measured and referred to the absorbed dose of ionizing radiation. A comprehensive device simulation that includes the process of charging the floating gate via tunnelling and the mechanism of charge collection from the SiO_2 has been carried out using the process parameters of a standard CMOS 0.18µm technology. The results suggest that this device could be used as a sensitive integrated dosimeter that allows the fabrication of the readout electronics on the same silicon chip.

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1.Introduction

1.1 A CMOS Floating Gate Dosimeter

The radiation sensor device presented here is based on the effect of floating gate discharge from charge generated in SiO_2 exposed to ionizing radiation ([1]-[2]).The device is based on a standard CMOS process routinely provided by a semiconductor foundry ([3]). The process is normally used for the fabrication of non volatile memories (NVM) and features a single polysilicon floating gate. The charge is injected into (or erased from) the floating gate via tunnelling by applying a voltage bias to a programming contact of a digital inverter, the logic output of which is being read out to determine the state of the memory cell. The sensor device proposed here and simulated using TCAD ([4]) consists of a single NMOS transistor, see Fig. 1. The polysilicon floating gate covers a large area and controls the functioning of the NMOS device. This gate is insulated in SiO_2 and separated from the substrate by a layer of a few 100's nm thickness. The layer is much thinner near the tunnelling contact TG and over the region of NMOS channel. The minimum size injector TG, to which a bias voltage is applied, allows injection or erasing of charge into the floating gate via tunnelling effect. The small size of the injector with respect to the size of the floating gate allows an accurate change of the threshold voltage of the NMOS device. In this case the tunnelling injector contact TG serves the dual purpose of injector and control gate of the NMOS transistor. Depending on the sign and amount of charge stored in the floating gate, the electric field in the surrounding SiO_2 modifies its intensity and direction. The charge generated in the SiO_2 by ionizing radiation is then initially separated, with an efficiency that depends on the local intensity of the field, and eventually partly collected by the floating gate, which discharges. This causes a shift of the threshold voltage of the device related to the amount of deposited dose of radiation.

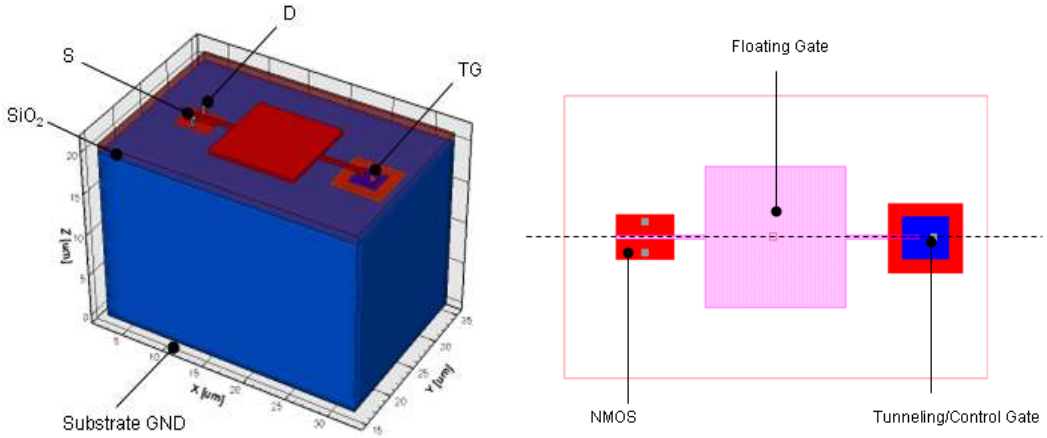


Fig.1 Layout and 3D model of the dosimeter

1.2 The Programming of the device

By applying a voltage bias to the TG contact with respect to the substrate, the transferring of charge is enabled onto the floating gate via tunnelling. In Fig. 2 the band diagram for three different biasing conditions of the device is shown, along the vertical direction through the device from the cross marked in the layout picture. At zero bias, the potential barrier provided by the thin layer (approx 7nm) of SiO_2 prevents any tunnelling of charge from the floating gate to the silicon substrate. By applying a positive voltage the bands bend downward and the potential barrier seen across the SiO_2 is lowered. A similar situation occurs when a negative voltage is applied but with the bands bent upward. Owing to the doping level, an asymmetry in the lowering of the barrier is seen, indicating that the process of tunnelling is more effective, for the same absolute value of the voltage applied, when the bias is positive. The process of tunnelling of charge across the barrier is simulated in TCAD using a direct tunnelling model that simplifies into a Fowler-Nordheim when the field in the SiO_2 reaches approximately 6MV/cm, regardless of the SiO_2 thickness. Following approximately 15 seconds of programming with the voltage V_{tg} = -10V a charge of a few fC's is predicted to be transferred onto the floating gate. A cross section of the floating gate region and the surrounding silicon SiO_2 is shown in Fig. 3, for different charge stored in the floating gate. The direction of the electric field is shown by the arrows and the different colors refer to its intensity. The initial condition, with no charge on the floating gate, shows an electric field directed from the floating gate into the SiO_2, with an intensity of up to 10kV/cm, due to the potential difference between floating gate and silicon substrate. With -4fC stored on the floating gate the electric field reverses its direction, now pointing towards the floating gate. The stored charge in the floating gate alters the SiO_2 electric field, thus enhancing or reducing the formation of the NMOS channel at the silicon and SiO_2 interface. This has the effect of shifting the threshold voltage of the NMOS transistor, in a positive or negative direction depending on the sign of the charge stored, Fig. 4.

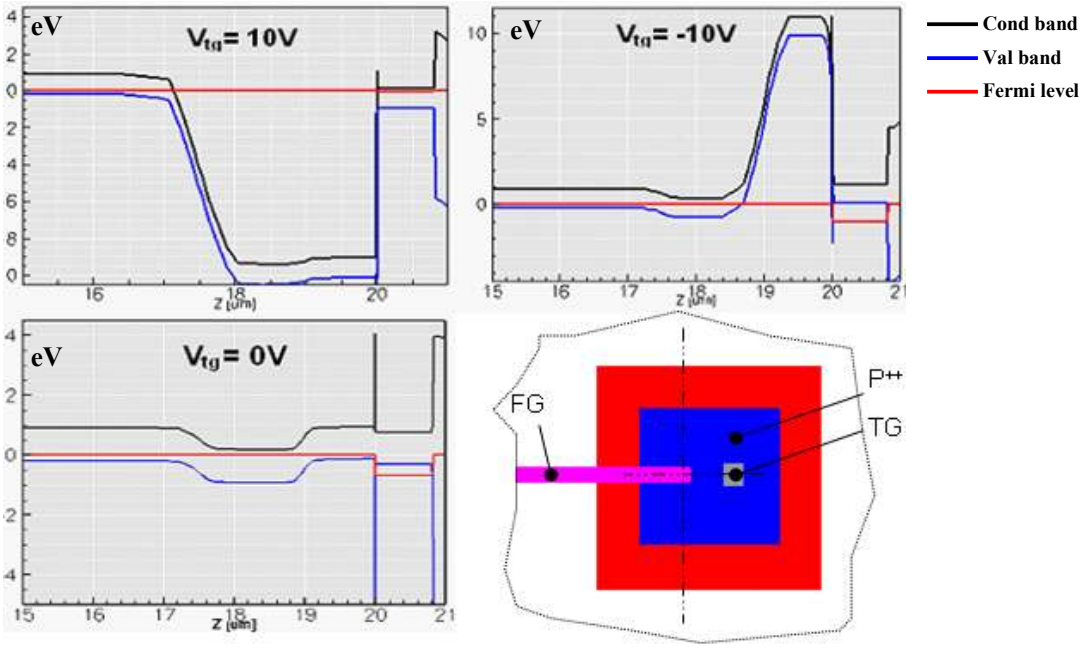


Fig.2 Band diagrams of the device

The threshold voltage of the device is here defined as the voltage V_{tg} applied to the control gate to obtain an I_{ds} = 0.3μA when V_{ds} =3V.

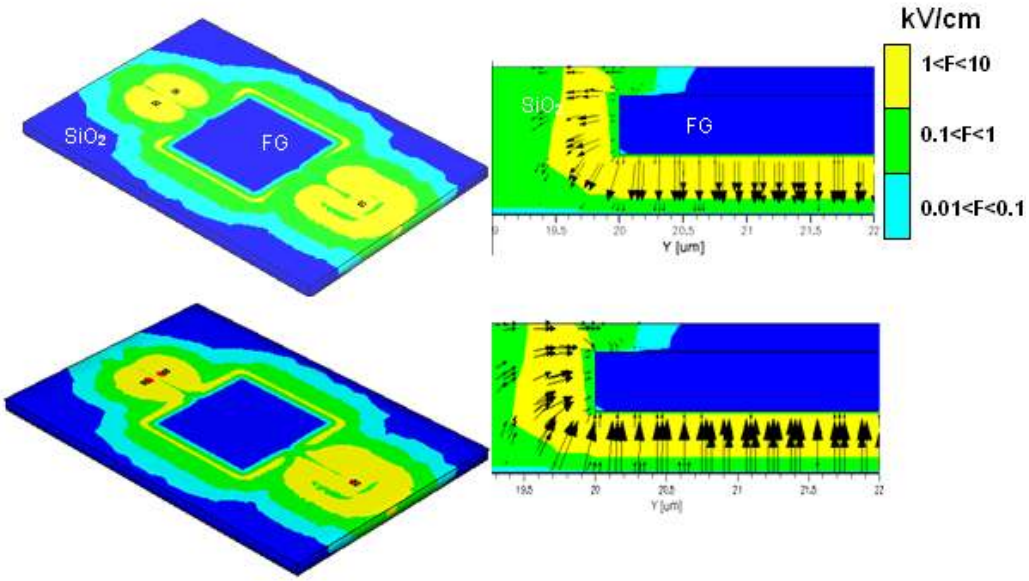


Fig.3 Floating gate electric field in SiO_2

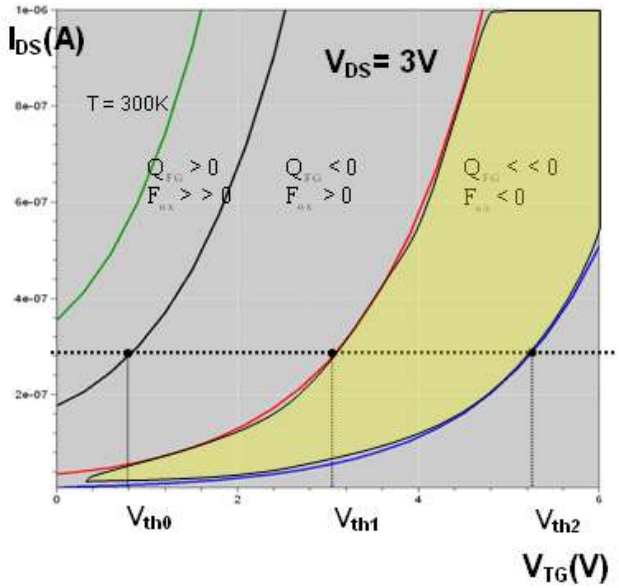


Fig.4 Threshold voltages V_{th} of the device for different values Q_{fg} of floating gate charge. The region beyond V_{th1} corresponds to a negative Q_{fg}

2.Radiation detection principle

2.1 Threshold voltage shift

As stated above, the principle of radiation detection studied here relies on the shift of the threshold voltage of the NMOS transistor stemming from the change in the potential of the floating gate. Following irradiation there are mainly three mechanisms that affect the floating gate potential. The charge stored in the floating gate that acquires enough energy from the radiation is emitted from this gate and swept to the substrate by the internal electric field, due to the stored charge and/or the bias applied, with a process similar to the EPROM erasure by UV radiation. The second effect is the migration of the radiation generated charge within the SiO_2 that surrounds the floating gate into the floating gate itself. This directly discharges the floating gate thus changing its potential. The third effect is the result of trapped positive charge either within the bulk SiO_2 or at the interfaces with SiO_2 and silicon, where the density of trap centres (E' centers) is high ([5]) due to the local lattice strains. This positive trapped charge could shield, or enhance, the electric field generated by the charge stored in the floating gate. The resulting net effect of all these phenomena is the shift in the threshold voltage of the NMOS device.

2.2 Charge generation in SiO_2

The direct floating gate discharge is the mechanism of radiation detection associated with threshold shift: the charge generated in the silicon SiO_2 by ionizing radiation migrates towards the floating gate, previously negatively charged, and neutralizes part of its charge.

To calculate the amount of charge collected by the floating gate it is necessary to estimate the amount of charge generated in the SiO_2 by ionizing radiation and the fraction of it that escapes recombination. The generated charge per unit dose of radiation (rad) and volume in the SiO_2 is estimated to be approximately 8 e^- /μm^3 and depends on the average threshold energy required to generate an electron hole pair in it. Fig. 5 shows the LET in SiO_2 for different particles. From it can be seen that for secondary Compton electrons generated in SiO_2 by gamma radiation of interest here an Onsager model is adequate to describe the recombination rate. This model gives the probability of an electron escaping recombination with its ion (fractional yield) in presence of an applied electric field and temperature ([6]). In Fig. 5 an example of plot of the fractional yield is shown for very low electric field up to those typically found in modern MOS devices structures. The initial electron - hole separation in SiO_2 is assumed to be 11nm.

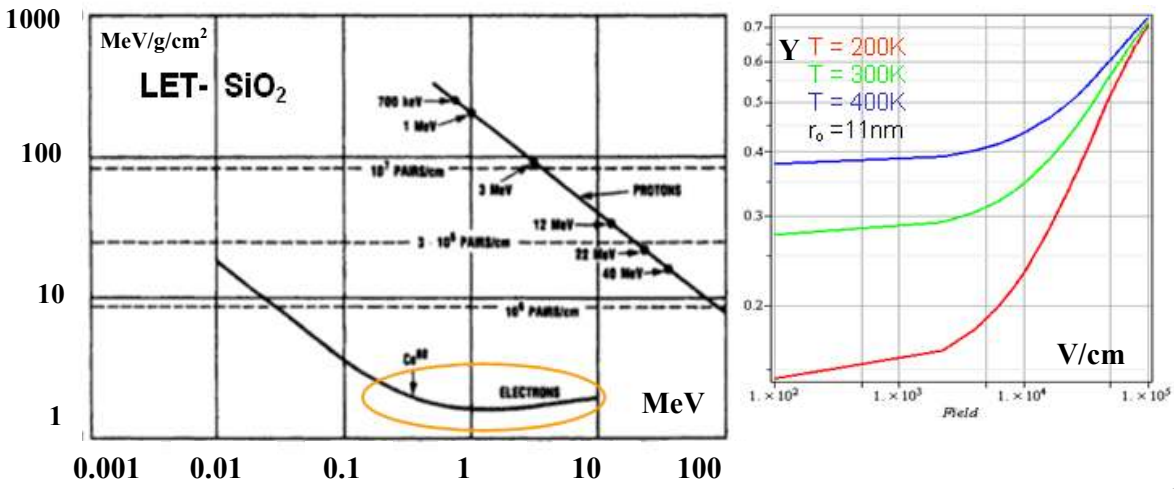


Fig.5 LET in SiO_2 and fractional yield

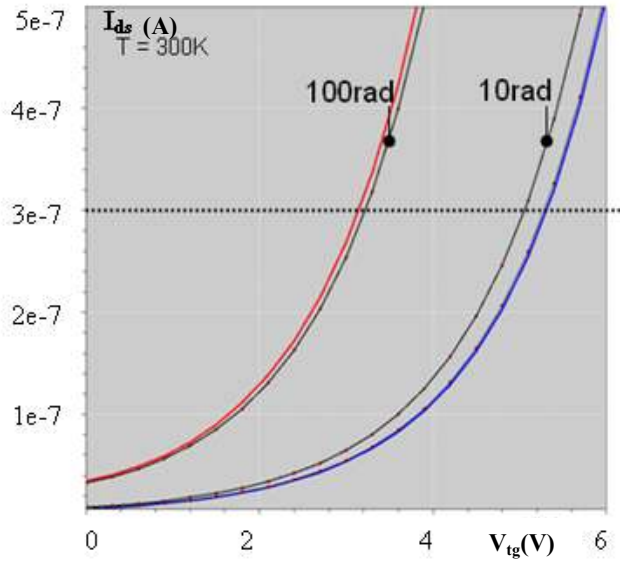
2.3 Floating Gate discharge

The procedure followed to calculate the amount of collected charge is to subdivide the regions of SiO_2 surrounding the floating gate according to their intensity of electric field, for values ranging from 100V/cm up to 10kV/cm. Then, assuming a uniform charge generation from ionizing radiation, the total charge eventually collected by the floating gate is taken to be equal to the sum of the individual fractions evading recombination in the different regions of the SiO_2, according to the values of the electric field. Once the charge collected by the floating gate has been calculated, the new value of the resulting electric field in SiO_2 is computed, to estimate the effect of the decreased sensitivity due to the floating gate discharge.

3.Simulation Results

3.1 Sensitivity to dose of radiation

The results of the simulations, shown in Fig. 6 indicate that a sensitivity of up to 26mV/rad can be achieved with the studied layout; as expected, a decrease in sensitivity is predicted at higher dose, resulting from the discharge of the floating gate which reduces the internal electric field. The total dynamic range of the device, in this case of the order of 1Gy, can be increased by increasing the size of the floating gate.



D	Sensitivity (ΔVth/rad)@ Vds=3V
0	26mV
10rad	26mV
100rad	11mV

Fig.6 Sensitivity to dose of radiation. The blue curve shows the initial $I_{ds}(V_{cg})$ of the device with charge of -4fC in the floating gate; the red curve is the $I_{ds}(V_{cg})$ when the charge in the floating gate renders the electric field in the oxide almost negligible. The black curves show the $I_{ds}(V_{cg})$ for different levels of absorbed dose of radiation. The sensitivity decreases with decreasing charge on the floating gate (i.e. moving from the blue to the red curve)

3.2 Minimum detectable dose of radiation

An estimate of the minimum detectable dose of radiation for different values of received dose can be obtained by estimating the noise of the NMOS device. The contributions of flicker noise are obtained from typical noise spectrum values measured from real devices. The thermal noise spectrum is calculated at the nominal threshold voltage as defined above. Fig.7 reports the estimated values of sensitivity and minimum detectable dose. A frequency bandwidth of 10Hz was used in the calculations. A theoretical maximum dose resolution of 38.4mrad is predicted.

D	Sensitivity (ΔVth/rad)@ Vds=3V, T = 300K)	Max resolution (rad)
0	26mV	0.0384
10rad	26mV	0.0384
100rad	11mV	0.091

Fig.7 Minimum detectable dose of radiation (resolution) for different values of dose. Only the electrical noise of the device is considered. The frequency bandwidth is 10Hz

4.Conclusions

The simulations presented here suggest that this technology is suitable for applications in radiation dosimetry. With the initially studied layout the predicted sensitivity is of the order of 10's of mrad for photon energies between 1 to 10Mev. A higher dynamic range could be achieved by changing the device size. The complete compatibility of this fabrication process with standard CMOS process suggests the use of this technology for monolithic implementations of radiation sensors and electronic readout. A natural application for this solution would be in the field of In vivo biomedical applications.

References

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