

## The Upgrade of the CMS Tracker for Super-LHC

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The CMS experiment at the Large Hadron Collider (LHC) at CERN, Geneva, is planning a major upgrade of its tracking system to adapt to an expected increase in luminosity of the accelerator by an order of magnitude to  $10^{35} \text{ cm}^{-2}\text{s}^{-1}$ , expected to be reached about ten years after start-up. The CMS tracker will have to cope with several hundred interactions per bunch crossing and fluxes of thousands of charged particles emerging from the 40 MHz collisions. This will require major developments of detector technology and R&D has begun to address the expected challenges. Among the most important are the radiation tolerance of sensors and other components, the provision and distribution of power for both electronics and sensors, the removal of increased heat loads, and the development of low power, but highly performing electronics in more advanced technologies. CMS has also identified a novel requirement, which is to provide tracker data to contribute to the first level trigger, which must maintain the 100 kHz rate for compatibility with existing sub-detector systems while increasing the trigger decision latency by only a factor of two. The motivations for the upgrade, recent progress in several aspects of the R&D as well as the current status of designs of a new tracker is described.

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## 1. The Super-LHC

The Super-LHC (SLHC) is a potential luminosity upgrade of the LHC that involves changes to the LHC injector chain and the interaction regions [1]. The luminosity will essentially be increased in two steps: from  $10^{34} \text{ cm}^{-2}\text{s}^{-1}$  to  $2 - 3 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$  at phase-1, and to  $10^{35} \text{ cm}^{-2}\text{s}^{-1}$  at phase-2. Phase-1 is expected to be realized in about five years from the start-up of the LHC. This phase has been approved and civil engineering for the new Linac4, the replacement of Linac2, has started. Phase-2 is much more complex and includes the replacement of the PS Booster by a new Linac (LPSPL), the replacement of the PS by the larger PS2, as well as enhancements to the SPS. Approval for phase-2 is expected not before 2011.

## 2. The Tracker Upgrade

The CMS tracker [2] is composed of a silicon pixel detector in the center, and a silicon micro-strip tracker surrounding it. The whole tracker is located inside the 3.8 T solenoidal field of the CMS magnet. The pixel detector has been designed to withstand two years at LHC design luminosity. It can be extracted and exchanged via a dedicated rail system during a standard shutdown. The strip tracker has been designed to survive ten years at LHC design luminosity; assuming an integrated luminosity of  $500 \text{ fb}^{-1}$  this corresponds for the inner central part (22 cm radius, pseudorapidity  $\eta = 0$ ) to a 1 MeV neutron equivalent fluence of  $1.6 \cdot 10^{14} \text{ cm}^{-2}$  and an absorbed dose of 70 kGy.

While most sub-detectors of CMS are expected to survive the conditions at the SLHC and to continue to perform well, with upgrades concentrating on trigger electronics or data acquisition, the tracker represents the most notable exception. The radiation level expected at phase-2 exceeds by far the specifications quoted above: for an integrated luminosity of  $3000 \text{ fb}^{-1}$  the fluence in the central part of the detector at a radius of 4 (22) cm is expected to reach  $19 (1) \cdot 10^{15} \text{ cm}^{-2}$ , while the dose increases to 5 (0.4) MGy. Even higher fluences are expected at larger  $z$  values, where  $z$  is measured along the beam pipe. The radiation-hardness of silicon sensors and readout electronics is therefore a major concern, and R&D has started to identify suitable sensor technologies. The increase of the number of pile-up events per bunch-crossing from 20 at the LHC to 300-400 at the SLHC is another worry, as the number of particles inside the tracker consequently increases from about 1 000 up to 20 000 per bunch-crossing. To keep the detector occupancy at the level of 1 %, the granularity of the strip tracker must be increased. The biggest challenge stems however from the requirement to maintain the first level trigger rate at its current (design) value of 100 kHz, for compatibility with existing sub-detector systems. This requires the use of tracker data in the Level-1 (L1) trigger, and consequently a completely new tracker concept.

The requirements on the tracker performance from physics will only be known once LHC operation has started and first results are available. It is however obvious that the tracker performance must not deteriorate but must rather be preserved or improved, in order to be able to fully exploit the potential offered by the SLHC. In particular the tracking and vertexing performance must be maintained, even though the environment will be more challenging. The expected intrinsic spatial and momentum resolutions are excellent and seem adequate for the SLHC. However, the performance is degraded by the rather large amount of material: 0.4 radiation lengths at  $\eta = 0$  and up to 1.8

radiation lengths at  $\eta \approx 1.5$  [2], in the transition region between strip tracker barrel and end caps. The strong desire to reduce the material inside the tracker volume is thus a major driving force for the new tracker design.

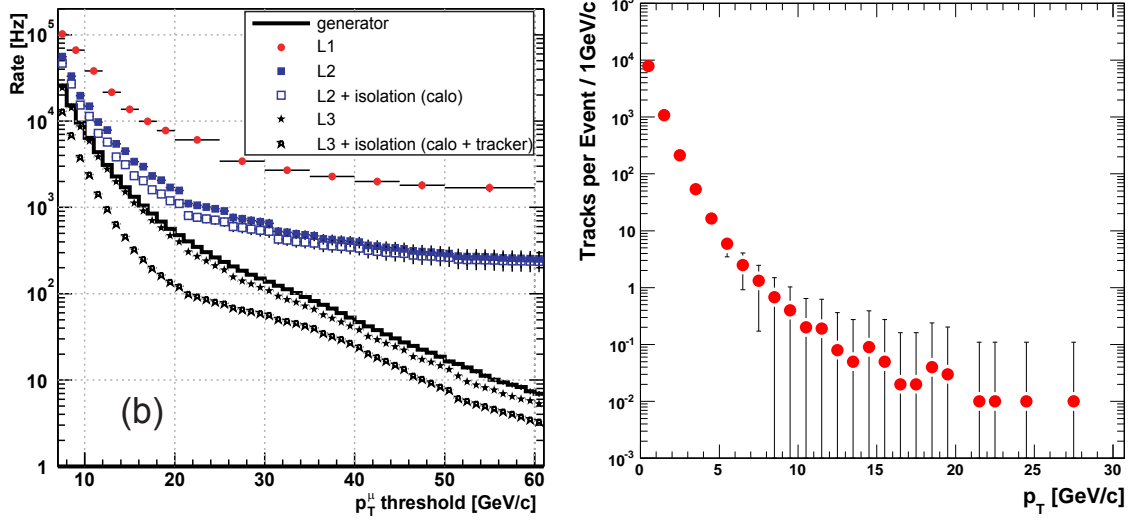
The upgrade of the pixel detector for phase-1 is discussed in Sect. 2.1. The subsequent sections concentrate on the upgrade of the outer tracker for phase-2.

## 2.1 The Pixel Upgrade at Phase-1

The main focus within the CMS pixel project is currently on phase-1, as this is when the pixel detector will have to be replaced for the first time. The current pixel detector is composed of a barrel part with three layers, and two end caps with two disks each. The detector comprises 66 million pixels with a cell size of  $100 \mu\text{m}$  ( $r\phi$ )  $\times$   $150 \mu\text{m}$  ( $z$ ), corresponding to a silicon area of about  $1 \text{ m}^2$ . The sensor technology is  $n^+$ -in- $n$ . In view of the schedule, radical changes are currently not foreseen for the phase-1 pixel upgrade. However, a number of technological improvements feasible on the given timescale have been identified and are pursued. These include a new lightweight mechanical support structure plus various other measures to reduce material; to move from the current monophasic cooling system based on the coolant  $\text{C}_6\text{F}_{14}$  to an evaporative  $\text{CO}_2$  cooling system; the use of a powering scheme based on DC-DC conversion; the change from an analogue-coded digital readout running at 40 MHz to a binary-coded sparsified serial readout at 160 MBit/s (320 MBit/s after multiplexing); and changes to the periphery in the PSI46 readout chip such as increase of buffer depth to reduce the deadtime. Novel powering and readout schemes are required because the upgraded detector will be composed of four barrel layers (at 3.9, 6.8, 10.9, 16.0 cm radius) and three disks per side, with a corresponding growth in the number of readout chips from 15 840 to 30 208, while the services cannot be exchanged. More details on the pixel upgrade can be found in [3].

## 2.2 Track Trigger Concepts

Currently in CMS the tracker information is used only at the High Level Trigger (HLT). In Fig. 1, left, simulated muon trigger rates at LHC are shown as a function of the  $p_T$  trigger threshold, for various trigger levels. While the L1 muon trigger rate saturates around 2 kHz (corresponding to 20 kHz at phase-2) irrespective of the applied  $p_T$  threshold, the use of tracker information in the second stage of the HLT (“L3”) helps to reduce the trigger rate by at least an order of magnitude [4]. The use of tracker data at L1 is therefore believed to be the only way to keep the L1 trigger rate at 100 kHz. Tracker data could be used to improve the muon  $p_T$  resolution, to facilitate electron matching, for the application of isolation criteria, and for primary vertex identification. However, the readout of the full tracker within the future trigger latency of  $6.4 \mu\text{s}$  is considered impossible. To reduce the data volume it has therefore been proposed to identify high- $p_T$  tracks, where “high” means above 1-3 GeV/ $c$ , in the detector, and use only these tracks for the trigger decision. Figure 1, right, shows the simulated  $p_T$  spectrum of tracks at 25 cm radius, which falls off rapidly [5]. In this way a reduction of the data volume by one order of magnitude or more seems feasible. In the following two different proposals for the identification of high-momentum tracks are presented. A decision on the track trigger concept has not yet been taken.



**Figure 1:** Left: single-muon trigger rates as a function of the  $p_T$  threshold at  $10^{34}\text{cm}^{-2}\text{s}^{-1}$  [4], for Level-1, Level-2 (first step in HLT, no tracker information), and Level-3 (second step in HLT, tracker information used), with and without isolation applied at Levels 2 and 3. The rate generated in the simulation is also shown. Right:  $p_T$  spectrum of the average number of tracks per event reaching a layer 25 cm from the beam axis and with coverage  $|\eta| < 2.5$ , for an average pile-up of 400 minimum bias interactions per event [5].

### 2.2.1 The Stacked Layers Approach

The idea behind this proposal is to compare hit patterns in closely spaced (“stacked”) detection layers, as tracks with large  $p_T$  are less bent by the magnetic field than low- $p_T$  tracks, and therefore these two track samples produce different hit patterns [6]. Pixelated detectors are required in this approach, with a pitch of the order of  $100\mu\text{m}$  in the bending plane. The distance between the two sensitive layers in one stack is of the order of 1 mm. The resulting 2-hit track pieces (“stubs”) are forwarded to the L1 trigger. Several stacks could be combined to reconstruct “tracklets”. The concept is compatible with thin sensors, preferred for their low mass, and provides information in the  $z$ -direction as well, as required for primary vertex identification. The correlation logic that compares the hit positions within one stack must take into account many effects, such as the Lorentz angle and the variation of the distance in  $z$  between the hits in the two layers with the track polar angle. The power consumption of the complex fast digital electronics will be considerable. Cost is another concern, since a potentially large area will have to be covered with pixelated sensors.

### 2.2.2 The Cluster Width Approach

In the second proposal the discrimination between low and high-momentum tracks is based on the cluster width in a single sensor layer [7], which varies between low and high- $p_T$  tracks due to the bending in the magnetic field. The hit information within a  $\phi$ -slice of the detector is then brought out via high-bandwidth optical links and reconstructed off-detector in powerful FPGAs by comparison with templates. The reconstructed high- $p_T$  tracks are then used in the L1 trigger. This method works with classical strip modules with a pitch of the order of  $100\mu\text{m}$ , which is beneficial under the aspects of power consumption, material and cost. As the discrimination is based on one

sensor layer only, no correlation between layers is required - a significant simplification. On the other hand the method is only efficient above a certain sensor thickness  $d$  and radial distance  $r$  from the beam pipe, as the cluster width is proportional to  $B \cdot r \cdot d / p_T$ . The method will be less efficient in an end cap geometry. The data volume reduction factor is rather sensitive to the background from secondary interactions, which is not well known at this point. In the cluster width approach the provision of precise  $z$  information is not foreseen, thus the vertex identification is less exclusive.

### 2.3 Strawmen for the Tracker Layout

The current strip tracker with its active area of  $200 \text{ m}^2$  features a classical design with a central barrel part and two end caps. A redundant layout has been chosen, with ten active layers in the barrel, four of them being double-sided to provide spatial information along the strip direction. The strip length in the 15 148 modules varies between 8.5 cm in the inner ring of the end caps and 20.2 cm in the outermost ring, and the (mean in case of wedge-shaped strips) pitch varies between  $80 \mu\text{m}$  and  $184 \mu\text{m}$ .

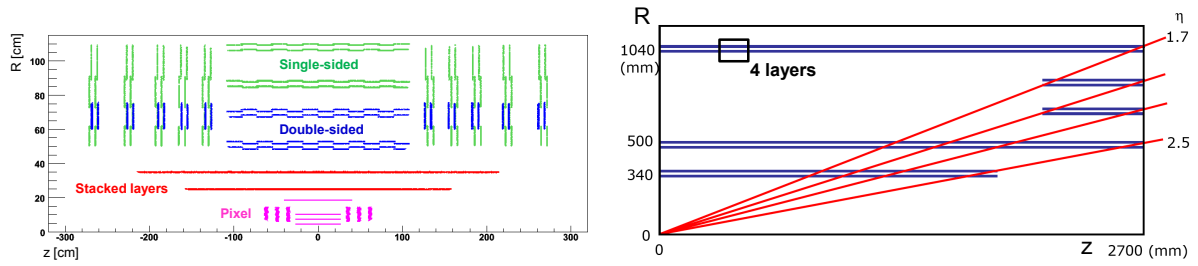
The future design is currently under study and simulations are used to understand the consequences of certain choices. Since the geometry of the current tracker layout is fixed in the simulation, a huge, now completed, task has been undertaken to modify the software accordingly. Various layouts have been proposed. Two basic “strawman layouts” using the stacked layers approach have been implemented into the software and are being studied and compared. In the following these two layouts will be described. A strawman based on the cluster width approach is under development.

#### 2.3.1 The Hybrid Layout

The hybrid layout is characterized by the combination of a minimalistic trigger configuration, consisting of two stacked layers at 25 and 35 cm radius with a layer separation within a stack of about 2 mm, and a classical 4-layer outer strip tracker (Fig. 2, left). The strip length in the tracking layers amounts to 2.5 cm in the inner part and 5.0 cm further outside. The outer tracker would have a sensitive area of about  $85 \text{ m}^2$  and a FE power consumption of the order of 10 kW, assuming a power consumption of 0.5 mW/strip (Sect. 2.4.1). The trigger layers would use pixels with a cell size of  $100 \mu\text{m}$  ( $r\phi$ )  $\times$  2.5 mm. Although the sensitive area of the trigger layers would “only” be  $27 \text{ m}^2$ , the FE power consumption would be larger than that of the readout part, namely 12 kW, assuming a power consumption of 0.1 mW/pixel. The link power is not included in these numbers.

#### 2.3.2 The Long Barrel Double-Stack Layout

In contrast to the Hybrid layout the Long Barrel Double-Stack layout avoids end caps. It consists of three full layers of double-stacks, plus two short layers to improve the acceptance at high  $\eta$  (Fig. 2, right). One such layer corresponds to two stacked layers or four sensor layers; in total there are therefore 12 sensor planes at  $\eta = 0$  in this layout. All layers contribute to the trigger decision. The intra- and inter-stack distances would be 1 mm and 4 cm, respectively. Modules are arranged on substructures called beams that run along the  $z$  direction. Neighbouring beams would be arranged in an “alternating” geometry at larger and smaller radius. A pixel cell size of  $100 \mu\text{m}$  ( $r\phi$ )  $\times$  1.0 mm ( $z$ ) has been proposed. With a sensitive area of  $300 \text{ m}^2$ , the band width requirements, power consumption (estimates indicate a FE power consumption of the order of 100 kW) and also cost are a concern.



**Figure 2:** Left:  $rz$ -view of one half of the “Hybrid” tracker layout. Right:  $rz$ -view of one quarter of the “Long Barrel Double-Stack” tracker layout. The pixel detector is shown only in the left figure.

### 2.3.3 Simulation Results for a Stacked Layer

A single stacked layer with untilted sensors at 25 cm radius has been simulated and the performance has been studied for sensor separations of 0.5, 1.0, 1.5 and 2.0 mm, using a sample of 10 000 di-muon events [5]. The search window for correlations has been fixed to 3 pixels in  $\phi$  and 2 (3) pixels in  $z$  for 0.5 mm (1.0-2.0 mm) separation. For a fixed search window the sensor separation effectively defines the  $p_T$  cut of the trigger. For 0.5, 1.0, 1.5 and 2.0 mm, respectively, the efficiency for tracks with a  $p_T > 2$  GeV/c amounts to 99.4, 99.2, 98.6, 97.1%; the fraction of fakes is 2.7, 6.6, 16.3 and 23.3%; and the important reduction factor is found to be 9.2, 22.0, 37.0, and 54.4. A sensor separation of 1 mm provides thus a significant reduction factor with a high efficiency and an acceptable fake rate.

## 2.4 Examples of R&D Projects for the Strip Tracker at Phase-2

### 2.4.1 Outer Tracker Module and the CMS Binary Chip

An “Outer Tracker Module” has been proposed for the outer layers of the Hybrid layout. The sensitive area is about 10 cm x 10 cm, composed of four 2.5 cm long strips in the inner layers and two 5.0 cm long strips further outside. The FE-hybrid (two hybrids for the short strip modules) would be glued directly onto the sensor. Each FE-hybrid carries six 2 x 128 channel readout ASICs, which are wire-bonded to the silicon strips. The strip pitch is 120  $\mu\text{m}$ . The pitch adapter is assumed to be integrated into the sensor, to reduce material. The sensor would mechanically be supported by strips of Carbon Fiber or Thermal Pyrolytic Graphite, which run beneath the backplane along the direction of the hybrid. The cooling circuit would be routed along the sides of the module (perpendicular to the hybrid), and cooling blocks are used for the thermal contact to the cooling pipe. The thermal and mechanical properties of the described module and several variations of it are currently studied with Finite Element simulations.

The successor of the APV25, the CMS Binary Chip (CBC) [8], has been proposed as the readout ASIC for this module. This chip in 130 nm CMOS technology features a binary unsparsified readout architecture, chosen for its low power consumption, synchronous readout and constant data volume. The simulated power per channel is 0.5 mW for a sensor capacitance of 5 pF. The amplifier with a peaking time of 20 ns is followed by the comparator, a digital pipeline and a digital multiplexer. The design is compatible with both signal polarities and DC and AC coupling. Challenges are to achieve robustness against external noise, the loss of diagnostic possibilities with respect to

an analogue readout, and the binary position resolution. A first prototype is expected to be available in Spring 2010.

### 2.4.2 Track Trigger Modules

Several module designs have been proposed. Two examples, representing the extremes of the spectrum in terms of complexity, are sketched here.

The “ $p_T$ -module” [9] aims for the  $p_T$  layers in the Hybrid layout and focuses on currently available technologies and the potential for easy prototyping. The module consists of two stacked sensors with 2.56 cm x 8 cm area each, with a pixel cell size of 100  $\mu\text{m}$  x 2.5 mm. Each sensor consists of 32 sub-units of 12.8 mm x 5.0 mm, and each sub-unit is being read out by one 2 x 128 channel ASIC, which is connected to the sensor by coarse pitch bump-bonding or even wire-bonds. The hits (0.5 % occupancy is assumed) are transferred to the chip edge with a 10 bit bus at 40 MHz. The hit patterns and addresses of the two stacked sensors are stored and compared in dedicated chips, which could be part of the readout ASICs. The connection between the layers would be realized by a dedicated “interconnect chip”. The FE-power consumption has been estimated to be 100  $\mu\text{W}$  per pixel, and twice as much once the link power is included.

The “Vertically Integrated Hybrid Module” [10] is based on 3D-interconnection technology and targets the Long Barrel Double Stack layout. The sensor size is 85 cm<sup>2</sup>, with a pixel cell size of approximately 100  $\mu\text{m}$  x 1 mm in the lower sensor of the stack and 100  $\mu\text{m}$  x a few millimeters in the upper sensor. Either the analogue data or digital data of the upper layer are transferred to the lower layer through vias in a ca. 1 mm thick “interposer” layer, whose via density drives the strip length in the upper sensor. Only the lower module layer is equipped with the master read-out circuit that analyzes the correlations. The thinned chips feature 3D-interconnection technology with through-silicon vias. The power and band width requirements have to be assessed.

### 2.4.3 Silicon Sensor R&D

CMS is carrying out an R&D project with HPK [11] for the evaluation of the future pixel and strip sensor technologies. The wafer layout includes multi-geometry pixel and strip areas and various test structures. The phase space to be explored is huge: float-zone (with 100, 200 and 300  $\mu\text{m}$  thickness), magnetic Czochralski (200  $\mu\text{m}$  thickness) and epitaxial silicon (75 and 100  $\mu\text{m}$  thickness) in p-in-n and n-in-p versions, with various pitches, strip widths and biasing schemes. P-spray and p-stop isolation techniques will be compared where applicable, and the integration of pitch adapters (Sect. 2.4.1) will be studied. The sensors, expected to be available early 2010, will have to be characterized before and after irradiation with various fluences.

### 2.4.4 Power and Cooling

The routing and installation of the tracker services (cooling pipes, optical ribbons, power cables) has been one of the biggest engineering challenges for the current tracker, and their exchange or enhancement is not considered feasible. This poses a major constraint for the upgrade.

It is likely that the future outer tracker will need more power than the current 35 kW, at a higher current. To limit resistive losses in the long (50 m) supply cables and to allow for thinner conductors inside the tracker volume a novel powering scheme based on the DC-DC conversion technique is foreseen. The idea is to bring the power into the detector at a higher voltage but a lower current,

and to use a DC-DC buck converter close to each silicon module to convert the input voltage to the operation voltage needed by the module. These buck converters are switching devices with air-core inductors and thus both conductive and radiative noise sources by design. The R&D within CMS is aiming for a better understanding and control of the noise effects, and the minimization of the converter dimensions and its material budget [12].

The current monophasic cooling system with  $C_6F_{14}$  as coolant will probably be replaced by a two-phase  $CO_2$  system. Due to the high latent heat of  $CO_2$  thin pipes with a diameter of the order of 1.5 mm are sufficient to remove the heat. With coolant temperatures as low as  $-35^\circ C$  being feasible, the effect of thermal runaway can probably be avoided.

A rather significant reduction of the material budget is expected from these changes.

## 2.5 Summary

For SLHC phase-1 CMS aims for the exchange of its pixel detector with a very similar, but larger and improved detector (less material, faster readout).

The whole tracker will have to be replaced for phase-2. The detector design is driven by the requirement to provide data to the L1 trigger, and the goal to reduce the material as much as reasonably possible. The current status of several selected R&D projects has been presented. The biggest challenge at this point is the definition of the tracker layout. Several suggestions exist but must be explored further until convergence can be reached. The collaboration is aiming for a common tracker strawman in 2010.

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