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The SuperB Silicon Vertex Tracker

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In the current design of the high luminosity SuperB asymmetric e^+-e^- collider, the center of mass boost is reduced with respect to BaBar and to efficiently perform the time-dependent measurements an improved vertex resolution is required. A vertex tracker based on the layout of the BaBar Silicon Vertex Tracker (SVT) with an additional innermost layer (Layer0) is a design that achieves such a tracking resolution, provided that the extra layer is placed at radius of 1.5 cm from the interaction point, its thickness is less than 1% X_0 and it is able to withstand a background rate of several MHz/cm^2. The different options for the Layer0 are reviewed, starting from the most technologically mature solution, a high resistivity short strip detector, describing then a small-pitch hybrid pixel detector and finally presenting the most challenging proposal, based on CMOS MAPS.

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1. Introduction

After the successful ten-year experience of the SLAC and KEK B-factories, the challenge of undertaking a new generation of e^+-e^- colliders is strongly motivated by the search for effects of New Physics (NP) in the decay of heavy quarks and leptons [1].
The high luminosity is the crucial ingredient in order to reach the sensitivity needed to set constraints on the models describing possible manifestations of NP. To open a window on the NP, an integrated luminosity of at least 50-100 ab^{-1} must be collected with an increase of two orders of magnitude with respect to the existing B-factories.
The physics program of a Super B-factory is focused on the search for the effects of physics beyond the Standard Model in processes where loop diagrams are involved. Potentially large effects might show up on rates of rare decays, time dependent asymmetries and lepton flavour violation. These processes are sensitive to large NP energy scale as well as to phases and sizes of NP coupling constants. Furthermore, it is worth reporting the unique feature of running with polarized e^- beam, that can be fully exploited in the $\tau^+ \tau^-$ channels. What has been briefly reviewed certainly asserts the complementarity and synergy of the SuperB program with the LHC one [2].
So far only the so called "Italian approach" is currently under investigation to build a new accelerator able to deliver a luminosity greater than $10^{36}cm^{-2}s^{-1}$. Instead of relying on brute force (i.e. high beam currents, requiring high radio-frequency power) the new concept is based on moderate beam currents, very small emittance (similar to the ILC damping ring design), small betatron vertical amplitude β_y^* at the interaction point. In addition, the crab-waist technique, recently tested at DAΦNE, allows a further luminosity gain and removes dangerous synchrotron-betatron resonances. The machine-related background is limited to moderate levels by adopting beam currents similar to the present B-Factories. The machine design sets a severe constraint on the beam-energy asymmetry. The preferred choice is 7 GeV electron colliding with 4 GeV positron beams, forcing $\beta\gamma$ to a value of 0.28 (it was 0.56 in BaBar). The reduced center of mass boost of the SuperB machine requires to improve the vertex resolution for optimal time-dependent measurements.
Simulation studies indicate as a viable concept a vertex detector based on the BABAR Silicon Vertex Tracker (SVT) layout with the addition of an innermost layer (Layer0). This paper reviews several technological options for the Layer0 design sorted in term of increasing complexity: a double-sided silicon detector with small strips, called striplets, tilted with respect to the detector's edge; a highly segmented hybrid pixel detector; the CMOS Monolithic Active Pixels (MAPS), a technology which is very promising but still needs an extensive R&D.

2. Requirements and Vertex Detector Conceptual Design

Fast simulation studies have been carried out to optimize the design of a vertex detector (SVT in the following) suitable for application at the SuperB collider. As a starting point it has been assumed the layout of the current 5-layer BaBar silicon vertex detector [3], properly extended in angular coverage down to 300 mrad in both forward and backward directions, and equipped with a Layer0 placed close to the beam-pipe that has a radius of 1 cm and a thickness of about 0.45% X_0. The resolution in the proper time difference between the two B mesons is the parameter driving the precision of the CP time-dependent measurements and it should not exceed the value obtained by

the BaBar experiment. This quantity is shown in Fig. 1 for the decay channel $B \to \pi^+\pi^-$ with the nominal SuperB boost for three different Layer0 radii, as a function of the total Layer0 material. The resolution on the single hit (z and ϕ) was set to 10μm. These simulations indicate the need of a Layer0 at radius of about 1.5 cm, very close to the reduced beam-pipe, with a material budget less than 1% X_0.

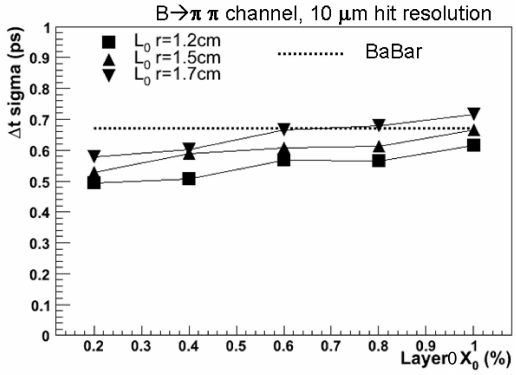

Figure 1: Resolution on the proper time difference of the two B mesons. As a reference the BaBar resolution is shown with a dashed line.

The machine related background has a strong impact on the whole experiment and adds also severe requirements on the Layer0 design. To correctly estimate the rates of the different sources of background a full Geant4 simulation of the detector and beamline has been used[1]. The background expected in the layers of the SuperB SVT placed at radius greater than 3 cm is similar to the background seen by the present BaBar SVT [3], because it is dominated by effects that scale with beam currents. The background at the Layer0 radius is instead dominated by effects that depend on the luminosity (i.e. irreducible), in particular by the process called $e^+ e^-$ pair production, being radiative Bhabha events several order of magnitudes smaller. The pair-produced leptons have energy belonging to the MeV range. The 1.5 Tesla solenoidal magnetic field is effective in bending these low transverse momentum tracks, suppressing the rate of hits on the Layer0.
According to these simulations, the background hit rate shows a strong radial dependence and for a Layer0 at 1.5 cm it is at the level of 20 MHz/cm^2. The equivalent fluence corresponds to 3.7 10^{12} n/cm^2/year and the dose rate to withstand is 3 Mrad/year. It seems adequate working with a safety factor of five on this background estimate.

3. Layer0 Technological Options

The preparatory phase of the SuperB experiment is going to produce by the end of 2010 the Technical Design Report (TDR). Several technological options are under study to build the Layer0: the lower level of maturity corresponds to the higher complexity and expected performance. In the following we describe modules based on high resistivity sensors with short strips, hybrid pixels, thin pixels based on CMOS Monolithic Active Pixel Sensors (MAPS).

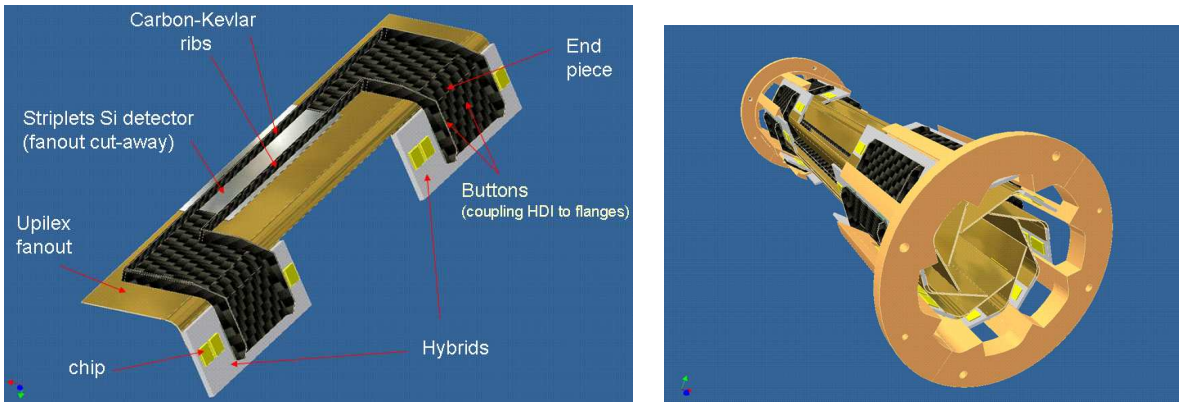

Figure 2: Left: schematic drawing of a Layer0 striplets module. Right: view of the whole Layer0 on the flanges with the eight striplets modules.

3.1 Striplets

A high resistivity double sided silicon detector 200 μm thick with short strips(striplets) read out by the FSSR2 [4] front-end chip has been characterized during the SLIM5 test beam [5]. Though this option is less robust against background occupancy with respect to pixel solutions, we believe that to produce the final Layer0 modules with this technology would require only moderate R&D effort.
A limited modification on the design of the analog front end of the candidate read-out chip is needed, to allow reading out signal on both sides of the sensors and to get a higher signal/noise ratio in case of its use also for the external layers. Furthermore, some electrical and mechanical issues must be solved: due to the large number of channels, several fanout layers are required and hybrid circuits hosting many chips must be properly designed (see Fig. 2). But as the technology these detectors rely on is firmly established, it is still worth considering a Layer0 based on striplets modules as a backup solution.

3.2 Baseline: Hybrid Pixels

The maturity of the hybrid pixels technology has been stated with the construction of all the tracking detectors for the LHC experiments. We are considering hybrid pixels as the baseline option for Layer0 in the TDR, even if we know that it still requires some R&D to demonstrate the possibility of the reduction in the front-end pitch (down to 50x50 μm^2) and in the total material budget (less than 1% X_0), needed to meet the requirements.
Our activity on the development of these new hybrid pixels already yielded the design of a first prototype front-end chip with 4000 pixels that has been submitted in October 2009 with the ST Microelectronics 130 nm technology. Also the layout of the pixel sensor matrix has been completed and the production at FBK-IRST of a batch of high resistivity n-on-n, p-spray isolated pixel matrix has started on 200 μm thick silicon wafers.
The read-out and sensor chips will be connected by bump-bonding and a test is planned in Autumn 2010 for their characterization with beam.
The 32x128 cell readout chip adopts a shaperless front-end. It has been designed to have a gain of

50 mV/fC, an ENC of 150 e- with a sensor capacitance of 100 fF (200 e- with 200 fF), a threshold dispersion of 350 e- and a recovery time linear with the signal amplitude.
Its fast readout architecture has been previously developed by the SLIM5 Collaboration [6] for CMOS Deep NWell MAPS [7],[8]: the data-push architecture features data sparsification on pixel and timestamp information for the hits. This readout has been recently optimized for the target Layer0 rate of 100 MHz/cm^2 with promising results: VHDL simulation of a full size matrix (1.3 cm^2) gives hit efficiency above 98% operating the matrix with a 60 MHz readout clock [9].

3.3 CMOS MAPS R & D

The CMOS MAPS are potentially very thin detectors, having the sensor and the readout incorporated in a single CMOS layer, only a few tenth of microns thick.
An extensive R&D on this technology has been carried out in the last few years by the SLIM5 Collaboration. As the readout speed is another relevant aspect for application in the SuperB Layer0, we proposed a new design approach to CMOS MAPS [7] which for the first time made it possible to build a thin pixel matrix featuring a sparsified readout with timestamp information for the hits [8]. In this new design the deep N-well (DNW) of a triple well commercial CMOS process is used as charge collecting electrode and is extended to cover a large fraction of the elementary cell.
The full signal processing chain implemented at the pixel level (charge preamplifier, shaper, discriminator and latch) is partly realized in the p-well physically overlapped with the area of the sensitive element, allowing the development a complex in-pixel logic with functionalities similar to the hybrid pixels.
Several prototype chips (the "APSEL" series [7]) have been realized in the ST Microelectronics-130 nm triple well technology.
The APSEL4D chip, a 4k pixel matrix with the new DNW cell and the sparsified readout has been characterized during the SLIM5 test beam showing encouraging results [5]. Hit efficiency of 92% has been measured, a value compatible with the present sensor layout that is designed with a fill factor (i.e. the ratio of the electrode over the total n-well area) of about 90%.
Even if the response to charged particles has proved that the proposed approach is very promising for the realization of a thin pixel detector, it is true that several issues still need to be solved before building a working detector with this technology.
Some R&D is required to assess the scalability to larger matrix size. Furthermore the radiation hardness of the technology is under evaluation for the TDR preparation. Test structure have been exposed to ^{60}Co γ-ray up to 10 Mrad integrated dose, with sensors biased during irradiation as in real application. After the 100^o/168h annealing cycle we recorded an increase of roughly 30% on the ENC, while the effect is negligible on the charge sensitivity.
Vertical integration technology [10] offers the possibility of further material reduction and improved performance. In the summer 2009 DNW MAPS with the two analog/digital tiers have been submitted for a Chartered/Tezzaron 130 nm production run and the results on these devices are expected at the beginning on 2010. This first submission of vertically integrated DNW MAPS includes a 3D version of a 8x32 MAPS matrix with the same sparsified readout implemented in the APSEL4D chip.

3.4 Pixel Module: Cooling, Mechanics & Integration

It is well known that the mechanical support and the cooling structure always add important contribution to the total material budget of a pixel module. On the other hand, the minimization of the material is mandatory if we want to limit the detrimental effect on the resolution due to the multiple scattering.
The pixel module support structure needs to include a cooling system able to evacuate the power (about 2 W/cm^2) dissipated by the front-end electronics in the active area.
The module will adopt a light carbon fiber support with integrated micro-channels for the liquid coolant, with a total thickness below 0.3 % X_0.
Prototypes exploiting this cooling technique have been realized and experimentally characterized, indicating that the cooling system based on microchannels is a solution to the thermal and structural problem of the Layer0 [11]. To connect the front-end chips in the active area to the hybrid circuit (HDI [1]) in the periphery of the module, a light multilayer bus is under development (Al/kapton based with total material budget of about 0.2 % X_0), with power/signal inputs and high trace density for high data speed (about 160 MHz).
To cope with the high background rate present where the Layer0 is located, radiation-hard fast links will be adopted to connect the pixel module and the DAQ system located outside the detector.
Common to all the Layer0 options, the HDI will be designed to carry several IC components: buffers, fast serializers, drivers and a custom IC to implement a glue logic. The components should be radiation hard (several Mrad/yr).
The link between the Layer0 modules and the DAQ boards is currently based on a mixed solution. A fast copper link (about 3 Gbit/s) is foreseen between the HDI and an intermediate transition board, positioned in an area of moderate radiation levels, while a fast optical link will be used from this transition board to the DAQ system. For the preparation of the TDR the various components that are under development will be subject to several tests. The various pixel module interfaces will be characterized in a test-stand with PCB evaluation boards based on FPGA.
Adding the material of the various pixel module components (sensor and front-end, support, cooling and the multilayer bus) for the Layer0 module based on hybrid pixel the total thickness is about 1% X_0.
A pixel module made of two layers of CMOS Deep-N well MAPS chips sandwiching a single carbon fiber structure with micro-channels, obtains similar material budget.
A schematic picture of the Layer0 with its 8 modules wrapped around the beam pipe in a pinwheel geometry is shown in Fig. 3.

4. Conclusion

The design of Silicon Vertex Tracker for the SuperB detector is based on the 5-layer BaBar SVT with an additional innermost Layer0 very close to the shrinked (1.0 cm radius) beam-pipe cylinder.
The design of this extra layer is really challenging for several reasons: the high level of background (rate of several MHz/cm^2) imposes high granularity, a fast readout and radiation hardness, and a low material budget is required to limit the effect on the resolution due to the multiple scattering.

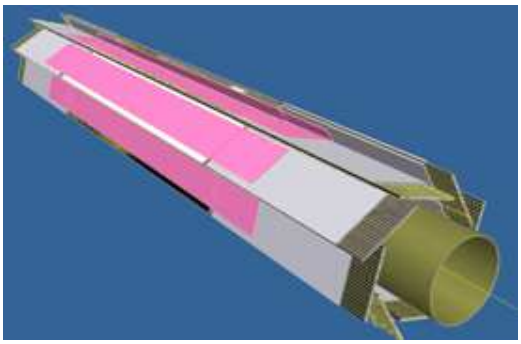

Figure 3: Schematic drawing of the octagonal Layer0 mounted in a pinwheel geometry around the beam pipe.

Several technologies are currently under study, striplets, hybrid pixel or CMOS MAPS. The extensive R&D activities must converge to a working design of the module that should be ready for the Technical Design Report of the project expected by end of 2010.

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