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Time-Resolved Studies of Single-Event-Upset in Optical Data Receiver for the ATLAS Pixel Detector

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A multi-channel optical transceiver (opto-board) housing a PiN array coupled to a BPM signal decoding ASIC, was exposed to a proton beam of 24 GeV/c momentum. The 40 MHz clock and 40 Mbit/s data supplied to the opto-board were restored directly on the board and then in addition transmitted back to the counting room for on-line checking of consistency. In the case of a data bit error or a missing clock transition, indicating an occurrence of a SEU, a sequence of time aligned data bits along with the corresponding clock states were recorded for off-line analyses. A compact DAQ system based on a FPGA processor was custom-developed for this task. Measurements were performed for input signals covering a certain range of optical power. We present results obtained from the August 2009 run at the CERN irradiation facility, including the SEU occurrence rate and cross-section, both as a function of the input optical amplitude, along with the time-resolved structure of the SEU incidents.

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1. Introduction

In the ATLAS pixel detector the timing-trigger-and-control (TTC) signals along with the readout-data are transmitted optically to and from the detector over a distance of about 100 m. In the past decade the optolink group has performed numerous detailed studies of the radiation effects on all components of the current optical link system. The results from on-detector components as well as a detailed description of the optolink architecture are presented in reference [1].

It is well known from earlier radiation-induced Single-Event-Upset (SEU) studies [2]-[4], that the optical PiN-diode receiver itself is the device most vulnerable to the instantaneous impact of radiation on transmitted signals due to its comparatively large SEU sensitive area. The PiN-diode coupled trans-impedance amplifier (TIA) is also reported to contribute to the occurrence of SEUs. It is the relatively low-current input-signals that make the TIA components sensitive to SEU incidents.

Taking into account both the expected particle flux of 2×10^{6} $cm^{-2}s^{-1}$ at the optical transceiver's location in the detector and the SEU cross-section of 4×10^{-10} cm^{2} [1] at the average PiN-diode photocurrent of 300 µA [5], the Bit-Error-Rate (BER) induced by SEUs is estimated to be 2×10^{-11} for 40 Mbit/s data transmission rate. This estimate is comparable to the intrinsic BER of $<10^{-11}$ for the data-receiver-integrated-circuit (DORIC) itself and corresponds to about one bit error in 20 minutes. The BER is expected to increase due to the radiation-induced degradation of the optical-fiber attenuation and the PiN-diode responsivity [5], reaching one bit error in 80 s (worst case) at the end of the detector lifetime.

The primary aim of the time-resolved SEU test, performed recently on the receiver part of the optical transceiver (opto-board), was to gain insight into the patterns of transmitted signals during the occurrence of a SEU. Another motivation was the development of more radiation tolerant optical receivers for future high-rate signal transmission applications. A similar time-resolved error-logging approach was adopted previously for a set of comprehensive SEU studies at Multi-Gb/s data transmission rates [6].

2. Experimental setup for time-resolved Single-Event-Upset measurements

The optical receiver used for this SEU study consists of an 8-channel PiN-array photodiode connected to the DORIC chip. In order to evaluate new optical components [7], the standard Si PiN-diode array used in ATLAS pixel detector [1] was replaced by a new generation opto-package [8] with a fast GaAs PiN-diode array [9]. The modified receiver is a prototype for the opto-link design for the future ATLAS pixel inner-b-layer (IBL) project. The block-diagram of the experimental setup used during the SEU measurement is shown in Figure 1. On the FPGA board a pseudo-random data-bit-stream is continuously generated, bi-phase mark (BPM) encoded with a 40 MHz clock and optically transmitted for subsequent decoding to the opto-board exposed to the proton beam. Both recovered signals, data and clock, are transmitted

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optically back to the FPGA board. The returned optical signals are converted into electrical signals by a commercial transceiver [10]. The returned data-bits are sampled by a 40 MHz reference clock on the FPGA board and compared to the data-bits originally generated. A difference in the compared bits causes the next 64 clock cycles to be recorded, as well as the preceding 7 cycles. As with the data-bits, the alternating states of the returned clock are continuously sampled by an 80 MHz reference clock. This allows us to keep track of the clock's transition from 1 to 0 and back to 1. Both clock state sequences 1-0-0 and 0-1-1 are considered to be clock errors and are also used by the test-system to trigger the event recording. The test system stores up to 208 events in a buffer before being read out by the DAQ-notebook.

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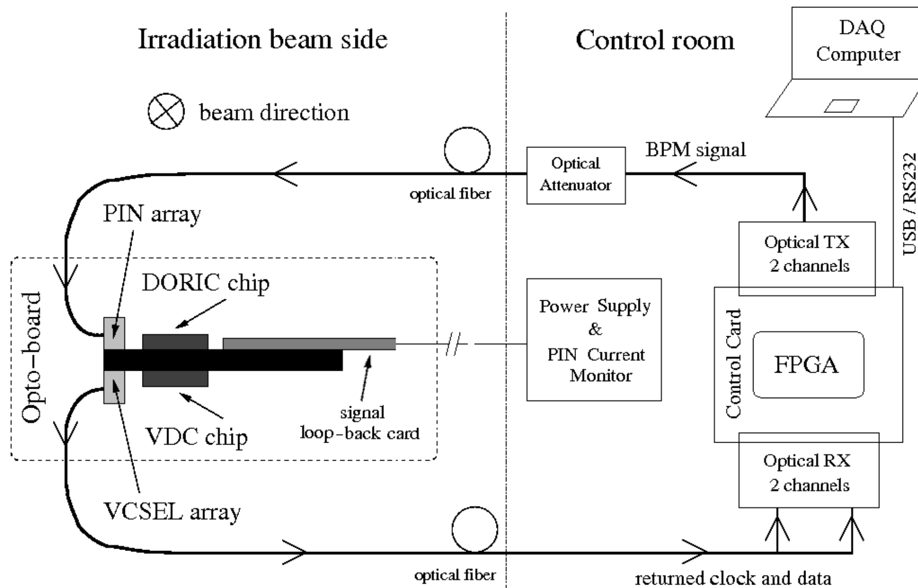

Figure 1:

Block diagram of the experimental setup used for the time-resolved SEU measurement.

The SEU test-system contains a VCSEL-array light emitter and a VCSEL-driver-chip (VDC), both located on the opto-board and used to transmit clock and data signals back to the counting room. These components are not expected to contribute noticeably to the measured SEU rate, due to their large driver-current of several mA.

3. Single-Event-Upset measurement run

The time-resolved SEU measurement was performed at CERN's PS-T7 24 GeV/c proton irradiation facility [11] in August 2009. In ATLAS the expected particle flux in the region where the opto-boards are mounted is dominated by pions with average momentum of 300 MeV/c [3]. Such minimum ionizing pions cannot induce SEU incidents by means of direct ionization; instead they undergo non-ionizing interactions with atomic nuclei, which then in turn produce enough charge to cause SEU effects through secondary ionization. The magnitude of

the non-ionizing cross-section of 300 MeV/c pions and those of 24 GeV/c protons in Si and in GaAs are similar [12]. This fact justifies the use of 24 GeV/c protons for studying the SEU effects in the ATLAS inner-detector's opto-electronics. The SEU data was taken independently on two PiN-array channels. The optical power of the input signal was optically attenuated to nine values between 10 and 110 μA by measuring the photocurrent amplitude in the PiN-diode. The PiN-diode was reversed-biased at +10 V. The lowest optical power, 10 μA, lies just above the DORIC's input current threshold [1], the highest power corresponds to the upper limit of the commercially available optical transmitter. For each optical power setting the beam exposure time was on average 10 proton-bursts, each 400 ms long and separated from each other by a 40 s beam-cycle period. This corresponds to an average exposure time of nearly 4 s at each optical power setting. The average proton flux of 4.18×10^{9} $cm^{-2}s^{-1}$ during the SEU test was deduced from the total proton fluence measured with the Al-strip activation method [11]. In between the proton-bursts the data monitoring was active in order to provide a SEU-free reference measurement. The SEU test data taking was accomplished in two hours of uninterrupted beam time.

4. Classification of Single-Event-Upset incidents

For the purpose of this SEU analysis three categories of upset-incidents were defined:

- **Type-D** (Data) with only data-bit errors observed but no clock deficiency,
- **Type-C** (Clock) with clock deficiency but no data-bit errors,
- **Type-B** (Both) with both data-bit errors and clock deficiency.

A total of **11065** events were collected in this study, among them **8474** events of type-D, **1192** events of type-C and **1399** events of type-B. A few typical events of each type are shown in Table 1. The frequency of SEU occurrence for several conditions of transmitted data-bits and recovered clock states is summarized in Table 2. The underlying selection was done by considering the number of bit-flips as well as affected clock states per SEU incident in parallel with distinguishing between three types of clock state deficiencies (H→L, L→H swaps and inverted clock), as well as two bit-flip modes (0→1 and 1→0) . Furthermore, in absence of bit-errors the transmitted bit-type ('0' or '1') was noted. As a result of this classification there are ten SEU occurrence cases, as listed in Table 2. Individual cases 1 to 10 are discussed in more detail below.

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	1) type-D	2) type-C	3) type-B	4) type-B
photo-current μA	22	55	34	10
Data bits:	001101+0 11010001	01101100 01000101	11101101 -0001101	1011101+ 1111+101
Clock L:	00000000 00000000	00000000 00000000	00000000 00000000	00000000 11111000
Clock H:	11111111 11111111	11111110 11111111	11111110 11111111	11111111 00001111

Table 1:

Typical measured SEU incidents: 1) type-D, 2) type-C and 3), 4) type-B. A '+' and '-' indicate 0 →1 and 1→ 0 bit-flip errors respectively.

Only five additional bit-errors were detected in between the bursts when the proton beam was off and the recovered signals were monitored. As a result of this analysis an intrinsic bit-error rate of 1.7×10^{-11} was estimated.

<table>
<tr><th rowspan="3">Type D
77%
only data affected
8474 events</th><th># Bit-flips</th><th>Bit-flip type</th><th>Case</th></tr>
<tr><td rowspan="2">one 8463</td><td>0→1 7815</td><td>1.</td></tr>
<tr><td>1→0 648</td><td>2.</td></tr>
<tr><td></td><td>two 11</td><td>both</td><td>3.</td></tr>
</table>

<table>
<tr><th rowspan="3">Type C
11%
only clock affected
1192 events</th><th>Clock deficiency</th><th>Bit transmitted</th><th>Case</th></tr>
<tr><td rowspan="2">H→L 1077</td><td>'0' 953</td><td>4.</td></tr>
<tr><td>'1' 124</td><td>5.</td></tr>
<tr><td></td><td>L→H 115</td><td>'0' 115</td><td>6.</td></tr>
</table>

<table>
<tr><th rowspan="7">Type B
12%
both clock and data affected
1399 events</th><th># Clock states</th><th>Clock deficiency</th><th># Bit-flips</th><th>Bit-flip type</th><th>Case</th></tr>
<tr><td rowspan="3">one 1014</td><td rowspan="2">H→L 904</td><td rowspan="3">one 1014</td><td>1→0 830</td><td>7.</td></tr>
<tr><td>0→1 74</td><td>8.</td></tr>
<tr><td>L→H 110</td><td>0→1 110</td><td>9.</td></tr>
<tr><td rowspan="3">two and more 385</td><td rowspan="3">reversed clock 385</td><td>two 214</td><td>0→1 214
for 2nd bit-flip</td><td rowspan="3">10.</td></tr>
<tr><td rowspan="2">one 171</td><td>0→1 115</td></tr>
<tr><td>1→0 56</td></tr>
</table>

Table 2:

SEU frequency of occurrence for various conditions of recovered clock and transmitted data (cases 1 to 10), compiled for events of type-D, -C and -B.

5. Single-Event-Upset rate and cross-section

The experimentally obtained SEU rate, calculated as a ratio of the SEU occurrence during the 400 ms long proton spill and the amount of data-bits transmitted during the spill, is shown in Figure 2 as a function of the input signal amplitude as given by the photocurrent in the PiN-

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diode. In general, the PiN's responsivity (A/W) relates the photocurrent in the PiN-diode (A) to the optical power (W) of the light input signal. Due to radiation damage the actual PiN responsivity is continuously decreasing and hence is considered to be an unknown quantity during the test measurement. As shown in Figure 2, the SEU rate decreases rapidly with the increasing amplitude of the input light signal. Such characteristic behavior was also reported by previous SEU investigations [1], [3], [4]. From a practical standpoint, this observation provides a way to mitigate the SEU effects by boosting the amplitude of the input light signal to the PiN-diode receiver. We conclude from the decomposition of the total SEU rate into D, C and B contributions (see Figure 2), that the type-D events clearly dominate the SEU rate for all optical power settings with nearly 77% probability of occurrence. Furthermore, for type-C and -B events a relative contribution of the order of 12% each was observed for all optical settings. It is a common practice to predict the expected SEU rate by multiplying the experimentally obtained SEU cross-section at a given signal amplitude by a given particle-flux. In Figure 3 we present the newly measured SEU cross-section, defined as a ratio of the SEU occurrence (per unit of time) and the corresponding proton flux, as a function of the input signal photocurrent.

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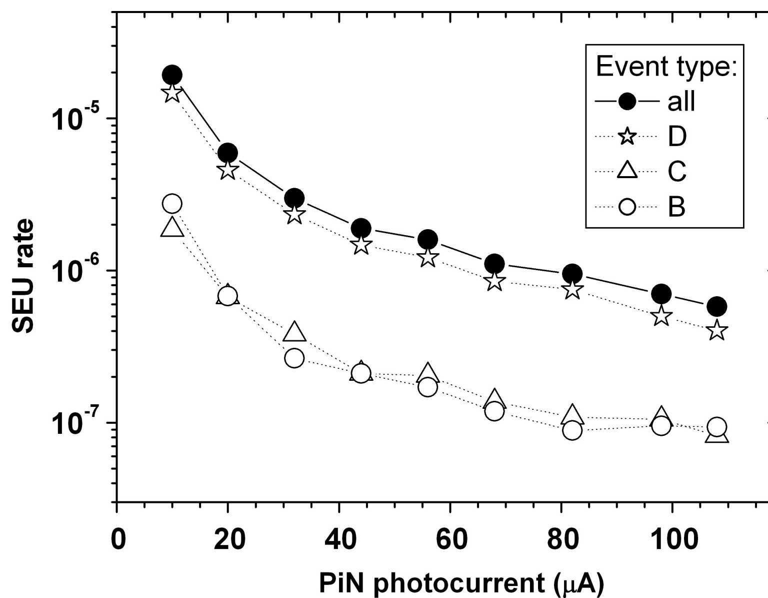

Figure 2:

Dependence of the SEU rate as a function of PiN-diode photocurrent for all event types.

The underlying data includes contributions from all event types and results from averaging two PiN-channels, for which the measurements were individually performed. The cross-section's relative error of 18% arises from channel averaging (16%) and from the uncertainty in the

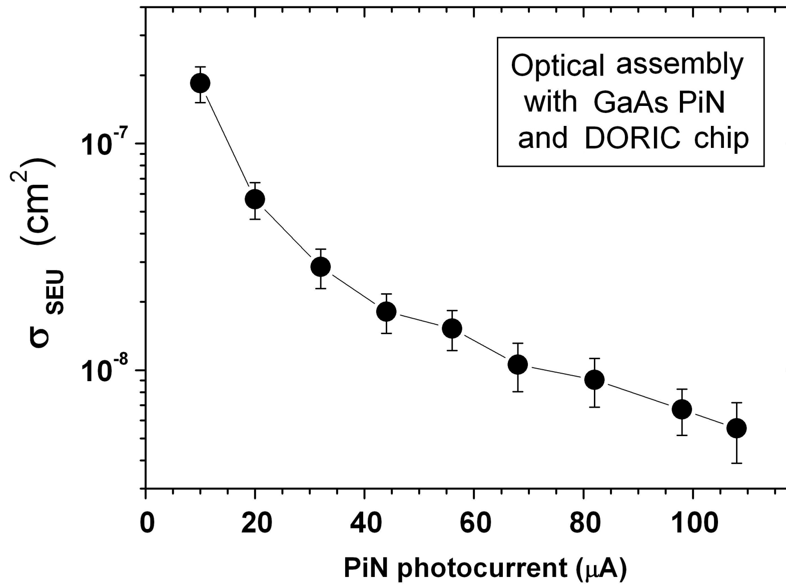

Figure 3:

Measured SEU cross-section as a function of the PiN-diode photocurrent.

determination of the total proton fluence (8%) [11]. A comparison with our earlier SEU cross-section measurement [1] shows good agreement. Unfortunately the latest measurements are limited to optical power settings below 110 μA, a setting close to the lowest expected PiN photocurrent of 100 μA [5], whereas the earlier published measurements provides SEU cross-section data covering PiN-diode photocurrent signals up to 500 μA. Thus only the earlier data can be used for predictions of the SEU rate for the expected optical input power range. Below we discuss in detail the SEU rate decomposition into type-D, -C and -B contributions.

6. Time-resolved results

6.1 Type-D events

The type-D events (cases 1 to 3 of Table 2) clearly dominate the total SEU rate with a probability of 77%. They appear as 0-to-1 and 1-to-0 bit-flip errors with relative rates measured as 92% and 8% respectively. The error rate for the 0-to-1 transition is expected to be the largest. When data bits are transmitted directly without encoding, extra charge deposited by an

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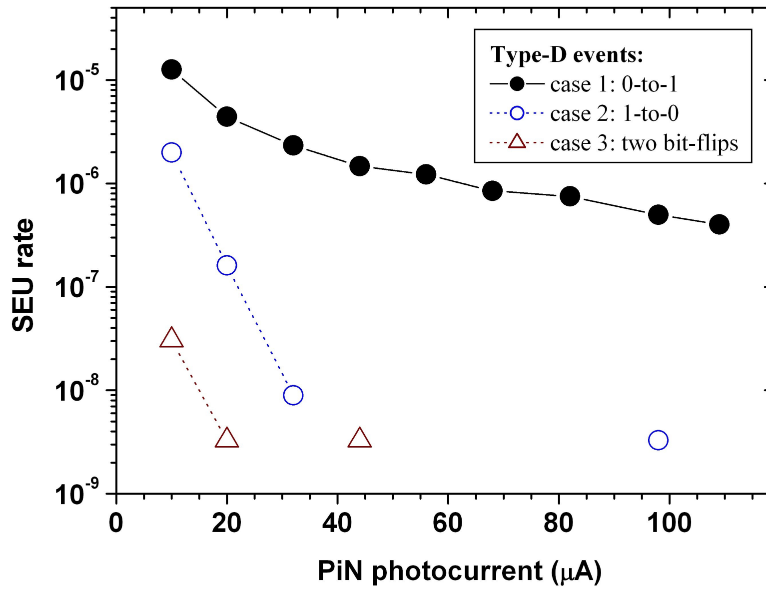

Figure 4:

Dependence of the SEU rate for events type-D, case resolved, as a function of PiN-diode photocurrent.

ionizing particle in the active area of the PiN-diode is likely to cause a 0-to-1 bit-flip. Obviously, bits sent as ‘1’ cannot be turned directly to a ‘0’ this way. However, when the data stream is bi-phase-mark encoded, both 0-to-1 and 1-to-0 bit-flip modes are technically possible. This can be understood by considering the decoding scheme of the receiver chip. When data-bits are sent as ‘0’ and a SEU occurs, the edge-detector cell, i.e. the logic which produces narrow pulses for each detected signal edge [1], is likely to create an additional edge-pulse out of the charge deposited between the edges of the PiN signal. This extra pulse is then interpreted as 0-to-1 bit-flip. On the contrary, for data bits sent as ‘1’ along with extra SEU charge injected between the PiN-signal’s edges, the edge-detector cell is likely to generate two edge-pulses nearly merged together. The data bit ‘1’ information is obscured and yields a 1-to-0 bit-flip error as a result. As shown by our experiment, this last scenario is a factor of 10 less likely to happen (case 2 in Table 2); presumably due to a larger charge required to satisfy the pulse-merging condition. This assumption is supported by the result presented in Figure 4, where the dependence of the SEU occurrence rate on optical input power is shown separately for cases 1 and 2. The 1-to-0 bit-flip contribution is explicitly confined to low values of optical power. Thus for PiN-photocurrents exceeding 40 μA only the 0-to-1 mode is of practical concern. Nearly all type-D events have one bit flipped as there are only 11 events with two bits flipped (case 3). These events (see Figures 4 and 5) result either from a pile-up of two type-D events or from a radioactive decay of an activated nuclei.

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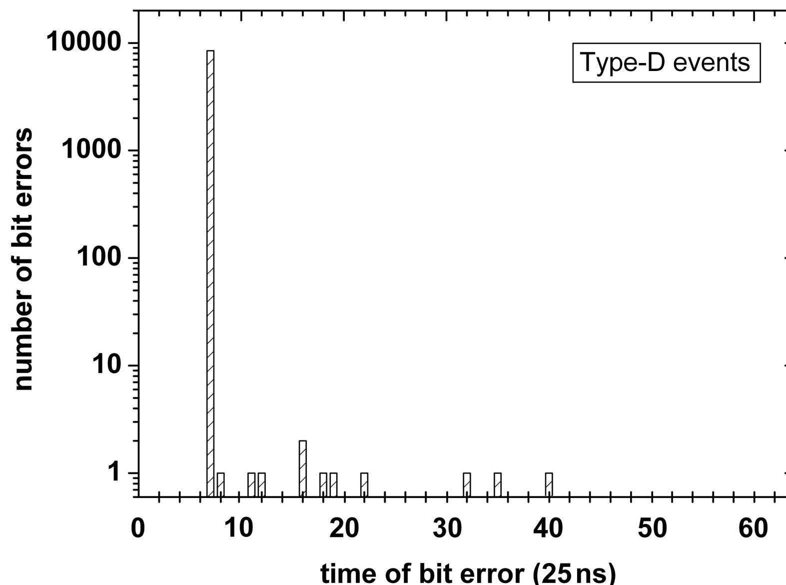

Figure 5:

Time distribution of type-D bit-errors. The errors outside the main peak also have a corresponding error in the main peak.

6.2 Type-B events

The measured total rate of type-B events is about 12%. Nearly 2/3 of type-B events are affected by only one clock cycle and simultaneously by only one data-bit error (case 7 to 9 in Table 2). Most of them (case 7) have one clock cycle with its high state missing while at the same time the associated data-bit is originally set to '1' but decoded as '0'. A distribution of the occurrence time for type-B events is shown in Figure 6. The maximum of the distribution occurs one clock cycle after the clock error is detected (time-bin 7 in Figure 6). This is understandable since on the receiver chip the recovered clock cycle is subsequently used for data bit extraction: a corrupted clock cycle produces a bit error one clock cycle later (see also Table 1.3). The SEU rates for case 8 and 9 as shown in Figure 7 are significantly suppressed and confined mainly to input optical power below 40 µA. Events with two bit-errors are a factor 5 less likely. There are no events with more than two bit-errors. All two bit-error events and some one bit-error events are associated with more than one affected clock-state (case 10). These events are correlated with a high number of data-bits set to '1' and transmitted in a single-chain. A typical event of this type has the signature shown in Table 1.4. Although SEU events of case 10 occur with a probability of only 3.5%, we carefully study such events because of their long-term impact on

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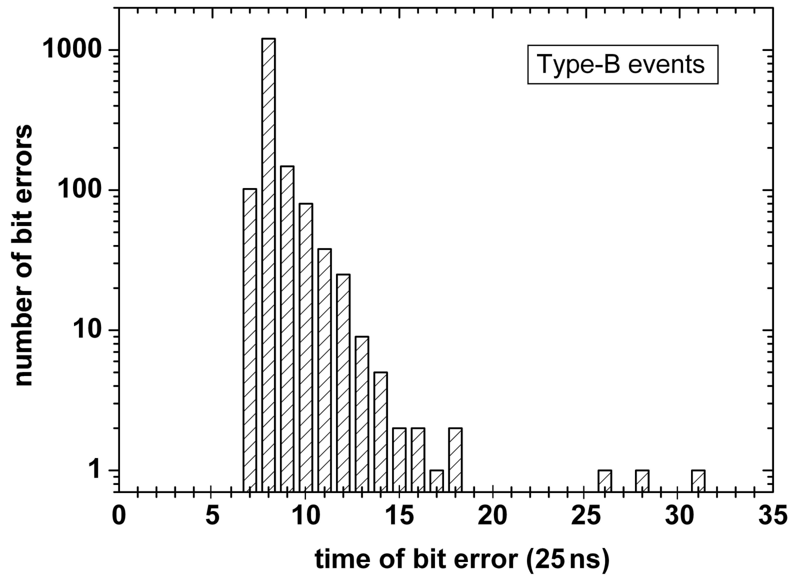

Figure 6:
Time distribution of bit-errors in type-B events.

the recovered data and clock. In fact for all case 10 events a chain of inverted clock cycles was observed (see Table 1.4). In the majority of these events the inverted clock chain is spanned by two data-bit errors. This is why the bit error occurrence time in Figure 6 marks the actual

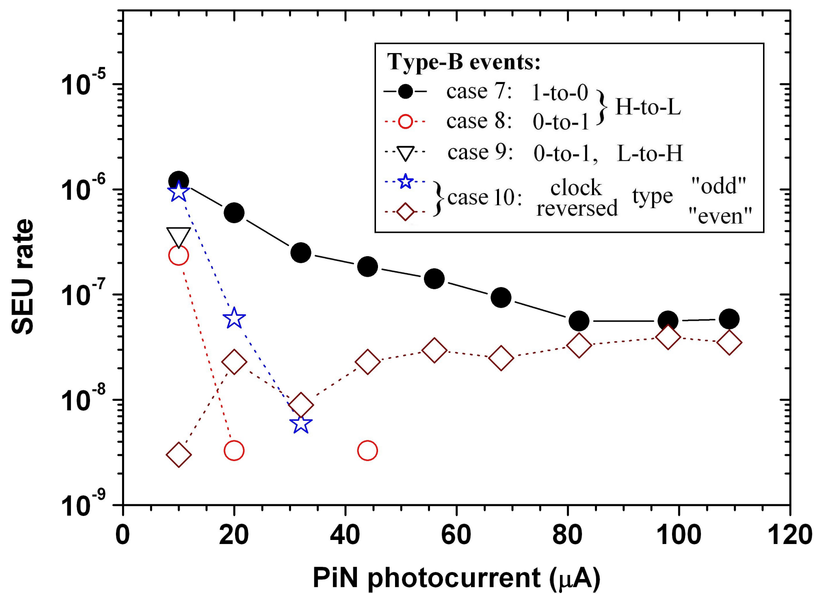

Figure 7:
Dependence of the SEU rate for events type-B, case resolved, as a function of PiN-diode photocurrent.

duration of the inverted clock chain. After a certain number of clock cycles the inverted clock becomes re-inverted to its original state by the appearance of a data-bit set to ‘0’ thus ending the

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preceding data-bit '1' sequence. It is interesting to note that the probability of case 10 events occurring with an even number of inverted clock-states is roughly a factor of ten larger than the one with an odd number, as shown in Figure 8. At the same time the "odd" type of case 10 is confined to low optical power, as further inspection of Figure 7 reveals. On the contrary, the occurrence rate of case 10 events with an even numbers of inverted clock-states ("even" data-points in Figure 7) is fairly PiN-photocurrent independent. The clock reversed case 10 events appear to have two different origins, one favoured at lower optical input power, the other being input-power-independent. However, a common cause of the clock inversion can be understood

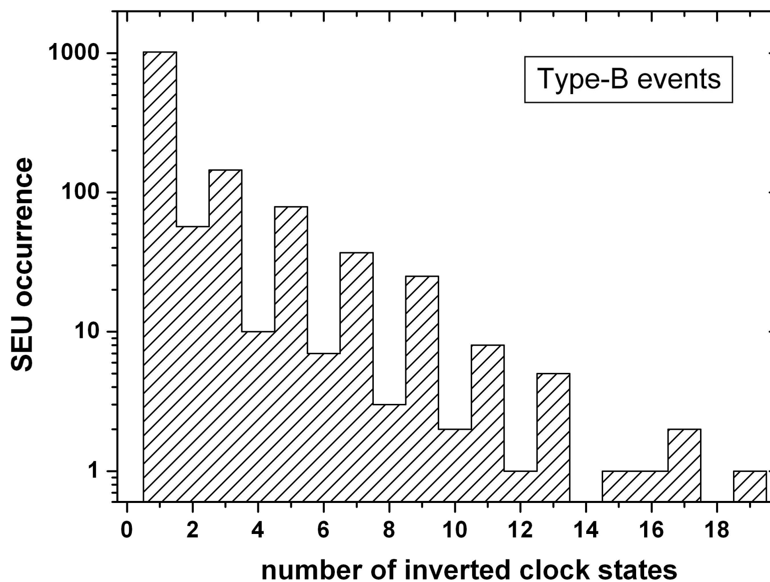

Figure 8:
Dependence of the SEU occurrence on the number of inverted clock-states for type-B events.

by considering the decoding part of the DORIC chip. Its upset sensitive circuit element is the D-flip-flop cell used for reconstruction of the 20 MHz clock signal, which in turn is presented to an exclusive-or cell for 40 MHz clock regeneration (see DORIC's block-diagram in [1]). The clock-inversion is triggered when the regular state transition of the D-flip-flop output signal is delayed until the D-flip-flop cell becomes clocked by an edge-pulse originating from a data bit '1' transition. In this way the output signal of the D-flip-flop becomes time-delayed by half of the 40 MHz clock period. The inverted clock condition is sustained by each edge-pulse originating from successive bits transmitted as '1'. In turn, the inverted condition is terminated when the first missing edge-pulse occurs, which is when the data-bit transmitted becomes '0' (event dump in Table 1.4).

6.3 Type-C events

The type-C events, which occur about 11% of the time, are characterized by only one clock cycle affected and no data-bit errors. In 80% of cases they have one clock cycle with a missing

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high state while at the same time the data-bit under transmission (one clock cycle later) is set to ‘0’ (case 4 in Table 2). As indicated in Figure 9 this event mode shows a typical SEU rate decline with increasing optical input power. In contrast, a data-bit transmitted as ‘1’ will most likely be afflicted with 1-to-0 bit-flip error due to a missing clock high state; this results in a

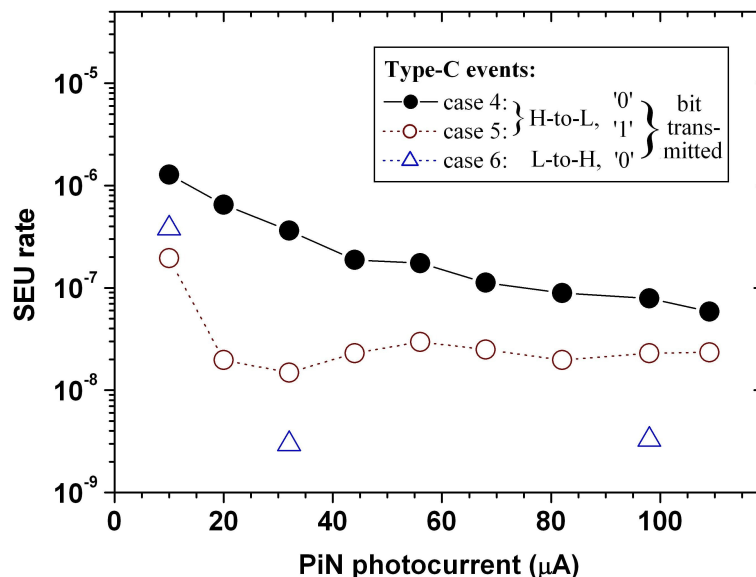

Figure 9:

Dependence of the SEU rate for events type-C, case resolved, as a function of PiN-diode photocurrent.

low occurrence rate for case 5. It is interesting to note that the experimentally obtained case 5 SEU rate appears to be independent of the PiN-diode photocurrent amplitude with the exception of the lowest power setting (Figure 9). This may indicate that the cause of the upset may be in the decoding part of the receiver chip. Finally, events displaying one missing clock-low state (case 6, Figure 9) are both suppressed as expected and mostly confined to lower optical input power. For all SEU induced clock errors (type-C and -B), the recovered clock signal always returns to its original phase.

7. Summary

We have analyzed SEU data collected during our first time-resolved measurement with the optical receiver. A set of initial results is discussed in this paper. The rates for various error conditions of reconstructed data and clock signals were obtained and analyzed for a range of optical input power up to 110 μA. These results provide insight into the causes of SEU induced errors in the optical receiver assembly. The detailed timing analyses of the decoded data-bits and recovered clock states provide additional useful information about the event’s internal bit-structure, presumably the location of occurrence, and indirectly, the mechanism of the error introduction. Our findings are summarized below.

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• The main SEU contribution, more than ¾ of all cases, has the simplest possible structure: only one data-bit is flipped, mostly 0-to-1. The 1-to-0 bit transition occurs with a rate one order of magnitude lower and is confined to low optical input power (< 40 μA).
• Approximately ¼ of all SEU cases have the decoding clock affected by the SEU incident. In 20% of all SEU cases only one clock cycle is disturbed resulting in the clock's high state to be missing. If at the same time the transmitted data-bit is high, then additionally a 1-to-0 data bit-flip normally occurs.
• In about 3.5% of all SEU cases the recovered clock becomes reversed for a period of up to 10 clock cycles, where mostly two data bit-flips span the reversed clock burst. This type of SEU effect happens when at the same time a sequence of data-bits all set to '1' is transmitted. Here the decoding circuit gets upset and locks temporarily to the data-bit transitions instead of the nominal clock transitions.
It is generally not possible to discriminate between SEU incidents occurring either in the PiN-diode, TIA- or decoding part of the receiver, without selectively shielding the radiation sensitive areas in the components during the measurement [6]. However, this is not practical in our situation using a 24 GeV/c proton beam. In addition, some of traceable SEU induced effects result presumably from a combined interaction of more than one component. Nevertheless, our time-resolved measurement provides evidence for SEU cases which are strongly confined to lower optical input power and thereby more likely to be attributed to the PiN-TIA locations, as well as other cases mostly independent of the optical input power and thus favoring SEU incident locations in the decoding part of the receiver.
One way to minimize the SEU effects in the PiN and TIA components is to use high input optical power. Another even more powerful technique would be to implement a Forward Error Correction (FEC) bit encoding scheme. The occurrence of the SEU becomes even more important when data transmitting ASICs are designed for lower supply voltages and the area of the sensitive circuit becomes smaller. For instance, the CMOS-130 nm process is expected to be nearly four times more SEU sensitive than the 250 nm process previously used. Special design techniques, in particular a triple modular redundancy (TMR) scheme, are needed to lower the probability of a malfunctioning circuit due to a SEU.
We plan to continue time resolved SEU studies in the near future by studying new PiN-array assemblies and new receiver and decoding integrated circuits, both designed for data transmission rates much higher than 40 Mbit/s. We are going to improve the SEU test system by allowing for larger input signal optical power and by using an order of magnitude faster signal sampling rate inside the FPGA.

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