PROCEEDINGS OF SCIENCE

New Concepts in Powering for the LHC Upgrade

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Detector mounted electronics for the upgraded LHC will need to take advantage of recent advances in deep submicron integrated circuit technologies in order to instrument a larger number of more closely packed silicon strips and pixels and collect data at higher rates. Although these technologies will operate at lower voltage, the total current requirements will likely be significantly larger than that for detectors presently in place. At the same time there will be a push to lower the material in the inside of the detector to improve the quality of the measurements. New powering techniques bringing more power into the detector over the same or a lower mass cable plant will be expected. To do this the voltage carried over the power cables will be increased to ten or more times that required by the front end electronics. Low mass power convertors will be added to the list of on detector components. These blocks will need to operate efficiently in a high magnetic field and meet the same radiation, reliability and low overhead requirements incumbent on the front end electronics they service. Two powering techniques are being investigated: Serial powering and DC-DC converters, each with several possible implementations. Work is presently underway to design and prototype realistic radiation tolerant powering blocks that can be used to achieve module level power conversion requirements with lower mass cabling for the next generation of LHC detectors.

19th International Workshop on Vertex Detectors - VERTEX 2010
Loch Lomond, Scotland, UK
June 06 – 11 2010

[1] Speaker

PoS(VERTEX 2010)003

1. Introduction

Tracking detectors at the LHC are designed to maximize the active sensor area and minimize mass. The density of channels is roughly inversely scaled to the distance from the interaction point to provide good position information and minimize occupancy. In practice this led to the well known onion shell aproach to detector construction at collider detectors. The desire for hermiticty coupled with the design luminosity of ~10^{34} at LHC led to a complex array of detector sub-systems and services that fills the volume of the tracker. Power and data cables for each sub-system are routed at the edges of the sensor arrays and then past other outer systems to the outside of the detector. The cross sectional area for these services was intentionally limited to only what was needed by design in order to minimize dead areas of the detectors.

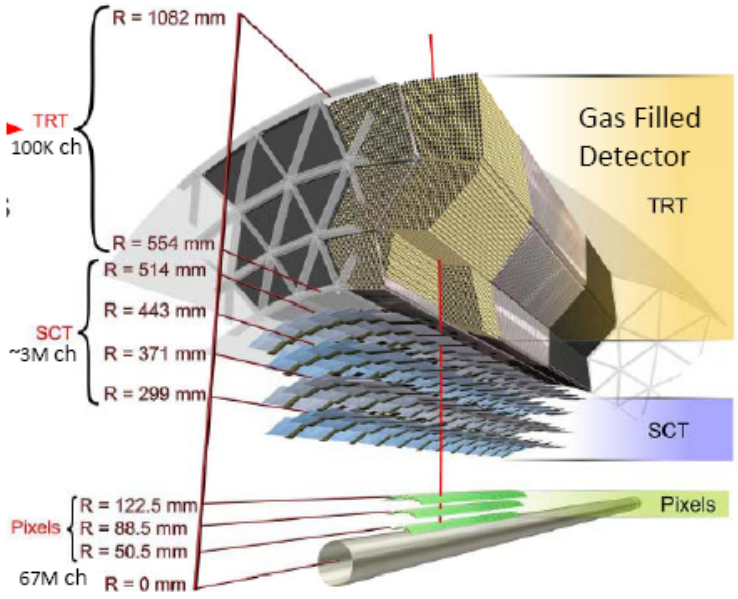

Figure 1 Barrel part of the ATLAS inner tracking detector. The number of channels in each detector sub-system scales with the particle flux at their location ranging from nearly 100 million in the (innermost) Pixel detector to 100K in the TRT. The barrel detector is designed so that power, monitoring and readout services for each sub-system can be routed out of the detector at either end.

Figure 1 shows the ATLAS inner detector with a section of the barrel portion of the Pixel detector, silicon strip detector (SCT) and Transition Radiation Tracker (TRT). Power for LHC detector systems is supplied remotely with the incoming voltages matched to the requirement for the custom integrated circuits. Cable granularity is determined by the groupings of sensors mated to the front end electronics hereafter called modules. These modules have multiple integrated circuits wired in parallel and readout a few hundred to many thousand sensors. Power supplies are located far from the interaction area in a low radiation area. The present generation of detector mounted LHC front end electronics employs parallel powering. Low

voltage power supplies for modules are isolated by design and each provides a few amps of current to one or a few modules through a long cable with both the supply and return lines specific to that powered unit. The cross sectional area of copper in the supply and return lines on the detector has been minimized, limited primarily by the cooling burden of heat loss due to the resistive voltage drop in the cables. Figure 2 shows the TRT and SCT barrel during

Figure 2 Barrel TRT and SCT installation into the ATLAS detector. Cable services take nearly all available space between the inner tracker and calorimeter.

insertion into the ATLAS detector. Most of the cable services seen coming in from the outside of the detector are routed between the outer part of the TRT and the Inner side of the Liquid Argon Calorimeter. A more complete explanation of the ATLAS sub-systems can be found in various places including [1].

Proposed improvements in the luminosity for an upgraded LHC machine are targeting an increase in rate of at least 5 fold over the original LHC design luminosity. This will require replacement of most or all of the present LHC tracking systems. To keep occupancy manageable the new pixels and strips will need to be smaller in dimension, increasing the total channel count significantly. New ASIC technologies employed will operate at lower voltage, lowering the overall power consumption per channel, but are not likely to require lower current per channel. In fact it is quite likely that the total current requirements will be higher than at present due in part to the larger number of readout channels. If the current LHC approach of providing power from off detector supplies to the front end electronics at the voltages required by the front end electronics is maintained a larger cross-section of cable will be required. This is unlikely to be acceptable given that one of the objectives of the upgraded detector will be to lower or keep the total amout of material the same. Thus a re-thinking of the overall powering scheme is underway for the new tracking systems being designed.

2. Power for upgraded LHC detector systems

Power companies have long known that in order minimize the cable resource required to deliver power from the source efficiently to a broad nework of distribution nodes the voltage must be increased to levels significantly above those required by the equipment attached at the user end. This problem has classically been solved using step up transformers on the sending end to boost the voltage going to the power line and then a step down transformer to reduce the voltage to a standard value for use on the recipient's side. This kind of approach is being evaluated for upgraded detector systems at the LHC where the crossectional area of the power cable plant must stay the same or decrease for on detector power distribution while the need for current will remain the same or grow as the segmentation of the detectors (and channel count) increases.

Power for detector mounted LHC electronics brings additional requirements for radiation and Single Event Effect (SEE) tolerance, and the need for remote voltage monitoring and control. Guidelines for power services will ideally address the following issues:

1. Ability to work in a relatively high magnetic field.
2. Suitable Radiation hardness and reliability to ensure 10 year operation.
3. Low cable mass and low mass in the on detector voltage conversion blocks.
4. Minimal collateral loss due to component failure.
5. Maximum operability, low probability of false trips, remote restoration of power.
6. Minimal additional power overhead in control and conversion.
7. Minimal interference with normal operation of the sensor readout. This includes operation without significant increase in systematic or random noise in the signal.

The LHC community has converged on two approaches to this problem. Serially connected modules with equal current and single or multi-step high efficiency DC-DC convertors. Both may find a place in LHC's upgraded tracking detectors.

3. Serial Powering

Serial powering offers a very simple approach for systems where the current requirement

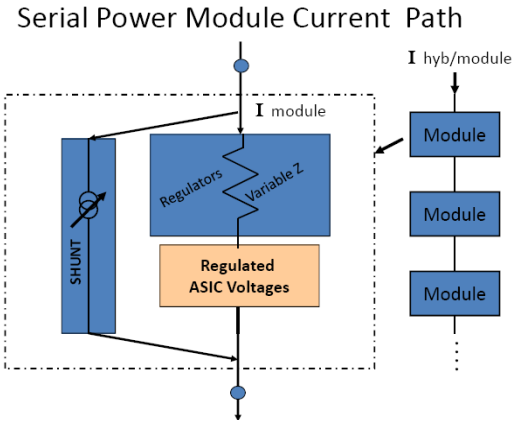

Figure 3 In Serial powering a constant current is passed from one module to the next. A shunt regulator is used to control the voltage across the module.

is constant among adjacent modules. As implied by the name, modules are series connected and a constant current is passed from one module to the next. The voltage across the module is regulated by shunting current around the load as shown in Figure 3. Typically the voltage drop across each module is the same. In this case, the voltage supplied to the serial chain of *n* modules must be the sum of the voltages for each module.

$$\mathbf{V_{supply}} \sim n^* \mathbf{V_{module}}$$

The reduction factor in current compared to parallel powering for the chain is n, subject to details of module current draw uniformity and control overhead.

The voltage across a module is a free parameter and can offer an operational voltage dependent buffer allowing multiple LDO's (Low Drop Out regulators) to deliver independent voltages to each module at the usual expense of power loss typical of any linear regulator.

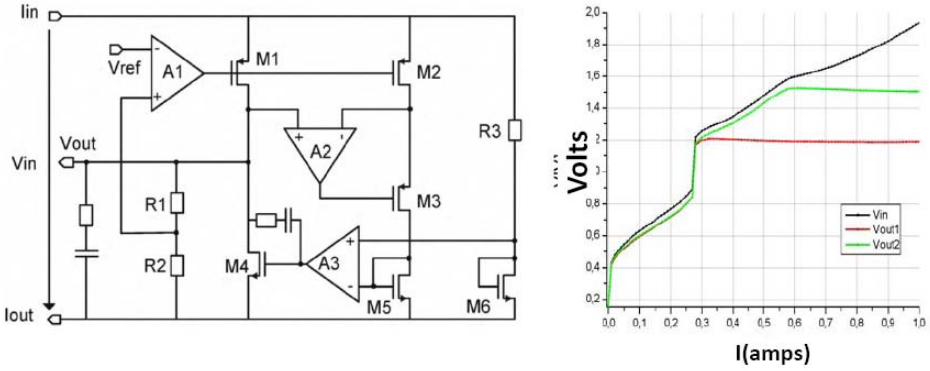

Figure 4 The block diagram of the serial power Shunt LDO(output Vout), designed by Bonn for the upgraded ATLAS Pixel subsystem. The performance of a fabricated version is shown in the graph on the right where a second LDO with a lower output voltage was added in parallel with Vout. The upper trace is the voltage across the regulator versus serial current and the lower two traces are the two LDO regulated voltage outputs.

The block diagram for a single LDO output shunt regulator proposed for the upgraded ATLAS pixel readout [2] is shown in Figure 4. The shunt current (see shunt block, figure 3) flows through R3 and the vertical transistor stack M2, M3 and M5. The plot on the right shows the measured performance of a prototype where a second lower voltage LDO was wired to Vout of the first. The plot shows that as the serial power current in the chain is increased while the local loads on the LDO's are constant the voltage across the module increases nearly linearly. This resistive behavior allows a current reserve for varied operational load currents.

In digital ASIC blocks the current requirement is primarily determined by the number of clocked elements which may vary widely based on operational modes. The worst case is when the clock to a module is turned *off* or *on* when the current to the digital blocks may vary by more than 75%. Since these major changes in current requirements may occur over a few clock cycles the serial power shunt regulators need to have high response bandwidth. Typically a shunt current range equal to the full current draw of the module is considered safe. Two approaches to handling the large current variation of several amps for the ATLAS SCT have been examined.

The first technique is to handle the shunt current within the shunt control ASIC as is done on the SPI chip developed at FNAL. This versatile ASIC has several independent blocks for testing various aspects of serial powering, but it's primary purpose is to offer a versatile self contained Serial Powering solution where the shunt and regulator blocks depicted in figure 3 are contained in one ASIC. A special bump bonded die attach is used to keep the hookup resistance low and allow the chip to channel shunt current for the whole module through the die. A block diagram detailing the functional blocks of the SPI chip is shown Figure 5. The SPI chip's shunt regulator, including current shunting transistor is depicted as a zener diode in the block diagram. The two blocks labeled *Linreg* may be used as part of the serial powering scheme or separately. The SPI chip also includes over current sensing and a special module shut down mode. The large transistor (shown straddling the Zener diode symbol) on the die to provides a low impedance path to conduct nearly all of the module current when turned on. This reduces the voltage drop across the module to about a hundred millivolts while shunting up to four amps of current, lowering the module power dissipation to a small fraction of it's nominal value[3]. Control of the SPI chip is accomplished through it's differential AC capable serial communication ports. In addition it contains 6 uncommitted differential bi-directional AC ports to enable communication with front end ASICs at different voltages along the chain. It should be noted that the SPI chip also includes sleep modes to explore possible ILC implementations.

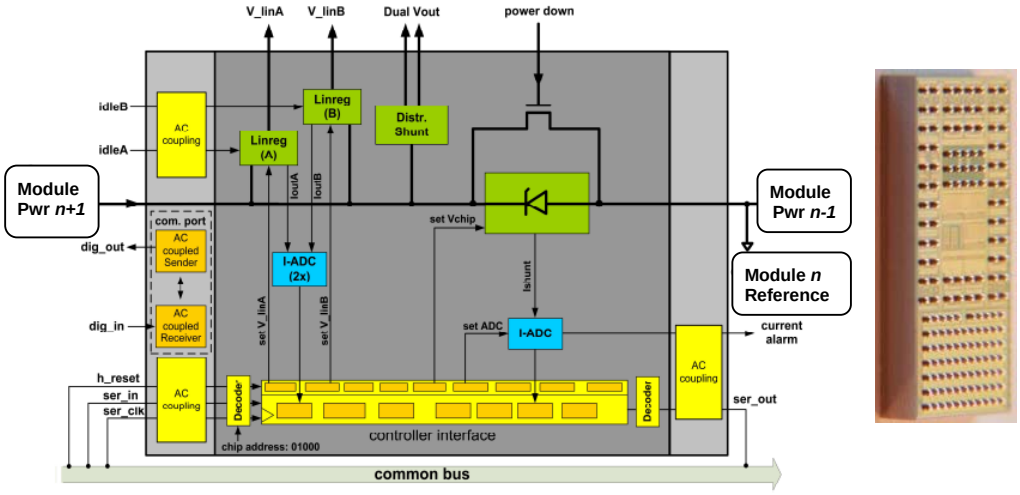

Figure 5 The Serial Powering Integrated Circuit (SPI) chip: functional Block diagram on the left and chip die on right showing arrayed high density bump bonds to carry several amps of shunt current from module to module. The shunt regulator including the on board current shunt transistor is represented as a Zener diode in the diagram. Two low dropout linear regulators(Linreg(A), Linreg(B)) are wired in parallel powered by the shunt regulated output voltage. As noted in the annotations on the left and right sides of the block diagram, the serial current is passed module to module with the voltage at the output of module n-1 forming the local reference for module n shown in the diagram.

A second technique currently used as default for the stave development for the ATLAS SCT is to distribute the shunt current and module shut down current among all front end ASICs reserving a small area on each die for an externally controlled current shunt transistor (~200umX300um) that can handle up to 500mA of current. Referring to figure 3, this technique splits the shaded box labeled *shunt* into two parts: Shunt transistors located on each of the front end chips to shunt excess module current and shunt voltage sensing and control located

in a dedicated ASIC on the module. The two parts communicate through one or more control lines bussed to the front end chips on the module. The control ASIC may be as simple as an operational amplifier and voltage reference. The front end ASIC based shunt transistors are designed for contingency. Each can handle sufficient current for the needs of more than one front end ASIC so that multiple control networks can be implemented, each with sufficient current handling capacity to service a full module. Distributing the current draw among the front end ASICs has the advantage of eliminating the high current density in any one place and keeping the power dissipation distributed among ASICs uniform independent of operating conditions. Figure 6 shows the wide operational current range across a hybrid designed by Liverpool. This first implementation of the distributed shunt technique is used to power 20 ATLAS SCT 2.5V ABCn ASICs [4].

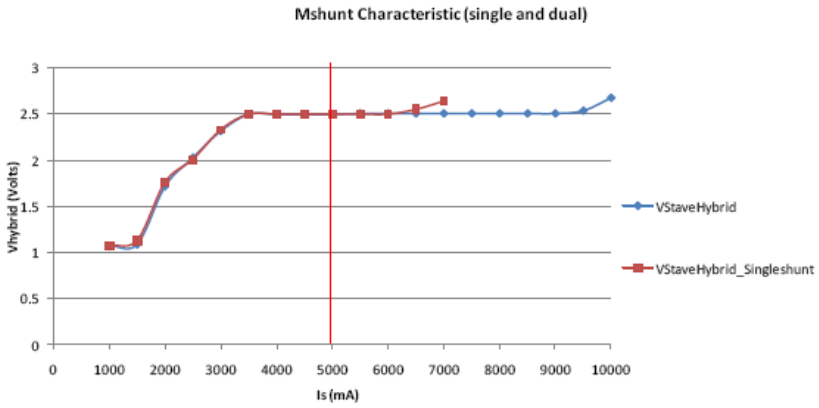

Figure 6 The current versus voltage characteristic of a 20 ASIC ATLAS Upgrade SCT Hybrid implemented using the dristributed shunt Serial Power approach. Normal operation using the shunt transistors in all 20 front end ASICs is shown by the trace in blue. The red trace indicates the response if one of the two shunt control lines is non functional and only half of the ASICs are available for shunt control in either case the reserve current is more than sufficient to exceed the maximum required module current of 5A.

The two traces in the plot refer to the use of ten or twenty front end ASICs through separate control lines to control the shunt current. The red trace showing an increase in voltage (loss of regulation) at about six amps of current is for the case where only one control line, distributed to half of the front end chips on the module is used. This case is shown to demonstrate the contingency afforded by splitting the module control into two parts. The six amp control range available is well above the worst case requirement of five amps for module control depicted by the red vertical line in the plot. The soft rise in voltage with excess applied current should also be noted, indicating a non catastrophic failure as the current increases beyond the regulation range. The low output impedance of the distributed shunt is indicated by the flat voltage response throughout the operational current range of 3.5 to 9.5 amps for the nominal case of all 20 ABCn ASICS on a hybrid being used to distribute the module shunt current. A commercial opamp and voltage reference (shown in the yellow box in figure 7) comprise the complete

control package used in current prototypes. In the future these will be replaced by a separately powered rad hard dual output opamp to be mounted similarly on the hyrid[1].

A single wire addressable, separately powered ASIC is under development to allow external control for this distribututed power technique[5]. The distributed shunt technique regulates a single module wide voltage. It is expected that linear LDO's will be added where required within each front end ASIC.

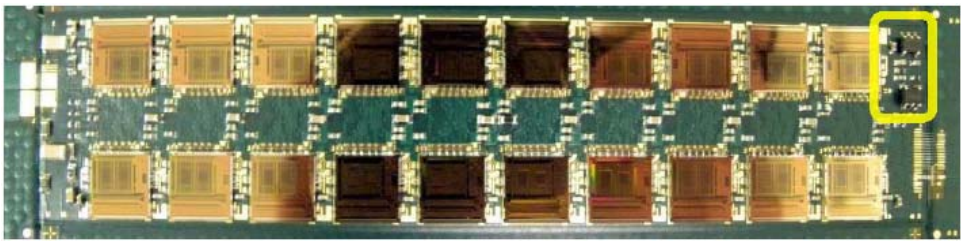

Figure 7 The distributed shunt contol logic is shown within the yellow box on the ATLAS SCT upgrade prototype hybrid demonstating the minimal material burden of this approach. The distributed shunt transistors are located in each of the 20 front end ASICs shown in the picture. A Separately powered control ASIC under development will replace this logic in an estimated 4mm^2 area.

An important element of the serial powering approach is the serial chain current supply. It should be constructed to have both a relatively high output dynamic impedance (>1000Ω) and protection against over voltage. A *high side* programmable current supply has been developed by RAL that includes voltage compliance limits so that in the event of a sudden impedance change the output voltage will not exceed the programmed limit. There have been some concerns the delay in the control loop caused by transmission line effects of the long cables, but these are easily eliminated by introducing a filter network on the load side (ordinarily used to filter conducted EMI from the cable into the detector) with sufficient capacitance to limit the voltage slew rate (I/C) until the current supply can sense the increasing voltage (~1us) and limit the current.

Some of the unique issues concerning serial powering are:

1. Data and Monitoring lines must be AC coupled to accomodate the large voltage drop across multiple serially connected modules.
2. The current in the chain must be equal to or higher than that required by the module with the highest current draw in the chain.
3. The loss of a series connection will disable the whole string of series connected modules making highly redundant connections between modules a requirement.
4. Each module must have a power down mode to avoid thermal runaway due to loss of regulation or cooling. This is accomplished by shunting the module current across a low on resistance device. (For the ATLAS SCT upgrade prototypes a last resort over voltage triggered SCR designed by BNL is used.)
5. A separately powered system is required to provide a remote module shut down[2].

[1] Note that the block labeled Distributed Shunt shown in Figure 5 is a radiation tolerant prototype of the Dual Output opamp for distributed shunt serial powering that has successfully been used to control a hybrid as shown in figure 6.

[2] The accepted way to shut down a module is to reduce the voltage across it to near zero. For external control over the shutdown of individual modules an external supply separate from the serial power current source is required.

6. In some proposed configuraitons, such as the ATLAS SCT barrel more than one serially powered unit may connect to a sensor array with a common substrate. The implications for sensor integrity and signal quality need to be examined.

Three serial powering approaches developed for the ATLAS Silicon strip tracker are described in reference[6]. Serial powering is under active consideration for both the the upgraded ATLAS pixel and SCT although no decision has been made.

4. DC–DC Powering

DC-DC powering is a versatile approach used widely today in commercial and industrial products to change from one voltage to another using capacitive or inductive energy storing mechanisms. DC-DC power convertors have become an integral part of the power management for CPU and support devices as integrated circuit technology has migrated to lower voltage and higher current requirements.

For detector mounted electronics at the upgraded LHC DC-DC powering may be used in conjunction with serial powering or as a sole solution for module powering. As with serial powering the power delivered to the module (or a group of modules) would be at a significantly higher voltage than that used on the module and the current would be proportionally lower. At the module DC-DC converters would reduce the voltage (and increase the current) to the desired module voltage in one or two steps. Assuming a constant current density in the cable the conversion efficiency, ε, and voltage multiplication factor determines the reduction possible in cable cross section. Typically a buck converter where the energy is stored in an inductor and connected in series between the input and output terminals by a pulse width modulated switching transistor is used for the first stage voltage reduction with a power conversion efficiency of 70-90% depending on details of the construction of the convertor. It should be noted that magnetic core materials customarily used in commercial DC-DC convertors can not be used for detector mounted applications due to the high magnetic field in the detector. This limits the ratio of inductance to resistance, but does not appear to severly limit the efficiency of convertor designs. The power dissipation on the detector side is:

$$\mathbf{V_{supply} * I_{supply} = 1/\varepsilon (V_{load} * I_{load})}$$

Most of the commercially available DC-DC convertors tested have not met radiation requirements with the exception of a product by Emperion [7] which is not rated for its radiation performance.

In order to gain practical experience using DC-DC converters in an on detector environment some groups have deployed commercial devices on custom PCBs designed for tracker upgrades[8]. The importance of line filters on the cables feeding the DC-DC converters to block switching noise is shown in Figure 8 where the succeptibility of the CMS end cap tracker to EMI from a custom designed DC-DC converter is shown for various powerline filters. Clearly the pi-filter is a significant part of the EMI reduction plan.

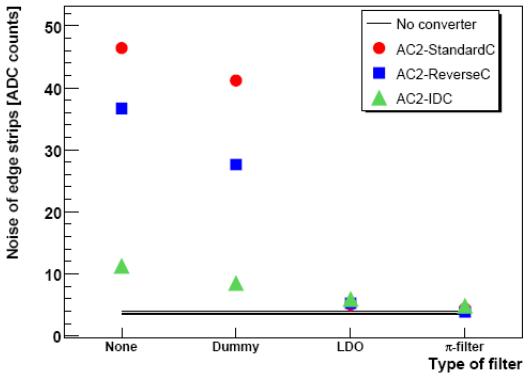

Figure 8 Succeptibility of the CMS end-cap strips to EMI from DC-DC converters used to supply power with various filter in the conductive path, pointing out the importance of line filter in the implementation of switching supplies. In the figure legend AC2 refers to a particular converter design and the colored symbols refer to filter capacitor designs: Standard surface mount (red), low inducance (blue) and interdigitated (IDC) being the best with externally accessible interdigitated contacts.

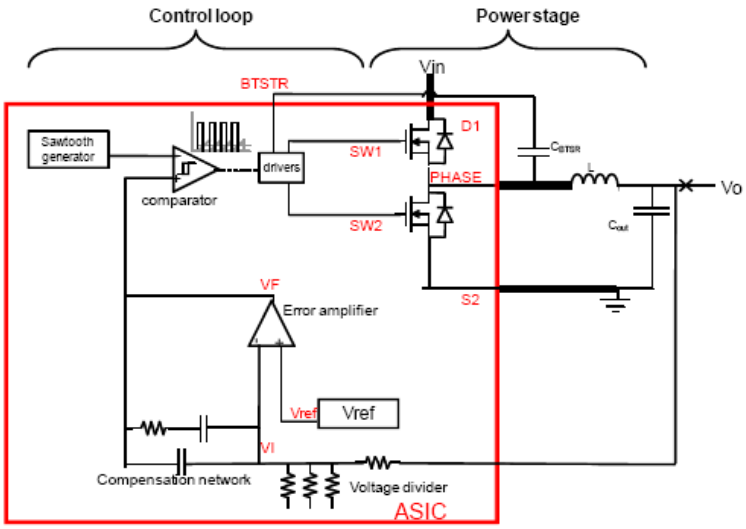

Figure 9 Basic blocks of the buck convertor circuit similar to that used in CERN's AMIS2 prototype. Components outside of the large rectangle are external to the ASIC.

Efforts focused at CERN are underway to develop a series of rad hard DC-DC convertors suitable for sLHC. Characteristics of candidate radiation tolerant transistors used to date limit the voltage and step down ratio that can be used for high efficiency conversion to less than 10 in a single conversion. A proposed design for the ATLAS silicion strip system accomplishes a factor of ~10 in voltage multiplication by using a two step approach: A first reduction of ~5 in voltage would be accomplished using a buck converter ASIC (shown in

figure 9) using a rad hard technology with an external air core inductor[3]. To keep the efficiency high with low inductance air core inductors a switching frequency of 1-3MHz is used. RF emission studies have shown that shielding around the inductor and associated components reduces EMI to satisfactory levels. Successful prototype ASICs have been designed by CERN in two different technologies AMIS HVT (AMIS 1 and AMIS 2 prototypes) and IHP SGB25V (IHP1 prototype) with an external air core inductor to deliver 2.5V to multiple modules where each front end ASIC would have a switched capacitor DC to DC converters to further reduce the voltage to that required by the analog and digital cores[9], [10].

CERN's AMIS 2 prototype has been shown to be sufficiently rad hard to be used in the LHC trackers. It remains fully functional after 300Mrad of total ionizing dose and exposure to $5X10^{15}$ protons/cm^2. Figure 10 shows change in efficiency vs input voltage for a DC-DC

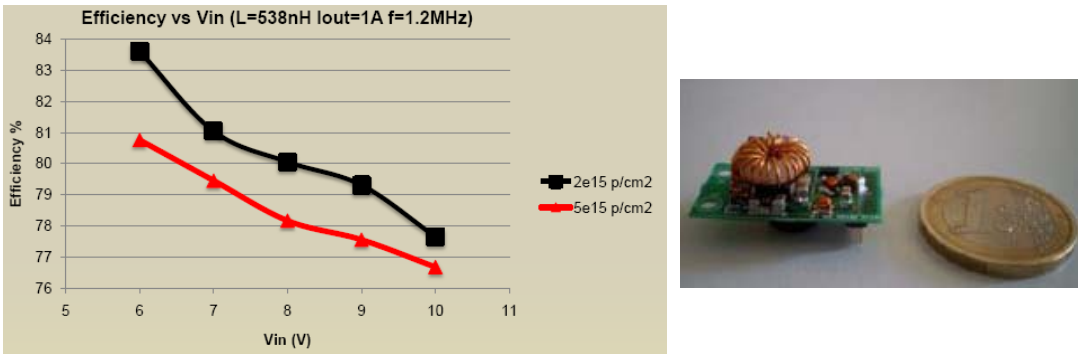

Figure 11 Efficiency vs Vinput voltage for CERN's AMIS 2 based Buck Converter (shown on the right) after exposure to 2 and 5 X 10^{15} protons /cm^2.

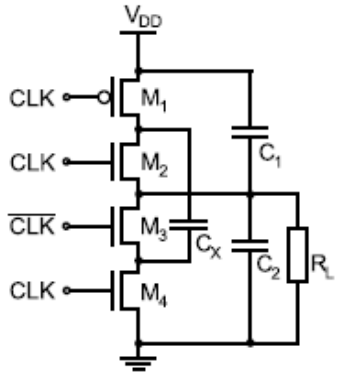

Figure 10 Block diagram of an integrated switched capacitor step down convertor. The incoming voltage (Vdd) at 2.5V is divided by two at the output across R_l .

converter using the AMIS 2 chip and a custom torroidal air core inductor (L = 538nH).

Miniature DC-DC converters designed at CERN (see figure 10 right) using AMIS 2 ASICs have been shown to produce no noticeable additional noise when attached to prototype Silicon Strip modules [11]. As mentioned above a high efficiency step down switched capacitor DC-

[3] A buck convertor uses a transistor switch to connect a higher voltage input supply to the output load through a series connected energy storing inductor. Pulse width modulation of the *on* time of the switch controls the current commuted through the inductor from the higher to lower voltage supply.

DC converter is planned to be included in each front end integrated circuit. The basic block diagram of this divide by two circuit is shown in figure 11. The step down converter is relatively simple and is expected to have an efficiency in excess of 95%. A prototype circuit that will convert incoming DC from 2.5V to 1.25V has been submitted through the CERN micro electronics group in 130nm technology and is waiting for completion of the fabrication[12].

Issues concerning DC-DC conversion for LHC tracking detectors include:

1. Development of low EMI, low mass air core inductors with minimal distortion of the local magnetic field for tracking.
2. Conducted and radiated high frequency EMI by components of switching circuitry.
3. Development of Radiation and SEU tolerant switching circuit control.
4. The complexity of the control system.
5. Failure mode of switching transistors. This is critical when the incoming DC voltage is high enough to damage the front end electronics or to short multiple modules powered by the same cable.
6. The lifetime of components and circuit blocks in the detector environmend.
7. Coupled EMI among multiple convertors during operation.

5. Conclusions

Although the final detector configurations and luminosity for the upgraded LHC have yet to be determined, a healthy program of research and development for *on detector* power conversion allowing a high input voltage for efficient power transmission from off detector supplies over low mass cables to the detector with efficient conversion to the significantly lower voltages required by a new generation of front end electronics is in progress. This work will lead to a set of verified building blocks and mature implementation techniques that will make it easier to instantiate reliable power services for the next generation of front end electronics at the LHC.

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