PROCEEDINGS OF SCIENCE

Fabrication of 3D silicon sensors

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Silicon sensors with a three-dimensional (3-D) architecture, in which the n and p electrodes penetrate through the entire substrate, have many advantages over planar silicon sensors including radiation hardness, fast time response, active edge and dual readout capabilities. The fabrication of 3D sensors is however rather complex. In recent years, there have been worldwide activities on 3D fabrication. SINTEF in collaboration with Stanford Nanofabrication Facility have successfully fabricated the original (single sided double column type) 3D detectors in two prototype runs and the third run is now on-going. This paper reports the status of this fabrication work and the resulted yield. The work of other groups such as the development of double sided 3D detectors is also briefly reported.

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1.Introduction

Many future experiments in high energy physics and X-ray imaging require fast signal response, high radiation tolerance and full area sensitivity [1]. In high radiation environments, defects are formed in the silicon lattice due to radiation damage. This leads to performance reductions, in the silicon detectors such as increase in leakage current and depletion voltage [2]. The effective drift lengths also reduce significantly. After being irradiated with a fluence of 10^{15} n/cm^2, the calculated effective drift lengths are reduced to 150 μm for electrons and 50 μm for holes at -20^{o}C [3, 4]. These drift lengths are shorter than the distance between the n and the p electrodes in a planar detector, which is approximately equal to the wafer thickness and is typically between 250 and 500 μm.

3D detectors [5], with vertical electrodes penetrating through the entire silicon substrate have drawn interest for use in high energy physics experiments and X-ray detection where radiation hardness, fast time response and active edges capability are important in terms of performances of detector systems. Because of their unique geometry, the through-wafer electrodes in 3D detectors have inter-electrode distances that are independent of the wafer thickness. This distance between the electrodes can be as short as 50 μm while keeping the overall wafer thickness to be about 250 μm for a good signal-to-noise ratio. The significantly shorter inter-electrode distance means 3D detectors have a much lower full depletion voltage and collection distance. Thus, 3D detectors can tolerate radiation damage better than planar detectors. 3D detectors also have very fast time response due to their short collection distances. Time response studies using 0.25 and 0.13 μm fast CMOS electronics [6] have shown that signals in 3D detectors can have rise times as low as 1.5 ns [7], and is limited by the readout electronics. In addition, the through-wafer electrodes can potentially be used to connect the detectors to the readout electronics via 3D stacking methods [8] once the technology has matured. Such systems result in less parasitic capacitance and inductance in the overall detector system when compared to conventional packaging methods such as wire bonding and flip chip bump-bonding, thereby reducing the signal processing time. Reduced charge sharing has also been observed in 3D detectors and is extremely beneficial in X-ray imaging applications [9].

The fabrication of 3D silicon detectors is rather complicated and requires advanced deep reactive ion etching (DRIE) and wafer bonding methods. DRIE also allows etching of through-wafer trenches, which surround the entire detector bulk. These trenches can be doped and form an ‘active edge’ electrode that is electrically active right up to the physical edge of the detector [10, 11]. The initial fabrication of 3D detectors was centred on university laboratory [12], but in recent years the development of 3D fabrication has been transferred to other fabrication facilities which offer the prospect of using 3D sensors in larger scale systems.

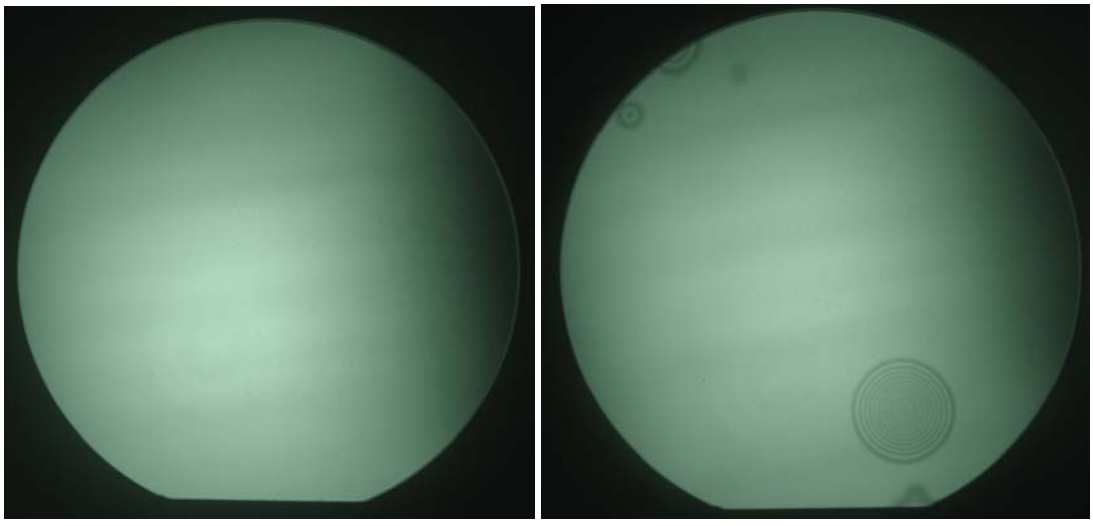
2. Fabrication of full 3D sensors with active edge at SINTEF

3D detectors were proposed by S. Parker in 1995 and active-edge 3D detectors in 1997 by C. Kenney. The first 3D detector prototypes were successfully fabricated also in 1997 [12].

Since then, many laboratories have begun research on 3D detector technology including SINTEF MiNaLab. A 3D Consortium (3DC) was set up in 2006 – a collaboration between

Stanford Nanofabrication Facility, Brunel University, the University of Hawaii and SINTEF with an aim to explore the possibility to fabricate the original 3D detectors with active edge on a small production scale. Two prototype runs have now been completed at SINTEF. By the start of the second run in 2008, the 3DC collaboration expanded, and the current members now include SLAC, SINTEF, the University of Manchester, the University of Hawaii, the University of Oslo and Purdue University. Meanwhile, a collaboration of 3D detector fabrication dedicated to the upgrade of the ATLAS IBL was set up, which includes four processing facilities, SINTEF, CNM, FBK-Trento and Stanford Nanofabrication Facility. While SINTEF and Stanford concentrate on the development of the original 3D structures, CNM and FBK-Trento have continued their development on the double-sided techniques. A brief summary on double-sided 3D devices is given in Section 6.

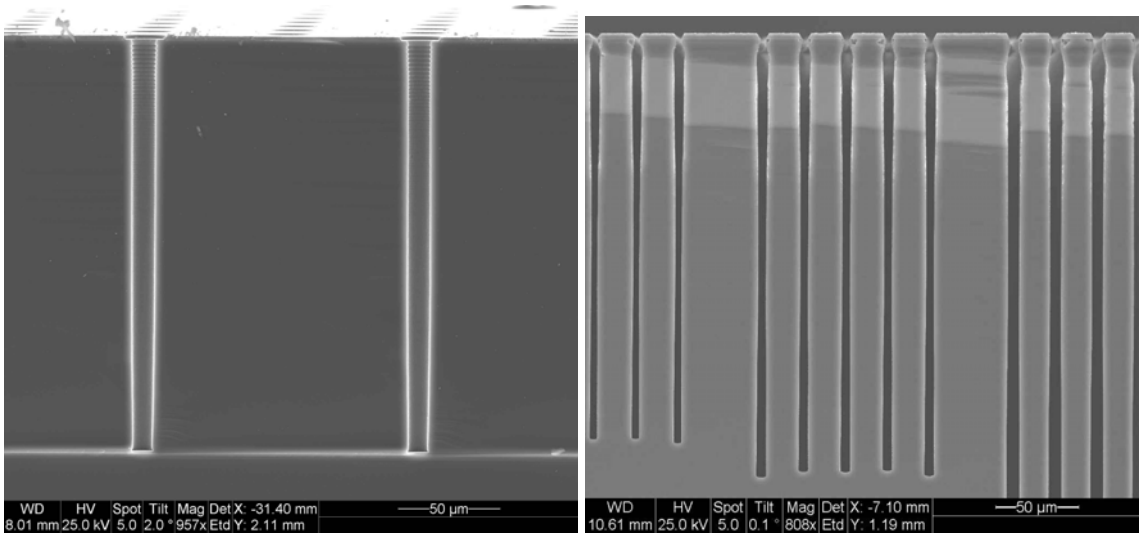
Processes in the two SINTEF runs were similar and are both adaptation of the original 3D process proposed by C. Kenney et al [12]. The SINTEF process described here refers to the second run completed in September 2009. Full details of the first run can be found in ref [13]. Twelve 200 μm thick and eight 285 μm p-type wafers with a resistivity of 10000 Ω.cm were processed. P-spray implantation on both sides was used to improve the isolation between the n-type readout pixels. A 1.5 μm thermal oxide was then grown on all process wafers and twenty 300 μm thick support wafers. Each process wafer was then bonded to the support wafer by direct fusion bonding [14]. Fig.1 shows infrared images of two bonded wafers. The first bonded wafer (Fig.1a) shows no signs of defects while the second (Fig.1b) shows several voids. The larger one is about 19 mm in diameter and 8 Newton rings deep. Voids are normally caused by small particles on either the process or support wafers which can affect the overall yield. In both the first and the second run, nearly 90% of the bonded wafers were perfectly bonded. Wafer bonding is therefore not the primary concern when considering the yield in 3D detector processing.



(a) (b)

Figure 1: Infra red images of two bonded wafers. (a) A perfectly bonded wafer with zero defects. (b) A bonded wafer with several visible voids.

After wafer bonding, a layer of 70 nm nitride was deposited, which acted as a doping barrier during both the phosphorous and boron gas phase doping. A 1.5 μm thick layer of aluminium was deposited on top of the nitride layer and used as a mask for the first DRIE process. The readout electrodes were first etched using a modified Bosch process. The diameter of the round holes on the aluminium mask was 14 μm, which became 15.5 μm in diameter after the DRIE process. An aspect ratio of 18.3 was achieved in the 285 μm thick wafers (Fig.2a) and using the same process on 5 μm trenches, an aspect ratio of about 54:1 was achieved (Fig.2b). More details of these DRIE processes can be found in ref [15].



(a) (b)

Figure 2: SEM micrographs of (a) cylindrical holes and (b) trenches after the DRIE process.

Polymer that accumulated on the wafers during the DRIE process was then removed by oxygen plasma cleaning and the aluminium mask was removed. A layer of 1 μm thick polycrystalline silicon was deposited before doping the readout electrodes by phosphorous gas phase doping using phosphorous oxychloride ($POCL_3$). The holes were then filled at Stanford Nanofabrication Facility by further polycrystalline silicon deposition. During this process, polycrystalline silicon is deposited over the surface of the wafers as well as the inside of the cylindrical holes. The excess polycrystalline silicon on the surface was removed by plasma etching. Once the n-type electrodes were completed, a 300 nm thick thermal oxide and a 70 nm thick nitride were grown and deposited as a diffusion barrier to protect the n-type electrodes during the processing of the p-type electrodes and active edges. Similar to the n-type electrodes, an aluminium mask was used for the DRIE process. The holes and trenches were then doped by boron gas phase doping using boron bromide (BBr_3) and filled by polycrystalline silicon deposition. Once the excess polycrystalline silicon was removed, the oxide and the nitride on the n-type electrodes were etched away before metallisation. A passivation layer of 0.5 μm oxide and 0.25μm nitride was then deposited by plasma-enhanced chemical vapour deposition (PECVD) and patterned.

3. Wafer yield

The overall yield is an important factor when considering the potential of 3D detectors. When a thick layer of polycrystalline silicon is deposited on the entire wafer surface, the wafer suffers from tremendous amount of stress. Wafer handling and process parameters must be planned carefully in order to avoid wafer breakage. The most critical is the polycrystalline silicon deposition itself. Polycrystalline silicon is deposited on the wafers as well as on the wafer boats which keep the wafers in place. In order to prevent the wafers becoming attached to the boats, the polycrystalline silicon is deposited in several runs, and the wafers are turned between each run. The wafers should also be separated by a gap that is significantly wider than the thickness of the wafer. In the first run, no wafer was broken and only one wafer was broken in the second run during polycrystalline silicon deposition. Despite the cost of this process, the polycrystalline silicon filling of 3D detectors is now well-established and has a good wafer yield.

A major yield problem in the first run was due to an asymmetry in the oxide thickness on the front and the back side of the wafer. The wafers then suffer from additional stress after the two polycrystalline silicon deposition. Wafer warping was observed and 16 wafers broke during the process after the second polycrystalline silicon deposition. In the second run, an extra layer of nitride was deposited on top of the thick thermal oxide. Since oxide etchants do not etch away nitride, the nitride layer acted to protect the field oxide, preventing it from becoming thinner on the front than on the back side during all RIE processes. Fig. 3 shows the wafer warping was significantly reduced in the second run. As a result, 18 wafers survived the entire process. In addition, results from lithography in the second run were significantly improved since the reduced warping allowed easier wafer-to-mask alignment.

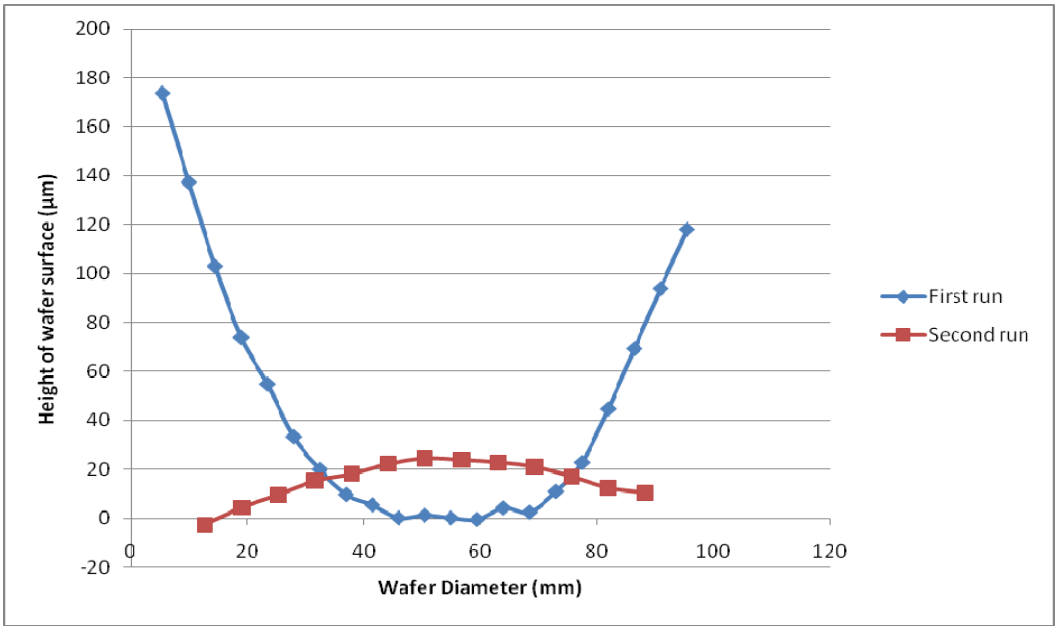


Figure 3: The curvatures of two wafers were measured. The curvature measured on a wafer from the first run was very large while the wafer from the second run was measured to be reasonably flat.

Surfaces with high topography and key holes were observed in the first run [13] after the polycrystalline silicon deposition. In the second run, the DRIE process was modified to give cylindrical profiles that are slightly narrower in the bottom. This reduced the size of keyholes in the electrodes after polycrystalline silicon deposition and in some cases keyholes and voids were entirely eliminated (Fig. 4). A smoother wafer surface with less topography was also achieved after the etching of excess polycrystalline silicon, and improved and easier lithography was achieved in subsequent steps.

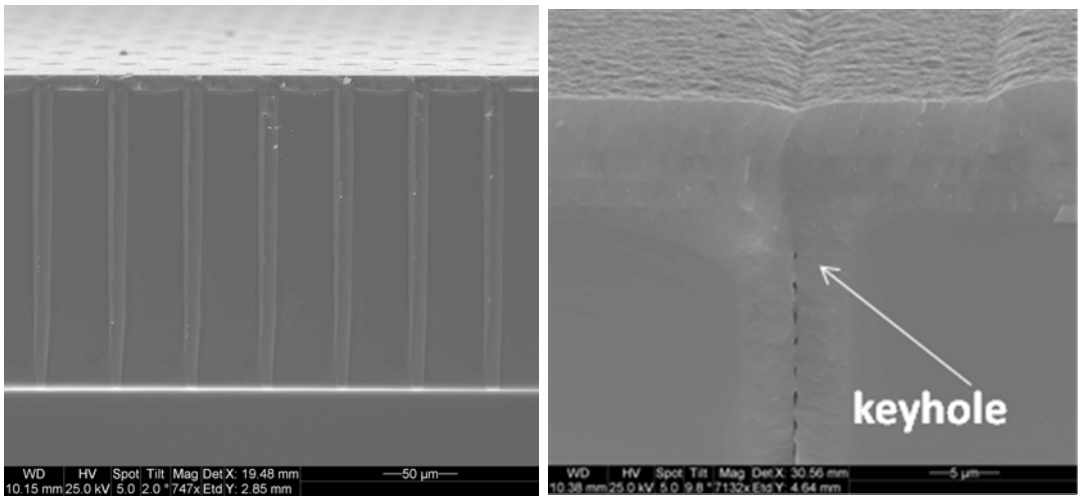


Figure 4: Cylindrical holes with 14 µm diameter (a) and 5 µm wide trenches (b) were filled with polycrystalline silicon. The cylindrical holes were completely filled with no keyholes or voids. Similarly, only a tiny gap was observed in the narrow trenches. The surface is also reasonably flat and allows easy lithography.

4. Electrical measurements

In the first run, all devices were ATLAS FE-I3 pixel devices of 2E, 3E or 4E configurations. The configuration type denotes the number of n-type electrodes in each pixel. For example, a 2E device consists of 2 n-type electrodes per pixel as shown in Fig.5. Despite the low wafer yield, good IV characteristics were measured on some ATLAS pixel devices by measuring a single pixel. Leakage current was measured to be about 1 nA per pixel with a breakdown voltage of 80 V [13].

In order to identify good devices, all pixels should be biased and measured. Probing pixels through their small passivation openings in the first run proved to be challenging. In the second run, all the pixel signal electrodes in each device were shorted together by test aluminium lines. The leakage current of an entire device was therefore measured in a single measurement. After the testing, the aluminium was stripped and the final metal mask was applied, as well as the passivation layer. The layout of the second run includes two Medipix [16] devices, two large ATLAS FE-I4 [17] 2E pixel sensors, 39 ATLAS FE-I3 [18] pixel sensors and 11 CMS pixel sensors. Fig. 6 shows the leakage current of all the ATLAS FE-I3 2E devices measured on wafer B2-14. Three devices show an early breakdown, but all other

devices showed a total device leakage current of less than 0.5 µA (0.9 x 0.9 cm^2) with a breakdown voltage between 80 and 100 V.

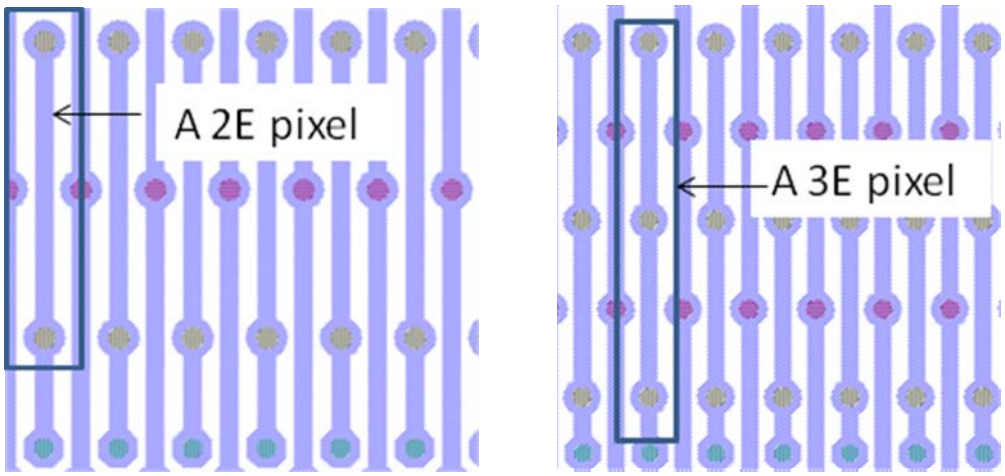


Figure 5: Layouts of sensors compatible with ATLAS FE-I3 readout chip. (a) Each pixel consists of 2 n-type readout electrodes. The two n-type electrodes (grey) are joined by a single metal line (purple) to form a 2E pixel. (b) Each pixel consists of 3 n-type readout electrodes. Similarly, 3 n-type readout electrodes (grey) are joined by a single metal (purple) to form a 3E pixel.

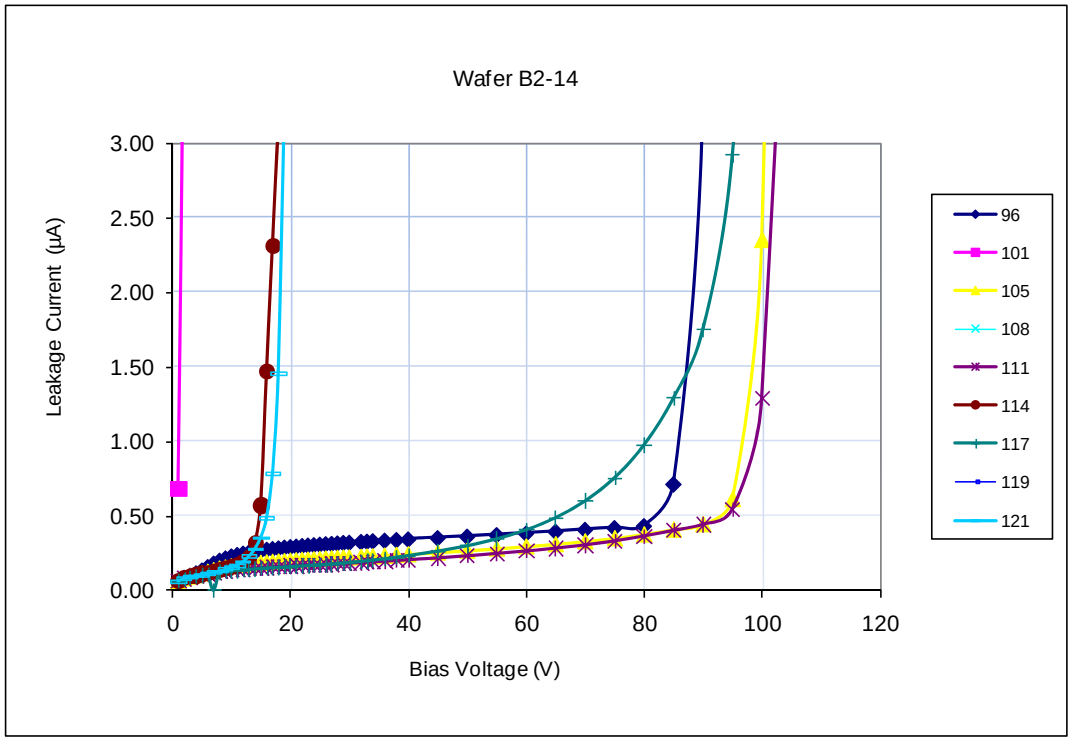


Figure 6: IV measured on all ATLAS FE-I3 2E devices from wafer B2-14. The number denotes the sensor number on the wafer.

5. Overall yield

The yield of the first run was very low due to wafer breakage and measuring all the pixels was rather difficult. The overall yield discussed here is therefore based on the results of the second run.

Devices measured with all pixels shorted with the test aluminium lines having a breakdown voltage of higher than 80 V and a leakage current of less than 2 μA at full depletion were considered to be good devices. The larger number of ATLAS FE-I3 devices on each wafer meant that some had to be placed close to the wafer edge. After the first DRIE process, it was clear that 34% of the ATLAS FE-I3 devices had electrodes not fully etched due to the wafer edge being covered by a clamp ring in the RIE process. On the contrary, only 18% of CMS devices have such electrodes, and this is reflected in the overall yield. The yield for the entire run was 32% for the ATLAS devices and 52% for the CMS devices.

None of the devices compatible with the ATLAS FE-I4 readout chip shows a good diode characteristic. However, since each wafer includes only two FE-I4 devices and one device is very close to the wafer edge, determining if a good yield is feasible for these devices was rather difficult. In addition, these devices have quite a large surface area (18.5 x 20.5 mm^2) and the larger number of pixels per detector increases the risk of having poor pixels. The overall yield of these large devices will be explored further in the next run where each wafer will include six FE-I4 devices, all located in the centre of the wafer. The new run will also include some process modifications in order to reduce damages in the single crystalline silicon when removing the excess polycrystalline silicon during plasma etching. The modifications should improve the device's performance, for example, lower leakage current at full depletion and higher breakdown voltage.

6. Other recent 3D fabrication activities

As mentioned earlier, 3D fabrication is rather complicated and integrating the doping process of both n and p-type electrodes from the same side of the wafer can be challenging. Several alternative 3D architectures have been proposed with the aim of simplifying the fabrication process. Some alternatives have been shown to be rather ineffective in charge collection, such as the single sided single type columns or semi-3D [19], where one electrode type consists of columns and the other electrode type is a planar electrode that is implanted on the back side of the wafer.

A promising alternative is the double sided double type columns (3D-DDTC) [20, 21]. This approach has been developed by both FBK-Trento and CNM in Barcelona, with each institute having their own design and processing preferences. In this architecture, the n-type electrodes are processed from the front side while the p-type electrodes are fabricated from the back side, allowing easier masking, DRIE and doping processes. FBK-Trento initially started their 3D activity on single sided single type devices [22, 23] but has now successfully fabricated 3D-DDTC. Enhanced performances have been shown in the second prototype run completed in 2009 [24]. CNM in collaboration with the University of Glasgow have also shown promising

results in 3D-DDTC processing [21]. Currently, these electrodes do not penetrate the entire substrate. The wafer can therefore withstand higher mechanical stresses and bonding to a support wafer is not necessary. Both CNM and FBK-Trento are now moving towards through-wafer electrodes, similar to the original 3D sensors within the framework of the ATLAS 3D R&D program.

7. Conclusions

A second prototype run of full 3D detectors with active edge has been successfully completed at SINTEF in September 2009. Several process parameters were modified with respect to the first prototype run in 2008 and the resulting wafer yield dramatically increased. However, the overall yield of both the ATLAS and CMS devices is still rather low and this problem will be addressed further in the third prototype run where further process modifications will be made. Additional process steps such as removal of the support wafers and using DRIE instead of a dicing saw to separate the devices will also be tested. Completed devices from the second run are currently being tested by both the CMS readout electronics and the ATLAS FE-I3 readout chips. Other groups working on 3D-DDTC have also completed several prototype runs with promising results.

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