PROCEEDINGS OF SCIENCE

Monolithic Active Pixel Matrix with Binary Counters (MAMBO III) ASIC

Farah Khalid[1]
Fermi National Accelerator Laboratory
P.O.Box 500, Kirk Road & Pine Street, Batavia, IL 60510, USA
E-mail: farah@fnal.gov

Grzegorz Deptuch
Fermi National Accelerator Laboratory
P.O.Box 500, Kirk Road & Pine Street, Batavia, IL 60510, USA
E-mail: deptuch@fnal.gov

Alpana Shenai
Fermi National Accelerator Laboratory
P.O.Box 500, Kirk Road & Pine Street, Batavia, IL 60510, USA
E-mail: farah@fnal.gov

Raymond Yarema
Fermi National Accelerator Laboratory
P.O.Box 500, Kirk Road & Pine Street, Batavia, IL 60510, USA
E-mail: deptuch@fnal.gov

Monolithic **A**ctive **M**atrix with **B**inary C**o**unters (MAMBO) III 3D ASIC has been designed for detecting and measuring low energy X-rays from 6-12keV. The top ASIC consists of a matrix of 44×44 pixels, each of 100x100μm^2. Each pixel contains analogue functionality implemented with a charge preamplifier, CR-RC^2 shaper and a baseline restorer. It also contains a window comparator with Upper and Lower thresholds which can be individually trimmed by 4 bit DACs to remove systematic offsets. The hits are registered by a 12 bit counter which is reconfigured as a shift register to serially output the data from the entire ASIC. The bottom ASIC contains gated diodes which can be controlled to improve pixel isolation and leakage current. It contains a small p-plus region with a large buried P-well (BPW), almost the same size as the pixel to obtain a parallel electric field in active volume and avoid potential pockets. It is also effectively shielded to electrically isolate the detector from the electronics. The T-Micro 3D integration process is used to bond the detector in the lower tier to the electronics in the upper tier. The ASICs have been manufactured by OKI, they are being 3D bonded at T-Micro.

[1] Speaker

PROCEEDINGS OF SCIENCE

19th International Workshop on Vertex Detectors - VERTEX 2010
Loch Lomond, Scotland, UK
June 06 – 11 2010

1.Introduction

Silicon on Insulator (SOI) technology allows detector and ASIC form factors that are indistinguishable from monolithic structures, like MAPS. In comparison to MAPS, a SOI detector may offer extended functionalities, but in order to achieve this goal, the standard SOI process must be enhanced, requiring features such as, through buried oxide (BOX) contacts and implantation of the handle wafer. Combining the detector with the signal processing electronics in each pixel is possible using the OKI SOI process available through the SOIPIX collaboration led by KEK. A fully depleted (FD) CMOS SOI 0.2 µm process is the base for this development. Multiple designs realized by the members of the SOIPIX collaboration on consecutive multi-projects-wafer (MPW) runs assessed detection properties, which has lead to maturing designs of SOI electronics but highlighted some undesirable effects of intra-structure couplings and charge collection anomalies. Fermilab has pursued designs of pixel detectors with complete in-pixel processing chain for imaging and some tests structures to explore the properties of the available process. The detailed tests led to the conclusion that the process has problems related to direct capacitive coupling between the detector and electronics.

2. ASIC top level

The Monolithic Active Matrix with Binary Counters (MAMBO) ASIC has been designed for detecting and measuring low energy X-Rays from 6keV – 12keV for applications such as autoradiography and fluorescence X-Ray spectroscopy. The MAMBO prototypes submitted in 2006 and 2008 allowed assessment of the correct functionality of the processing electronics and detection of signals originating from conversions of low-energy X-rays in the bulk. The new MAMBO III prototype was designed using advanced features of the SOI technology and targeting exploration of the Au/In + adhesive underfill 3D bonding process offered by T-Micro (formerly ZyCube). The device was divided into two tiers, the top tier, comprising the electronics and the bottom tier, consisting of an array of detector diodes.

The MAMBO III top ASIC is 5mm x 5mm in dimension, it contains a matrix of 44×44 pixels, each 100x100µm^2 in size.

3. In-Pixel Electronics

Each pixel contains analogue functionality accomplished by a charge preamplifier, CR-RC^2 shaper and a baseline restorer.

The preamplifier and shaper both use a regulated cascode design to achieve a high open loop gain. Cascoding is particularly important in deep submicron processes because of channel conductances, $g_{ds,}$ being typically higher than for older processes. The resultant low dynamic resistance, below 1MΩ, does not allow for high voltage gain. The preamplifier uses a 5fF feedback capacitance and an active transistor feedback resistance of 28MΩ. The transconductance gm of the input transistor is equal to 6.5µS. A test capacitance of 1.7fF is connected at the input of the preamplifier for analog calibration independently of the detector signal.

The pixel also contains a window comparator with upper and lower thresholds which can be individually trimmed by 4 bit current steering DACs to remove systematic offsets. The window comparator consists of two hysteresis comparators and double discriminator logic (DDL). If the output of the shaper is within the upper and lower threshold it is counted as a hit, all other signals are discarded. The hits are registered by a 12 bit counter which is reconfigured as a shift register to serially output the data from the entire ASIC. The pixel contains an analogue and a digital buffer which can be enabled for single pixel tests. It also contains a configuration register, which controls various testing modes and can be used to disable the pixel. The pixel block diagram is shown in Figure 1; the pixel layout is shown in Figure 2.

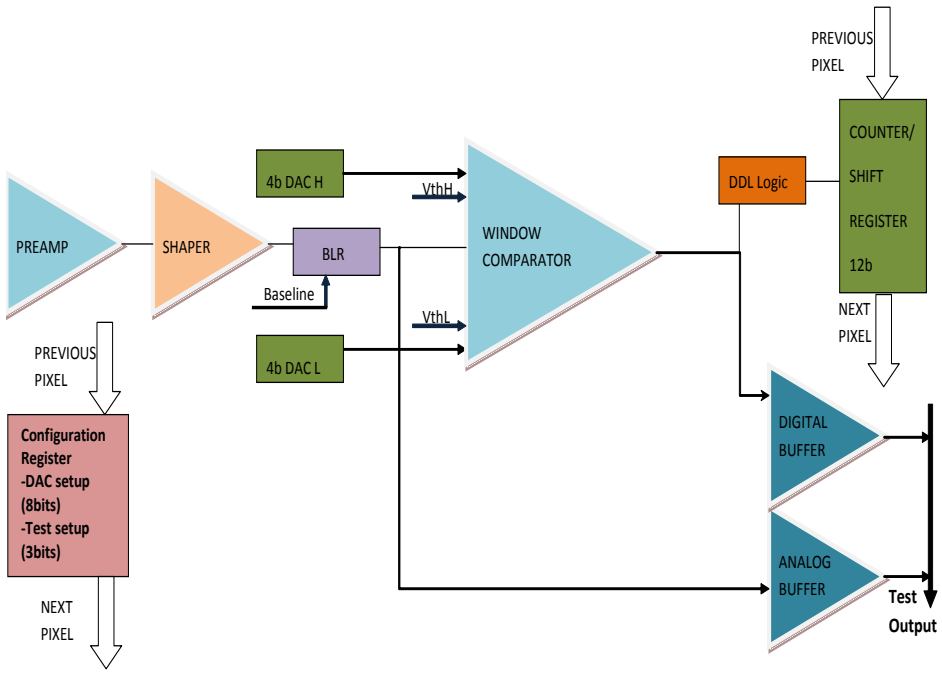

Figure 1. Pixel Block diagram

MAMBO 3 is a prototype ASIC, the layout of the pixel has not been optimised for smallest area. The goal of the ASIC is to perform pixel by pixel analysis of both analogue and digital functionality to gain independent performance statistics. 25% of the pixel is occupied by test buffers. The design also uses a binary ripple counter rather than a pseudo random counter to avoid complex analysis of the output data during tests. The switches used for reconfiguring the counter to the shift register mode further increase the area of the pixel. Differential flipflops are used for both counter and configuration registers to reduce noise coupling between the closely placed analogue and digital sections, which again results in a larger area. The transistor count per pixel is approximately 1000. In the final ASIC once the electronics has been completely characterised for the OKI 0.2µm SOI process, the area of the pixel can be reduced atleast by a factor of 3 to 4 by eliminating the test buffers and using a pseudo random shiftregister.

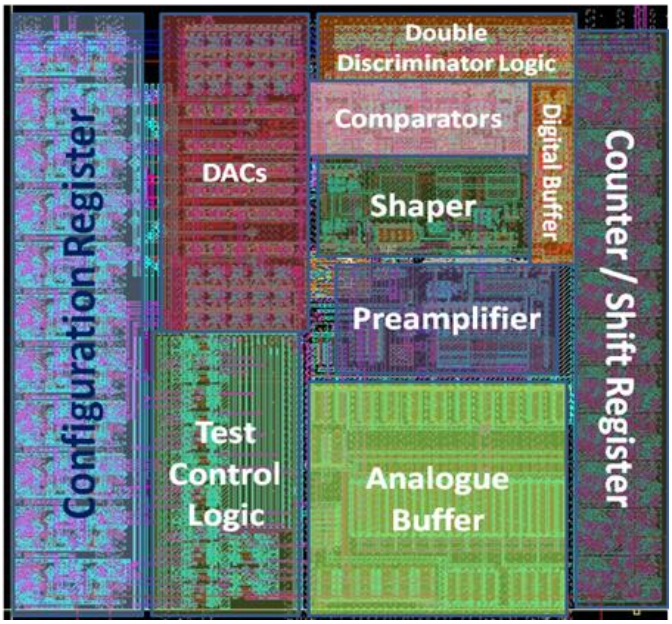

Figure 2. Pixel Layout

The MAMBO III bottom ASIC contains gated diodes which can be controlled to improve performance such as leakage current. The dimensions and pixel matrix size and number of cells matches the top ASIC. Each pixel contains a small p-plus region with a large buried P-well (BPW), almost the same size as the pixel to obtain a parallel electric field in active volume and avoid any potential pockets that may alter charge transport. The diode is covered with metal1, by controlling the voltage of the metal1 layer the performance of the diode such as inter-pixel separation and leakage current can be controlled. The layout of the pixel is shown in Figure 3.

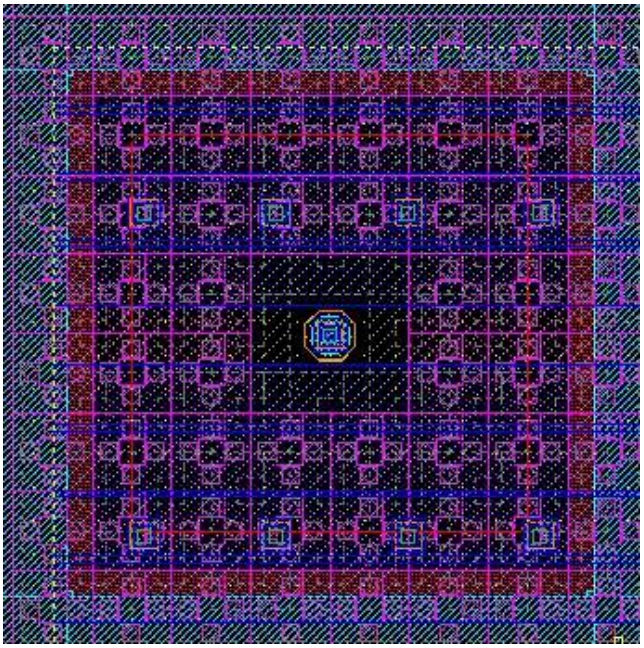

Figure 3. Bottom pixel layout

Implants are connected to the pads on the surface of the chip using through-BOX contacts. The detector is also effectively shielded, using available process metals, to electrically isolate the detector from the electronics. The pixel matrix is surrounded by four guard-rings. Three Inner P type guard rings and one outer N type guard ring. The guard rings stabilize the electric fields outside the pixel matrix in the periphery of the ASIC, which helps to reduce edge leakage currents. The rings are connected to pads on the top ASIC through 3D bump bond connections.

4. Simulation

The Figure 4 shows the simulation output of the various blocks in the pixel. The simulations are performed for an input change of 2000h+. Analogue simulation results are summarized in Table1. The sensitivity at the output of the shaper is 100mV for every 1000h+ at the input. The response saturated for larger charge signals.

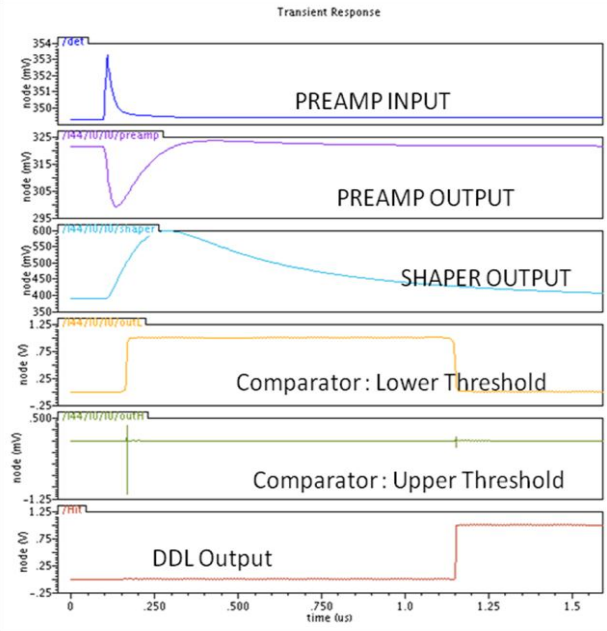

Figure 4. Simulation results

Table 1 MAMBO 3 Simulation Results

Input Range	From 500h+ to 4,000h+ for positive polarity detector p-on-n
Sensitivity	100mV/1000h+ for small signals
Shaping Time	200ns
Leakage current tolerance	Up to 200pA (realistic values are expected not to exceed single pA)
Noise	ENC ~ 80 e-
Power dissipation per pixel	2.7µW

5. 3D Integration

The T-Micro 3D integration process is used to bond the detector in the lower tier to the electronics in the upper tier. This separates the functions of charge generation and charge processing to two SOI layers, thus, eliminating the direct coupling paths. Each pixel has 11 connections, one diode connection from the bottom pixel to the preamplifier in the top pixel. The 10 dummy connections are added to increase the bonding density to satisfy process requirements for better yield. The conceptual diagram of the 3D connection between the two pixels is shown in Figure 5. Each 3D microbump is 2µm x2µm in size; each pixel has a microbump density of 0.4%. The 3D bonding process requires mechanical rigidity which is enhanced by using more contacts between the two ASICs.

The bottom ASIC does not have any pads. All connections are made using the micro bump bonds to the top ASIC.

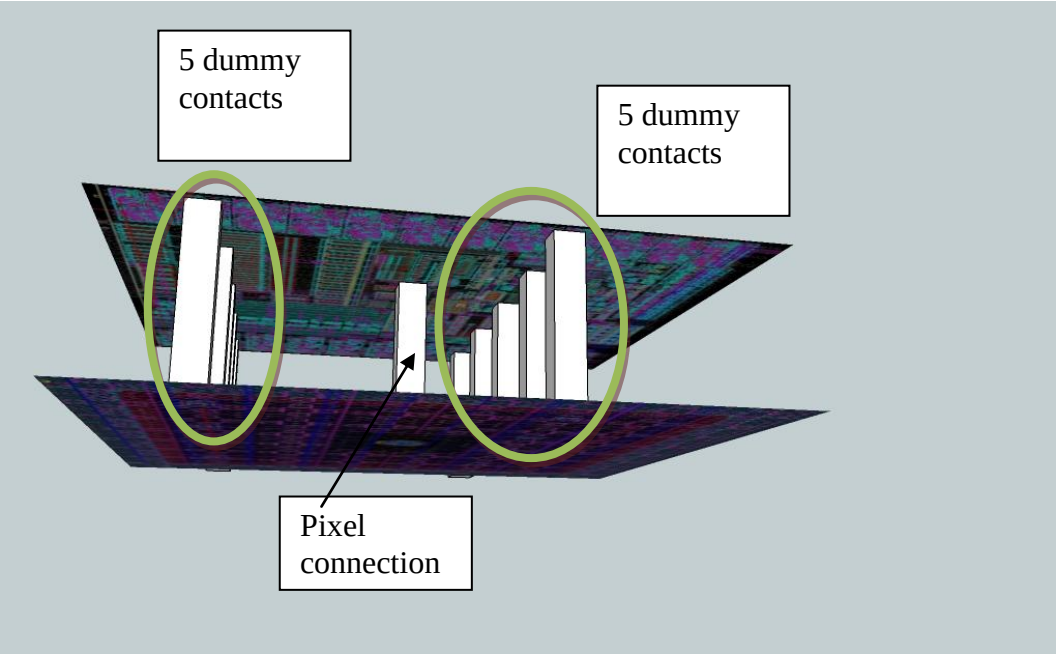

Figure 5. Conceptual diagram of the 3D bonded pixel

The top ASIC is back thinned. The silicon handle part is removed and through-BOX contacts, inserted at the fabrication of the wafer, are exposed. By depositing and patterning metal on the back, all the pads are available on the surface. The through BOX contacts provide electrical connections to the post-processed pads on the surface as shown in Figure 6. After the handle part of the wafer is removed the transistors and sensitive nodes are exposed to electrical couplings through a buried oxide (BOX) layer of 200nm from external environment. Hence the back metal is used as a shield to protect the transistors, as shown in Figure 6 and Figure 7.

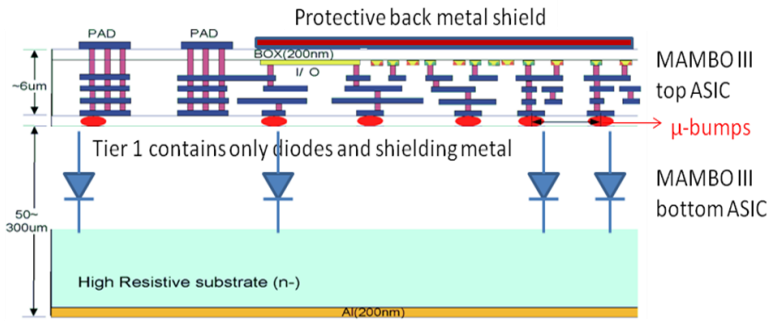

Figure 6. Cross sectional view of 3D bonded ASICs

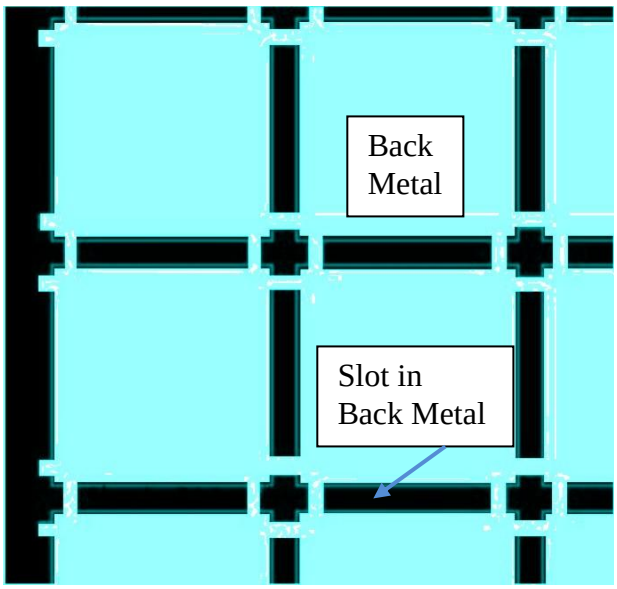

Figure 7. Shielding per pixel using back metal

6. Conclusions

The exploration of the T-Micro bonding that became available on the last run was seized as a very attractive opportunity to complete the portfolio of the explored 3D bonding processes at Fermilab in the focus of the 3D-IC development. OKI has completed the manufacture of the 2D ASICs, the 3D assembly is currently being undertaken by T-Micro, processing is expected to be completed by mid-October. The 2D ASICs cannot be tested as the PAD opening is on the back metal which is deposited after the 3D assembly.

Introduction of nested wells (BPW and BNW) has recently been agreed, thus efficient shielding of the detector and electronics will become available on the process. BPW (Buried P-Well) is the charge collecting electrode, is placed underneath an BNW (Buried N-well) layer which is connected to AC-ground. The nested well structure effectively screens capacitive coupling between the diode and the electronics and will also create a homogenous electric field through the entire detector volume. The minimum detectable charge of the pixel is related to the

minimum settable threshold voltage of the comparators, which is ideally defined by the electronic noise of the system. However various interferences result in increasing the threshold values further. It is envisaged that the nested well structure could shield the parasitic interferences between the pixel electronics and the detector. With the inclusion of nested wells, a successive submission of MAMBO IV was accomplished to integrate back the detector and electronics in a single tier. This will enable us to once again exploit the advantages of the SOI process with a monolithic combination of the detector and electronics, having eliminated its negative impacts. The advantages offered by this type of detector over currently available hybrid detector systems include eliminating the need for bump bonding, resulting in a fully monolithic compact device with simple processing.

References

[1] Deptuch, G. "Monolithic Pixel Detectors in deep submicron SOI process", NIM A (2009)

[2] SOIPIX collaboration: http://rd.kek.jp/project/SOI/

[3] Motoyoshi, M., Kamibayashi, K. Bonkohara, M. and Koyonagi, M., "Current and future 3 dimensional LSI technologies" , Technical Digest of the Intenational 3D system integration conference (2007)