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Recent results and plans of the 3D IC consortium

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Vertical integration technologies are very promising in view of the demanding requirements set by the future High Energy Physics (HEP) experiments at particle accelerators. In these applications silicon pixel sensors will be required to integrate advanced functionalities and to have low mass and small pitch. This paper presents the activities of the 3D IC consortium and describes the designs submitted in the first multi-project (MPW) run taking advantage of a homogeneous vertical integration technology.

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[1] Speaker

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1. Introduction

Continuous scaling of VLSI circuits is dramatically increasing the cost of productions. Each new generation requires a capital investment of several billion dollars for enormously complex fabrication systems, which have a short useful lifetime since the next generation of advanced technology is typically only a few years away. Moreover this trend is rapidly increasing the impact of interconnection delays and in particular performance improvements beyond 130nm technology node is begin to saturate. Three-dimensional integrated circuits (3D-ICs) offer the ability to reduce the interconnection length, parasitic R, L and C, improve power efficiency without shrinking transistor size. As CMOS scaling slows down 3D-ICs are worldwide considered the best way for carrying ICs further along the path of Moore's Law.

3D integrated circuits will also play a critical role in the development of new detectors, in particular if heterogeneous integration is considered. In this case two or more different technologies can be independently optimized for the different layers of a 3D vertically integrated device (e.g., nanoscale CMOS for digital circuits and high speed SiGe BiCMOS for a fast analog front-end, or non-Si material on top of a readout circuit for X-ray or infrared detectors). Furthermore, thanks to the technologies associated to 3D processing, it is possible to thin devices to less than 50um complying with demanding material budget requirements.

The development of 3D integrated circuits is a challenge for high energy physics applications and for scientific applications in general. The cost can be very high for small research institutions in the R&D phase. To cope with the cost of engineering runs and to share efforts and experience in the design of vertically integrated devices, the high energy physics community has organized itself in a worldwide consortium among research institutions. In late 2008 a large number of international laboratories and universities with interest in high energy physics formed a consortium, promoted by Fermi National Accelerator Laboratory, to explore various issues associated to vertical integration [1]. This international consortium is now comprised of 17 institutions from 7 countries. There are numerous benefits related to this association: sharing of the designs, development of special software programs, development of libraries and test structures, design review, frequent meetings and cost reduction.

2. Chartered-Tezzaron process

Three dimensional circuits can be expensive to fabricate. Each tier in a 3D circuit generally comes from a separate dedicated run. Thus the cost is roughly proportional to the number of tiers plus bonding between each of the tiers. If wafer-to-wafer bonding is used, the yield will be lower resulting in a further increase in cost. In the first MPW run, to reduce costs, only one set of masks has been used for both the top and bottom layers of the 3D circuits [2]. For the face-to-face bond, as shown in Figure 1, one wafer is flipped horizontally and thinned after bonding. Designs up to 5.5x6.3mm^2 in area have been accommodated into the 26x30 mm^2 frame.

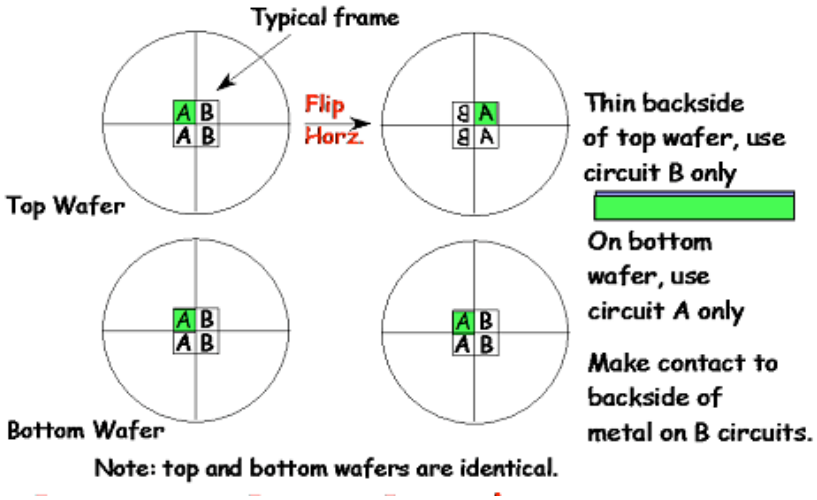

Figure 1: two tier 3D IC obtained from one set of masks. The two tiers are face-to-face bonded.

For the first MPW run the consortium decided to investigate 3D devices based on two layers, also called tiers, of the 130nm CMOS technology by Chartered Semiconductor [3], vertically integrated with the Tezzaron interconnection technology [4]. Tezzaron is a leader in 3D technology and has built 3D devices for imaging, memory stacking, FPGAs and microprocessors. The wafers are fabricated by Chartered in Singapore where the 3D assembly is completed by Tezzaron. Chartered Semiconductor, now subsidiary company of GlobalFoundries, is one of the world's top semiconductor foundries with an extensive line of CMOS and SOI processes down to 28nm. Chartered has fabricated more than one million of eight inch wafers in the 130nm process and data demonstrate consistent high yield. Chartered is working to extend TSV processes to 300mm wafers and 45nm technology. The 130nm process is well suited to analog circuits design offering deep N-wells (DNW), MiM capacitors, multiple threshold voltage transistors. Among the options available in the Chartered technology, the low power (1.5V supply voltage) transistor option was chosen. The technology also provides 6 metal layers (including two top, thick metals), dual gate options (3.3V I/O transistors) and N- and P-channel devices with multiple threshold voltage [3]. In the Tezzaron-Chartered process, wafers are face-to-face bonded by means of thermo compression techniques. Bond pads on each wafer are laid out on the copper top metal layer and provide the electrical contacts between devices integrated in the two layers. The top tier is thinned down to about 12um to expose the through silicon via (TSV), therefore making connection to the buried circuits possible. Furthermore, to allow the possibility of testing each tier separately, I/O pads for bonding or for probe testing can be reformed above metal 6 (layer used for the face-to-face bonding). This possibility is given by adding a particular metal layer called RDL (Re-Distribution Layer). These wafers are for 2D testing and therefore are lost for 3D interconnections.

The through silicon vias (TSVs) may be added as the last step after wafer bonding (process also called "via last") in the areas free of active devices or may be an integral part of the foundry process, being formed before ("via first") or after Front End Of Line (FEOL) processing ("via middle"). The Tezzaron 3D process is a "via middle" process since TSVs are formed after

FEOL processing as shown in Figure 2. The vias are only 6 microns deep. Figures 2-7 show the Tezzaron's stacking method based on two layers used in the first MPW run [5].

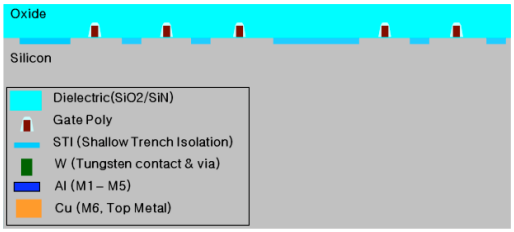

Figure 2: cross section of the wafer after transistors have been created but before contact metal. The Tezzaron 3D process is a "via middle" process since TSVs are formed after FEOL processing.

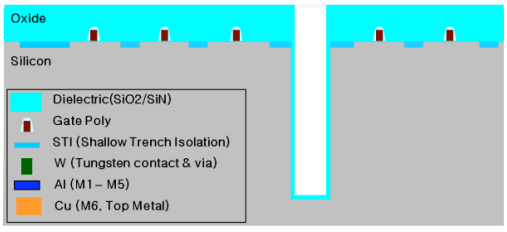

Figure 3: the through silicon via is etched through the oxide and into the silicon substrate.

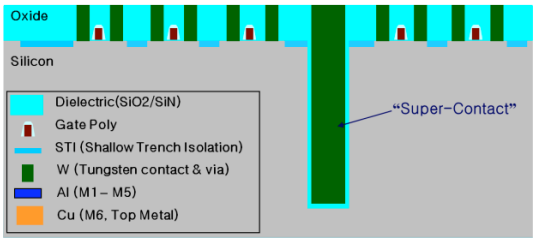

Figure 4: the TSV is filled with tungsten and finished with chemical-mechanical polishing (CMP).

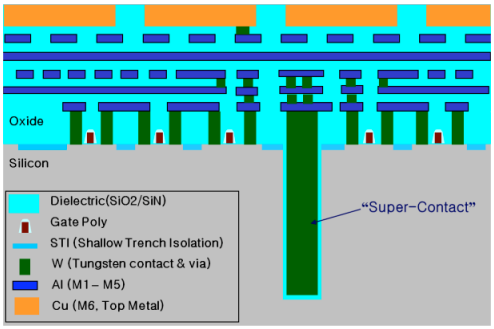

Figure 5: the wafer is finished with its normal processing (FEOL processing), which can include a combination of aluminum and copper wiring layers. The last layer, used for wafer-to-wafer connection, must be copper.

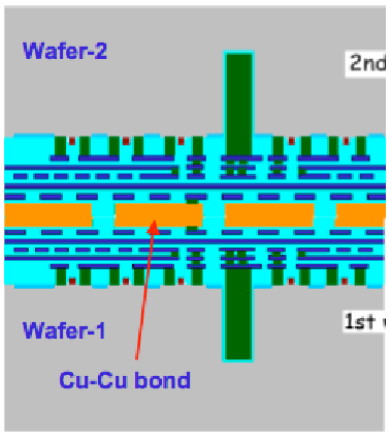

Figure 6: the wafers are aligned and bonded in a copper thermal diffusion process.

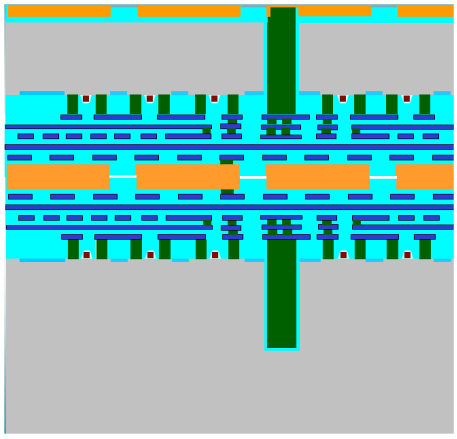

Figure 7: after bonding the top wafer is thinned to the bottom of the TSVs. The backside of the thinned wafer is covered by an oxide, then a single damascene copper process creates bonding pads for subsequent stacking or wire bonding as in the MPW run.

After complete processing of each layer, the height of the total stack increases by about 15um per wafer. Tezzaron has created stacks of up to four wafers and intends to manufacture five-layer devices in the next years, but there is no fundamental limit on the number of layers that this method can incorporate.

3. Design submitted in the first MPW run

The first multi project run should allow for evaluation of many elements and establish guidelines for future submissions. In particular the goals of this run are:

- Evaluate the Chartered process (planar technology)
  - Suitability of the process for Monolithic Active Pixel Sensors (MAPS)
  - Noise performance and radiation tolerance
  - Performance of a large number of different circuits exploring many different operating conditions
- Evaluation of the 3D processing
  - Effect of thinning and bonding process on device performance
  - Yield of the bond connections between tiers and of the TSV
  - TSV parasitic effects on the device performance
  - Digital coupling between the two tiers.

The circuits designed cover a wide range of applications: ATLAS pixel upgrade, CMS silicon strip, ILC vertex detector, charged particle tracking at the SuperB Factory, X-ray imaging. A lot of test structures for characterizing the technology from the standpoint of radiation tolerance, bond and vias reliability, TSV parasitic effects on the device performance, single event upset tolerance, cryogenic operation. As shown in Figure 8, the full frame layout has been divided into 12 reticules among the consortium members. The main characteristics of the design submitted are summarized in the following subsections.

- **Subreticule A** – This subreticule includes two subcircuits to be bonded to sensors from XFAB (0.35um with high resistivity epitaxial layer). An amplifier may be integrated in each pixel sensor. The first subcircuit is designed by IPHC Strasbourg and IRFU Saclay for ILC applications. It is a rolling shutter, low power pixel tracker composed of 34x240 array of 20um pitch pixels [6]. In the analog tier, a charge amplifier, a discriminator and a latch, are integrated in each pixel. The digital tier includes a 1 bit memory and the readout electronics. The second subcircuit is designed by IPHC Strasbourg and Universities of Bergamo and Pavia. It is a self triggering pixel tracker composed of a 245x245 array of 20um pitch pixels with fast X-Y projection readout [7].

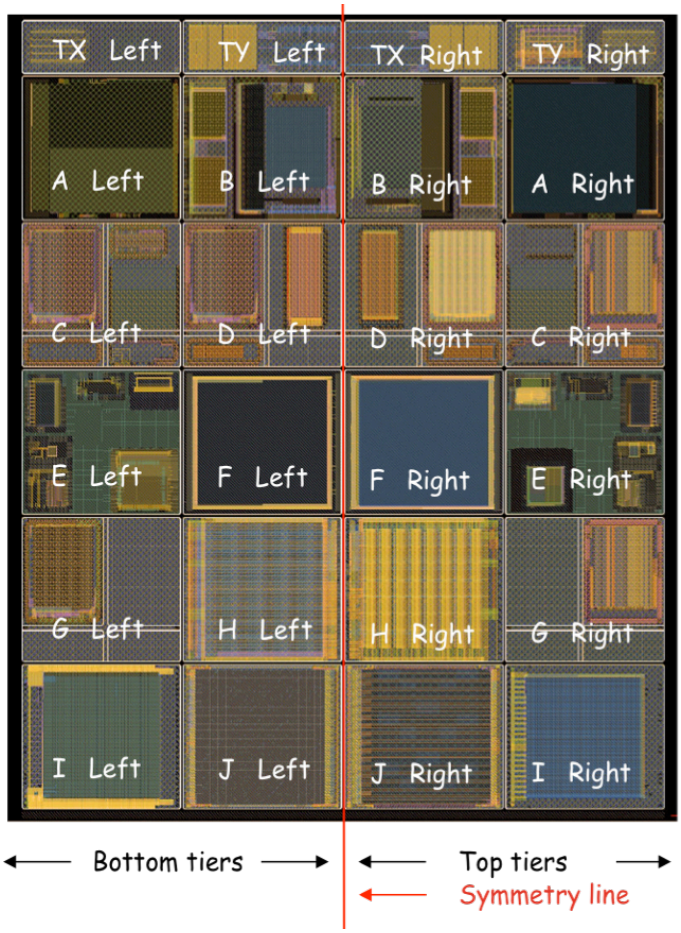

Figure 8: full frame layout of the first MPW run.

- **Subreticule B** – This subreticule includes three subcircuits. The first subcircuit, designed by IPHC Strasbourg and IRFU Saclay, is a 34x240 array of 20um pitch monolithic active pixel sensors (MAPS) for ILC application operating in rolling shutter mode, 80ns/row. The analog tier includes amplifier and discriminator with only NMOS transistors, in the digital tier there are 1 bit memory and the readout electronics. The second subcircuit, designed by IPHC Strasbourg is a 128x192 MAPS array, 12x24um pitch pixel with 5 bit time stamp, second hit marker, full serial readout for ILC applications [8]. The future goal of this architecture is to use a separate sensor tier for reducing the pixel size to 12x12um. The third subcircuit is composed of two separate memory cores: one standard design and one with built-in single event latchup (SEL) hardness circuitry designed by the Circuit Multi Project design team (CMP).

- **Subreticule C** – This subreticules includes four subcircuits. The first subcircuit, designed by CPPM Marseille and Bonn University, is a planar 2D pixel detector based on earlier design in IBM 0.13um (FEI4) for the ATLAS pixel detector [9]. The second, third and fourth subcircuit have been designed

by CPPM Marseille and include a 14 columns, 60 rows, 50x166um pitch pixels with simple readout, SEU resistant register and TSV/bond interface daisy chain to measure TSV as well as bond yield; a test structure to evaluate transistor performance with TSVs in close proximity; and test structure to measure robustness of circuits under wire bond pads.

- **Subreticule D** – This subreticule includes three subcircuits. The first one includes a 3D front-end pixel design foreseen for ATLAS pixel upgrade. In the analog tier a 14 columns, 60 rows, 50x166um pitch pixels (same as subreticule C) has been included, and the digital tier contains special features such as time stamp, time over threshold, and 4 pixel grouping [10]. The second subcircuit, designed by LAL Orsay, includes a small pixel 24x64 array of 50 um pitch for Super LHC, threshold adjustment DAC/pixel, 24 DFF register/pixel [11]. The third subcircuit is a TSV capacitance test circuit designed by CPPM.

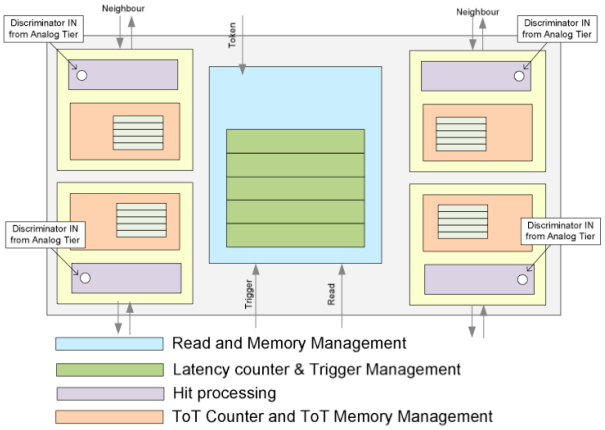

Figure 9: the 4-pixel regional digital logic of the FE-TC4-DC chip [9].

- **Subreticule E** – This subreticule includes seven subcircuits:
  - a 32x64 3D MAPS array of 25um pitch with correlated double sampling technique, three-transistors front-end, discriminator and auto-zeroing in the digital tier and all the control logics in the digital tier. The two tiers have been designed by INFN Roma3;
  - INFN Roma3 also designed planar 2D small matrices with 10 and 20 um pixels to test signal to noise performance of MAPS in the Chartered process;
  - 8x32 3D MAPS matrix of 40um pitch pixels, deep N-well sensors (DNW) and data push architecture designed by Universities of Pavia and Bergamo, INFN Pisa and INFN Bologna [12,13];
  - a 3D MAPS test structure with two 3x3 40um pitch arrays. One is designed with enclosed layout transistor input devices (designed by Pavia/Bergamo/Pisa);

- two test structures for the subreticule F DNW MAPS device (Pavia/Bergamo): small matrices, 20um pitch;
- a planar 2D version of 3D MAPS device of subreticule F DNW MAPS device: 64x64 array of 28 um pixels (Pavia/Bergamo);
- two 3D test structures designed by INFN Perugia [14].

- **Subreticule F** – This subreticule includes 3D MAPS device with 256x240 array of 20um pixels with DNW sensors and sparsified readout. The device may be tested with both a full thickness sensor substrate (for ILC applications) or with sensor thinned to 6 microns (for bio-medial imaging) [15,16]. Figure 10 shows how a deep N-well MAPS may evolve from a standard two-dimensional CMOS implementation to a 3D vertically integrated two-tier device;

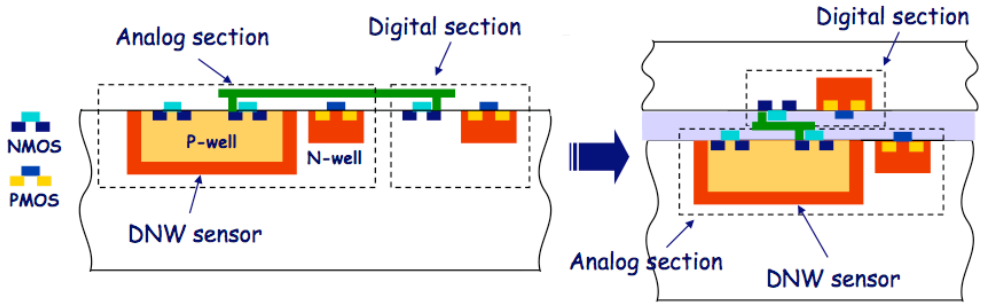

Figure 10: conceptual evolution of a MAPS device with deep N-well sensing electrodes from a 2D standard CMOS technology to a 3D vertically integrated structure.

- **Subreticule G** – This subreticule includes two subcircuits designed by LBNL and LAL Orsay. The first circuit is a planar 2D version of the ATLAS FEI4 chip based on earlier design in IBM 0.13um technology. The second circuit includes a similar design as one integrated in chip C1. This circuit is designed for an opposite polarity input signal.

- **Subreticule H** – This subreticule, designed by FNAL, CPPM and LBNL, includes a 3D chip (VICTR) used as a demonstrator toward developing a Level 1 trigger for Super CMS using sensors pairs [17]. To identify hits with pt above 2GeV, two 80um pitch sensor barrels, one with long silicon strips and the other with short strip are separated by 1mm interposer, as shown in Figure 11. A hit in a long strip gives phi information and a hit on the shorter strip gives Z information. The chip collects hits from both sensors and finds hit pairs with pt above 2GeV by means of a coincidence circuit. The chip is only 24um thick and by means of top and bottom connections is mounted between the interposer and bottom sensors.

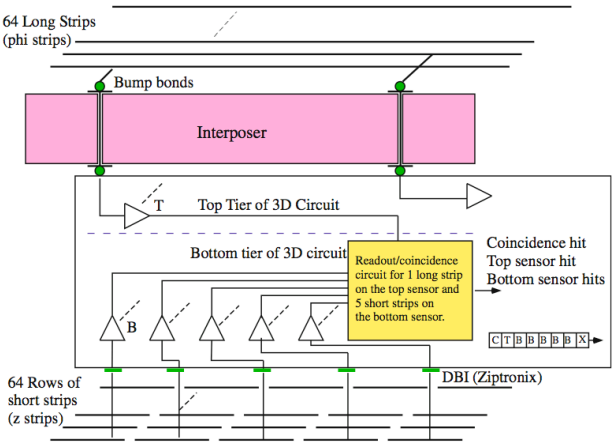

Figure 11: block diagram of a portion of the VICTR chip and the top and bottom sensors [17].

- **Subreticule I** – This subreticule, designed by FNAL, includes a 3D demonstrator chip (VIP2b) for ILC vertex detector with separate bonded sensor [18]. This design has been adapted from earlier MIT Lincoln Laboratory design in SOI technology. It is a 192x192 array of 24um pixels, 8 bit digital time stamp and data sparsification. The analog information is available using correlated double sampling.

- **Subreticule J** – This subreticule has been designed by FNAL, BNL and AGH University [17]. The chip included in the subreticle was designed for X-ray photon correlation spectroscopy to study the dynamics of equilibrium and non-equilibrium processes. The 64x64 3D array of 80 micron pixels has a sparsified binary data output with a read out time of 10us for occupancies of about 100 photons/cm^2/s. The chip has to be bonded to a separate sensor.

- **Subreticule TX** – This subreticule includes test transistors for noise, radiation, and cryogenic measurements. Pavia University designed NMOS and PMOS transistor arrays with nominal Vth, low Vth, thick gate oxide I/O, zero Vth, and zero Vth with thick gate oxide. Devices can be measured on thinned substrate only. FNAL designed NMOS and PMOS transistor arrays with different numbers of fingers/transistor for measurements at cryogenic temperatures. Devices can be measured on thick or thin substrate. This subreticule includes test circuits for VIP2b integrated in subreticule I: correlated double sampler, single channel front-end, front-ends with different W/L input transistors and stand alone discriminator.

- **Subreticule TY** – This subreticule includes two long daisy chains of bond interconnects to measure interconnect yield, two different daisy chains having different bond interface patterns. Each daisy chain has 140000 bond

interconnects with multiple taps. Test transistors based on a standard set of devices (about 46) used by CERN to characterize different processes have also been included. Devices can be measured under different conditions: on standard wafers (2D wafers), on thin substrate bonded to a thick second wafer, on thick substrate bonded to a thinned second wafer.

4. Conclusions and future activity

A large number of institutions formed a consortium for the development of 3D integrated circuits for physics applications. More than 25 designs have been submitted for fabrication in the first multi-project run in the two-tier, vertically integrated, Tezzaron-Chartered 130nm CMOS technology. This multi-project run was a learning experience for the HEP community. Numerous problems arose when putting together different subreticules due to non homogeneous designs and due to the absence of a common software platform for design rules checking. At this point the designers made the design changes, implemented new design rules and accommodated new requests from the foundry. After this rework time the final frame was accepted by the mask house in March 2010 and 3D wafers are expected by the end of 2010. It is true that the expected turn-around time was three month. Actually in the second semester of 2010 many MPW runs in different technologies from different foundries were delayed due to high production workload of the IC industry. CMP, CMC and MOSIS, already cooperating since several years offering commonly some processes and sharing the manufacturing prices, are engaging to provide 3D-IC services. A new design kit of the Tezzaron-Chartered technology has been distributed in July 2010 by the CMP, CMC, MOSIS partnership and the first CMP/CMC/MOSIS MPW run is planned for March 2011. After the evaluation of the structures fabricated in the first run, the 3D-IC consortium has already planned a second MPW run through this new partnership. The members of the consortium provided sufficient expression of interest to fill a full frame (rather than just a half frame as in the first MPW run). The 3D-IC consortium will continue to provide a venue to discuss design issues and compare test results.

Acknowledgments

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