PROCEEDINGS OF SCIENCE

# The Via Revolution

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Throughout history major technological breakthroughs have led to major advances in science. This paper will present an overview of the dramatic impact which Through Silicon Vias (TSVs) are having on the electronics industry and physics community. Basic information is presented to understand TSVs, their formation and use. Some history is presented to show that while TSVs have been used for some time, it is only recently that TSVs are being found in major IC foundries and in physics applications. TSVs permit three different types of 3D integration platforms: 1) wafer level packaging, 2) silicon interposers, 3) 3D integrated circuits. Each of these platforms is described along with examples. A brief glimpse of unusual applications for TSVs concludes this paper.

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## 1.Introduction

A revolution has started in the electronics industry. This revolution is due to the acceptance of through silicon vias (TSVs) in wafers as a new technology to replace transistor scaling as a means of improving circuit performance. With this new feature every integrated circuit can be considered to be a two sided device where connections can be made to the top and bottom or just the bottom of a chip. This leads to 3D integrated circuits with multiple levels of transistors and increased metal routing levels. The adoption of TSV techniques also allows for newer packaging options such as WLP (Wafer Level Packaging) and SiIP (silicon Interposers). An overview of TSV technologies is presented.

3D packaging and 3D integration are sometimes confused. 3D packaging generally applies to stacking of die or packages without the use of TSVs as shown in Figure 1.

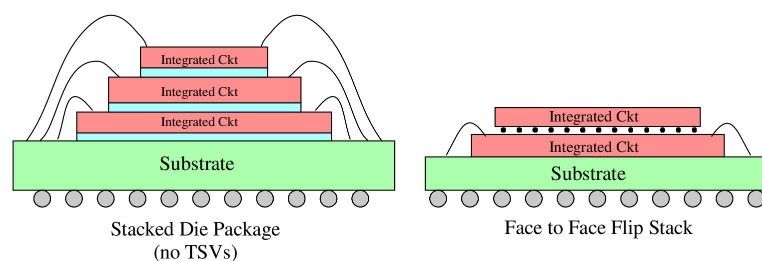


Figure 1 – 3D packaged parts without TSVs

However, 3D integration always uses TSVs. TSVs are used in three broad areas: 1) wafer level packaging, 2) silicon interposers, 3) and 3D integrated circuits. The TSVs are generally used either as an electical connection through a thinned wafer or as a heat conductor.

## 2. Through Silicon Vias

TSVs were used as early as 1975 in a GaAs IC for backside grounding. More than 10 years ago, backside illuminated CCDs were fabricated by thinning the CCD and opening a long trench behind the normal bond pads to allow wire bonding from the backside of the die. In 2005, the technology was applied in High Energy Physics (HEP) to a MAPS device wherein separate openings were made behind each bond pad to allow for wire bonding from the backside, thus allowing backside illumination. [1] More recently, all Medipix3 I/O signals have TSV landing pads in place for backside wire bonding as a first step toward increasing tiling efficeincy for large areas.

### 2.1. TSV Hole Fabriation Techinques

The most common techniques for fabricating TSVs are etching and laser drilling. The Deep Reactive Ion Etch (DRIE), also known as the Bosch process, is the most widely used method for forming small holes in silicon. Holes are formed by rapidly alternating etches with $SF_6$ and passivation with $C_4F_8$. Almost any size hole from submicron to hundreds of microns in



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diameter is possible. The etch rate is sensitive to hole depth and aspect ratio (AR). Walls of the vias are generally very steep and have scalloped sides due to the alternating etch and passivation process. By carefully tuning the process the scallops can be virtually eliminated as shown in Figure 2. [2] For hole diameters below 10 um, the maximum AR is limited to about 20:1. Often a liner needs to be placed in the via to insulate the silicon from the fill material. The practical via AR limit for a good liner in a round via is about 7:1 which thus sets the hole AR.

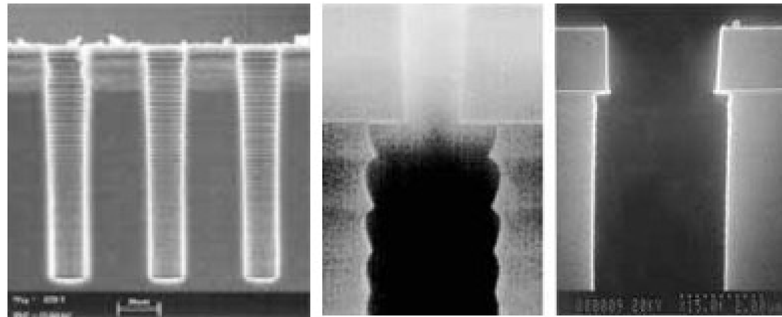

Figure 2 – DRIE hole cross sections: left- holes with steep sides, middle – hole with scallops, right- hole where scallops are minimized.

A plasma oxide etch is used to form small diameter holes in SOI processes. MIT Lincoln Labs uses an oxide etch as shown in Figure 3. [3] The hole does not require passivation before filling with a conducting material since the hole is in an insulating material.

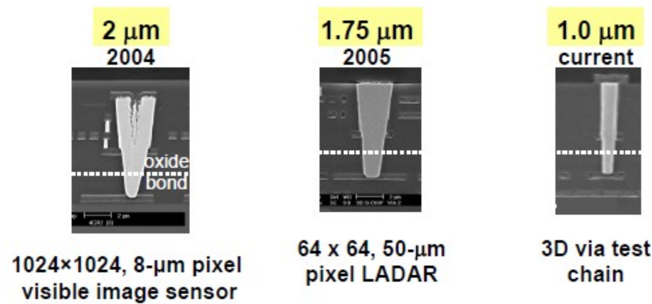


Figure 3 – Oxide etch holes from various MIT LL designs showing improvement with time.

Another common etch procedure is the KOH silicon etch or wet etching. This procedure produces openings with shallow sides and hence is not used for small TSVs.

Laser drilling is used to form larger diameter holes (>10 um) as shown in Figure 4. [4] With laser drilling, holes can be drilled through metal bond pads as well as silicon. The holes can have an AR up to 7:1, and generally the side walls are not as smooth as those formed by etching. Laser drilling is a serial process not well suited to high hole count applications.

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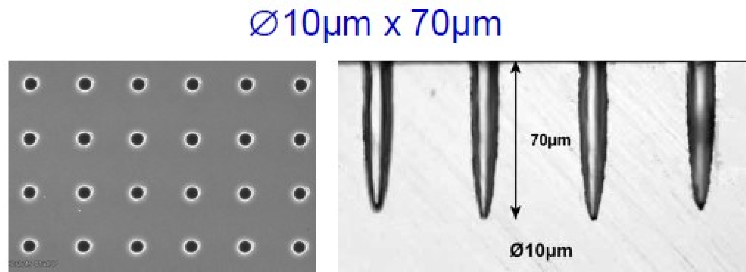


Figure 4 – Laser drilled holes by XSIL

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**2.2. TSV Shapes**

Etched TSVs come in many shapes depending on the application. Annular vias provide a large conducting volume and reduced thermal stress near the via. Trench vias, available in the IBM 0.35 um BiCMOS process, are used to provide high current capacity to the device backside. Both are shown in Figure 5. [5] Cylindrical and tapered holes are also shown in Figure 5. [6] Tapered holes allow for better liners and easier plating or filling of holes.

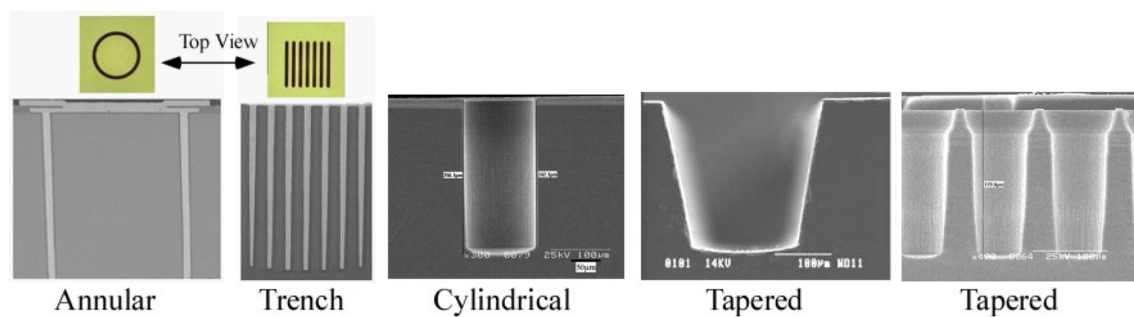


Figure 5 – Cross sectional views of different etched vias

**2.3. Via Fill Materials and Fill Factor**

Various materials are used to fill the vias depending on the application and the foundry. Electroplated copper is preferred by many foundries but copper has a serious TCE mismatch with silicon, which can lead to oxide cracking. However, copper can be used to fill larger vias. CVD tungsten provides an excellent TCE match to silicon but is generally only used for small diameter vias. Tungsten has a thermal conductivity similar to silicon, so it offers no improvement over silicon for thermal vias. Polysilicon is less frequently used to fill holes because of the high temperture that is required. Table 1 includes parameters for materials commonly associated with the TSV process. Larger diameter via holes generally have plated side walls and smaller holes are generally filled.

| **Material** | **Thermal Conductivity (W/m/K)** | **Thermal Coefficient (ppm/K)** |
|---|---|---|
| Silicon | 149 | 2.6 |
| Silicon dioxide | 1.4 | 0.5 |

| Copper | 410 | 16.5 |
|---|---|---|
| Tungsten | 170 | 4.5 |

Table 1 – Commonly used materials associated with TSVs

### 2.4 Types of Vias

Three different types of vias are generally used in 3D integration as illustrated in Figure 6. One type is a blind via, which generally reaches from M1 a short distance down into the substrate. A second type is full TSV, which passes all the way through a wafer from the top side to the bottom. The third type is a backside TSV, which is etched from the backside and stops on M1.

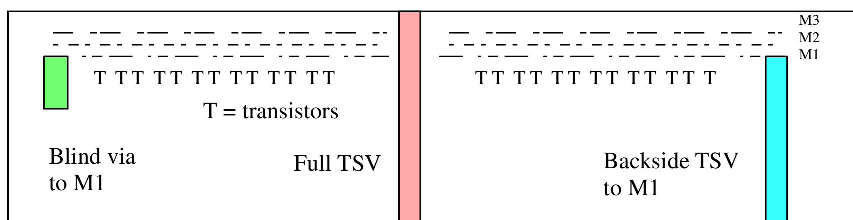


Figure 6 – Example of three different types of vias used in 3D integration

TSVs can be implemented at various stages in the IC processing but there are three that are most common. Vias fabriated before the Front End of Line Processing (FEOL) or transistor fabrication are generally blind vias and are called “via first” vias. Vias added after transistor fabrication but before all of the Back End of Line (BEOL) metalization is completed are also blind vias and are called “via middle” vias. TSVs added after BEOL processing is complete are called “via last” vias. These vias are generally larger than “via first’ or “via middle” vias since they are usually deeper. A “via last” process usually takes away routing space on all routing layers as shown in Figure 7.

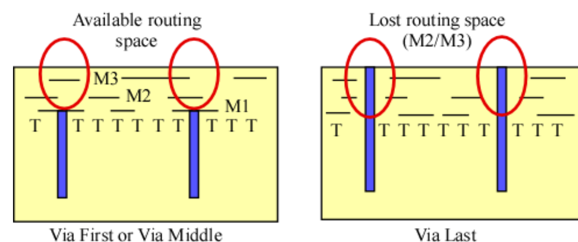


Figure 7 – Comparison of routing space with different via processes

## 3.0 3D Integration Platforms

There are three different 3D integration platforms that depend on TSVs. One that has been used for a number of years is called Wafer Level Packaging (WLP). Vias are added from the backside to M1, allowing contacts to be placed on the back side of a chip. This is a small, low cost package which can also be used for chip stacking.

Another platform is silicon interposers which are built on blank silicon wafers. Among other things, interposers provide a pitch bridge between IC pads and another substrate. Interposers are expected to find many near term applications and are often referred to as 2.5D integration.

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The third platform is 3D integrated circuits which opens the door to multilevel high density vertically integrated ICs. This is the most widely discussed platform at this time and the one that is leading the revolution towards higher performance integrated circuits without additional technology scaling.

### 3.1 Wafer Level Packaging

Wafer Level Packaging is now often used with CMOS image Sensors (CIS). The sensors use a "via last" process. First a transparent glass cover is bonded to the surface of a wafer for mechanical support and surface protection. Then the backside of the wafer is thinned to perhaps 100 microns in preparation for adding the TSVs. Subsequent steps are shown in Figure 8 where a photoresist is added and the vias are etched to the dielectric. An additional etch is used through the dielectric to reach M1, after which the photoresist is removed. A TSV liner is added and an etch step is used to clear the via bottom before the metallization process is completed and a backside bump is added. This process allows for small packages and the top side illumination allows for good performance. Most important, it is a low cost process.

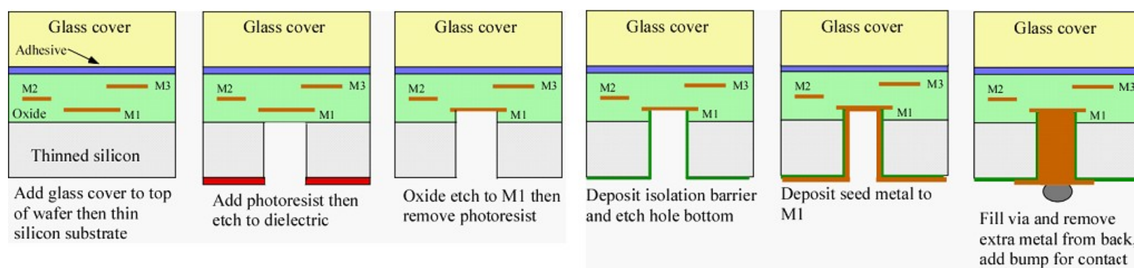
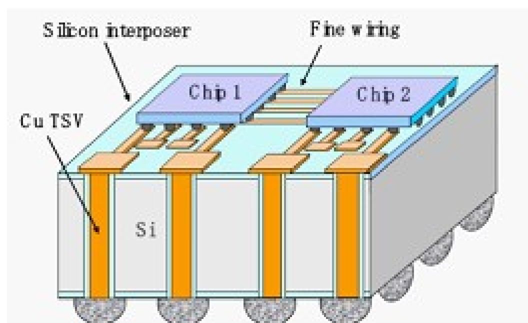



Figure 8 – Wafer Level Packaging steps

### 3.2 Interposers

Silicon interposers (SiIP) have become identified with 3D integration due to the use of TSVs. Typically the interposer wafers are about 300 microns thick and have vias about 50 microns in diameter. Multiple metal layers can be placed on each side of the wafer often to provide fine pitch interconnection between chips and as a pitch adapter between a chip and another substrate. Being made of silicon, there is no TC mismatch between the interposer and ICs. Figure 9 shows a perspective view of an interposer and Figure 10 shows a four chip interposer assembly.



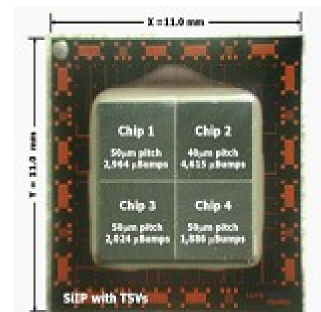






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Figure 9 – SiIP perspective view [7]

Figure 10 – Four chip SiIP Assembly [8]

Silicon interposers are starting to become available from several commercial sources. Although Allvia Inc. focuses on different via technologies for 3D integrated circuits, it also does SiIP with full wafer TSVs. The via diameters range from 30-150 um with a maximum AR of 5. In addition they offer large integrated capacitors within the interposer for localized bypassing. RTI in North Carolina can do SiIP with multiple metal layers as shown in Figure 11. [9] TSVs are etched with an AR of about 7.5 and passive device layers can be included. IPDIA is a French company that has offered two SiIP MPW runs in 2010. The SiIPs are 300 microns thick, and have three metal trace layers and 75 micron vias filled with copper where each via has resistivity less than 10 milliohms.

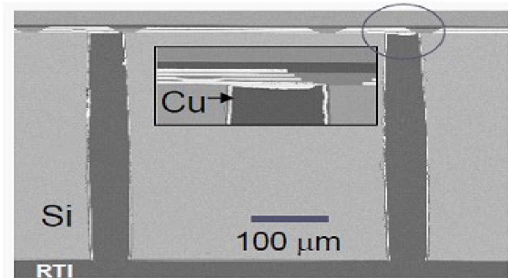


Figure 11 – Cross section of SiIP from RTI

### 3.3 3D integrated circuits

Three dimensional integrated circuits have two or more layers of thinned semiconductor wafers or dice that are bonded together and interconnected with TSVs to form multilayer monolithic devices. It is possible to integrate devices from different technology nodes or semiconductor processes. The TSVs are used to provide interconnection between layers or to provide connections to the top or bottom of the assembled 3D stack. The TSVs allow performance improvements due to shorter traces between functional blocks and higher localized data processing in the case of pixel devices. Figure 12 shows a device from RTI which demonstrates a 3D integrated circuit with an analog layer in 0.35 um CMOS, a digital layer in 0.18 um CMOS, and a HgCdTe photodiode layer. [9]

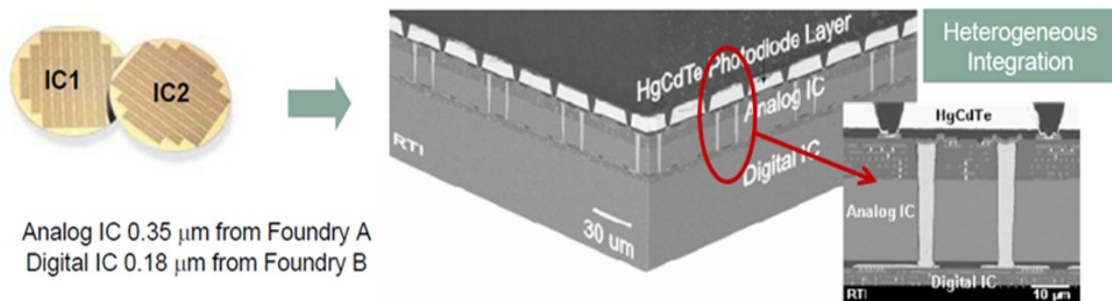


Figure 12 –Multilayer 3D integrated circuit with each layer from a different technology.

#### 3.3.1 Austria Microsystem 3D process

One commercial foundry offering a 3D process with TSVs is Austria Microsystems (AMS). The TSV process is available on any of the AMS 0.35 um analog specialty technologies such as CMOS, SiGe, BiCMOS, HV-CMOS. Two layers are bonded together using a low



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temperature oxide bond. A "via last" process is used to etch vias from the top side. TSVs are 100 um in diameter in a 250 um thick wafer. The vias are plated, have a minimum pitch of 400 um, and can carry 100 mA. The process is intended for mating a ROIC to a photo diode sensor or for mating two layers of CMOS circuitry. Being a "via last" process, space must be left in all the metal routing layers for the TSV. A cross section is shown in Figure 13.

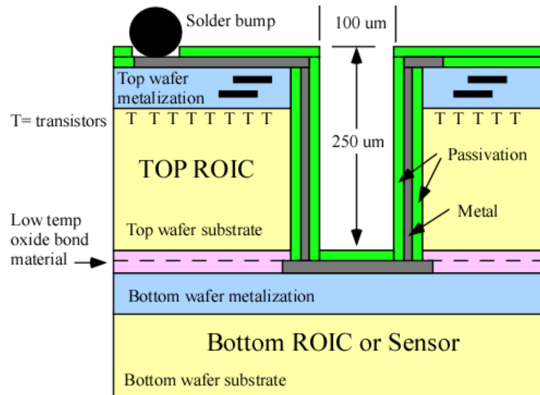


Figure 13 – AMS 3D chip with TSV

### 3.3.2 MIT Lincoln Labs 3D Process

MIT LL also uses a via last process. The vias, however, are used in an SOI process which means that it is not necessary to add a liner to the via before filling with metal. After the BEOL processing is complete on two wafers, the second wafer (tier 2) is inverted, aligned, and bonded to the first wafer (tier 1) using an oxide bond. The back side of the second wafer is thinned, leaving a layer that is only about 7 microns thick. At this point, vias are etched through the second wafer to reach the first wafer and the vias are filled with tungsten, leaving a 2 layer (2 tier) structure with a face to face bond as shown in Figure 14. [10] Additional layers can be added above the second tier by using face to back bonds, and etching and filling additional vias.

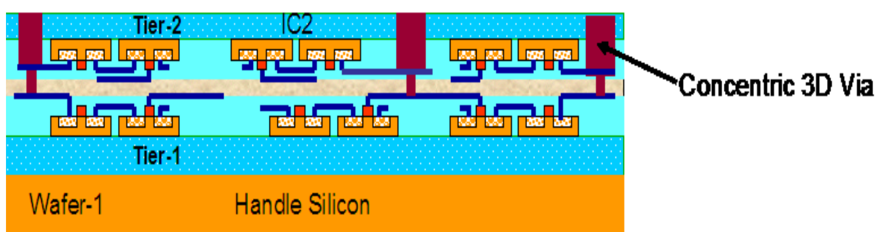


Figure 14 – Cross section of MIT LL two tier 3D integrated circuit, vias shown in red

### 3.3.3 Tezzaron 3D Process

Tezzaron uses a "via middle" process which is currently implemented in the Chartered 0.13 um CMOS process. Tungsten filled vias 6 microns deep are inserted in wafers by Chartered after the FEOL processing and before the BEOL processing. The vias are to be connected to M1. After the BEOL processing is finished, the wafers are ready for 3D assembly.



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The initial bond between wafers is face to face like MIT LL, however, a copper to copper thermocompression bond is formed using the last metal layer rather than using an oxide bond. After the two wafers are bonded, one of the wafers is thinned to expose the 6 micron deep vias. Then pads are added to connect to the exposed vias or an additional wafer is bonded to to the wafer pair using back to face, copper to copper thermocompression bonds. Figure 15 shows a Tezzaron copper to copper bonded pair of wafers with 6 um TSVs in both wafers. [11] One wafer is thinned to expose the 6 micron deep via and pads are attached to those vias.

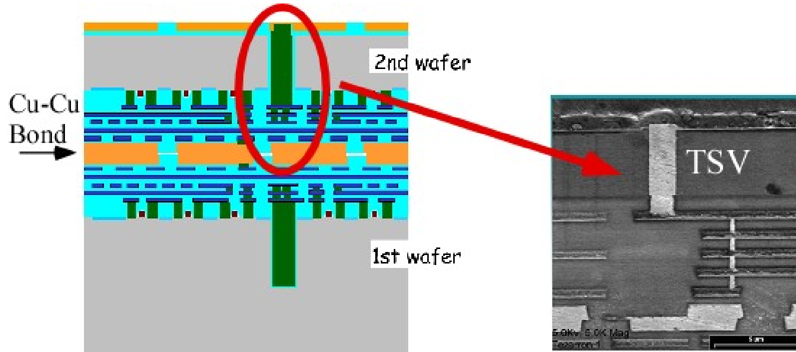


Figure 15 - Cross section of Tezzaron two tier 3D integrated circuit

The Tezzaron 3D process was adopted by a consortium of 15 international HEP organizations to design and build a number of 3D prototype circuits for a variety of applications. In the first MPW run, a single set of masks was used for both the top and bottom tiers of a two tier 3D circuit. The frame shown in Figure 16, included more than 20 designs for projects like CMS and ATLAS at the Large Hadron Collider, B factory, the International Linear Collider, and X-ray imaging. Delivery of these chips is expected late in 2010. [12]

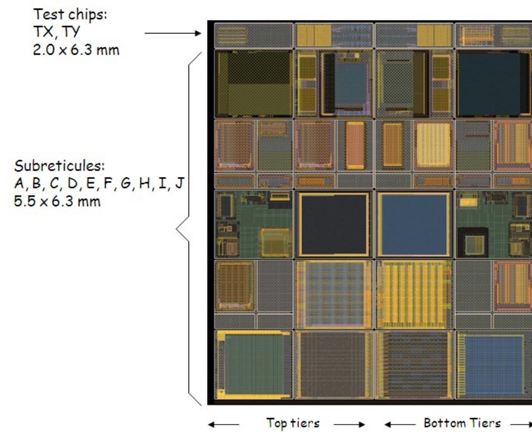


Figure 16 – Frame for Tezzaron MPW run showing layouts for top and bottom tiers

### 3.4 Other uses for TSVs

TSVs are finding other uses. 3D pixel sensors use small diameter, DRIE, blind vias as shown in Figure 17. [13] The top vias are n+ doped while the bottom vias are p+ doped. These 3D sensors offer radiation and speed improvements over conventional 2D pixel sensors.

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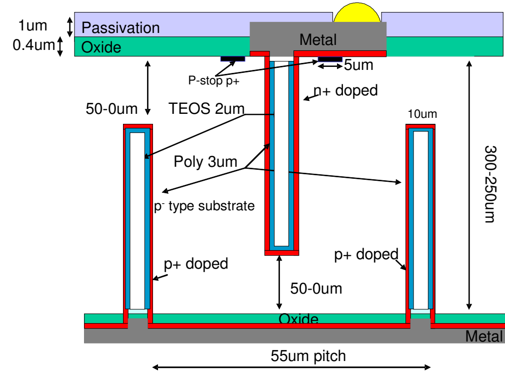


Figure 17 – Cross section of 3D pixel sensor

Horizontal TSVs can be used to form micro channels for cooling. These channels can be formed by etching grooves in two separate wafers which are then bonded together to form the cooling channel as shown in Figure 18. [7]

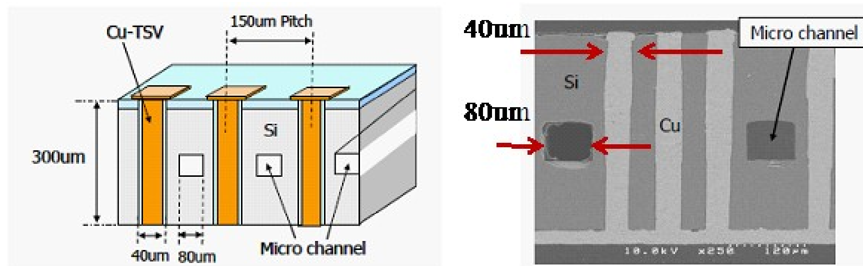


Figure 18 – TSVs used as cooling channels in an SiIP

## 4.0 Conclusion

TSVs have been used in integrated circuits for some time. Recently, however, a via revolution has started since it now recognized that TSVs provide a viable means to extend the performance improvements associated with Moore's law by building 3D integrated circuits. 3D integrated circuits have special benefits for HEP. 3D circuits allow moving much of the peripheral circuitry on 2D detector ROICs to a separate tier which allows more efficient use of real estate for large area arrays. Furthermore, 3D designs allow for more local data processing to reduce data transfer rates off the chip. Reduced data transfer rates are becoming a necessity in large area detector systems.

As a side benefit, wafer level packaging and silicon interposers are using via technologies to offer packaging options heretofore not readily available. Interest in TSVs by the HEP community has developed as evidenced by the 3DIC consortium and the first dedicated MPW run using the Tezzaron Cu-Cu thermocompression 3D assembly process. Vias and 3D integration are here to stay and will continue to find applications in HEP whether it is via first, via middle, or via last. HEP should be ready to embrace the via revolution and the benefits it will bring.

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