

The upgrade of the LHCb vertex detector

Jan Buytaert¹

Cern

CH1211, Geneva, Switzerland

E-mail: jan.buytaert@cern.ch

LHCb will upgrade its detector to be able to take data at 10x higher luminosities (up to $2 \times 10^{33} \text{cm}^{-2} \text{s}^{-1}$) from 2017 onwards. This implies mainly new front-end electronics to readout events at 40MHz. The upgraded VELO baseline design will be a pixel based device. The expected accumulated dose after 100fb^{-1} will be $8.10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$ or 370Mrad, requiring an efficient thermal management of the module to avoid thermal runaway in the silicon. Cooling will be based on the existing evaporative CO₂ cooling system. R&D has started on sensor material, thickness and guard ring structure. The design of a new radiation hard pixel readout asic 'VELOpix' has started. The main challenge will be to handle the enormous, multi Gb/s data rates both on and off chip. A new RF foil must be designed to accommodate the new module geometry and layout.

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¹ Speaker

1. Introduction

According to the current LHC machine run plan, the LHCb experiment will be taking data at its nominal design luminosity of $2 \times 10^{32} \text{cm}^{-2} \text{s}^{-1}$ by the end of 2010. During the following 5 years, LHCb expects to collect an integrated luminosity of at least 5fb^{-1} , which will largely cover its proposed physics program. Thereafter, we want to upgrade the detector during the planned long LHC shutdown in 2016, to be able to run at higher luminosity, initially at (phase1) and later at $20 \times 10^{32} \text{cm}^{-2} \text{s}^{-1}$ (phase2). This increase of luminosity can be achieved by focusing the beams stronger at the interaction point, and does not depend on any LHC machine upgrade.

2. The rationale for the upgrade of the detector

2.1 The expected occupancies

Table 1 shows, for the various luminosities, the average number of collisions for all bunch crossings and for crossings where at least 1 collision occurred. The latter is what defines the occupancy of the minimum bias events and the table shows that this only increases by a factor 2 (1.2 to 2.3) for a 5-fold luminosity increase (2 to $10 \times 10^{32} \text{cm}^{-2} \text{s}^{-1}$). The reason for this is the significant decrease of bunch crossings without any collision.

Luminosity ($10^{32} \text{cm}^{-2} \text{s}^{-1}$)	2	10	20
average # of collisions / all bunch crossings.	0.4	2.0	4.0
average # of collisions / crossings with collisions.	1.2	2.3	4.1
% bunch crossings without collision.	67	13	2

Table 1: The number of collisions at various luminosities.

Most sub-detectors of LHCb can handle this twofold occupancy increase with their current granularities and no major detector overhaul is necessary. For the phase2 upgrade, some detector changes might be needed, e.g. in the tracker stations and the inner calorimeters.

2.2 A new and more efficient trigger

Currently, LHCb has a single hardware trigger (L0), selecting the events to be read out at a maximal event rate of 1MHz into a large CPU-farm.

When increasing the collision rate, this limit on the event readout rate requires that the thresholds of the L0 trigger must be raised. This leads, in particular for the hadron trigger, to a serious drop of efficiency and even a lower total event yield. Rather than rebuilding a new and more complicated trigger in hardware, the decision was taken to increase the readout rate to 40 MHz and implement a flexible event filtering in software on a ‘massive’ CPU-farm.

As a consequence, all front-end electronics must be redesigned or adapted to transfer the data of all crossings to this CPU farm and to zero suppress the data to reduce the required bandwidth.

The L0 hardware trigger will still be used, but with very low thresholds and consequently high efficiency, to reject uninteresting events before they enter the router. This brings a significant saving on the required router and CPU farm sizes.

2.3 The pixel vertex detector

Since the electronics is strongly integrated with the Si-detector, the vertex detector modules will be completely rebuilt. A design based on a 256×256 array of square $55 \times 55 \mu\text{m}^2$ pixels, similar to Timepix [1], is chosen. The advantage, compared to the r-phi strip geometry used in the current VELO, is the true 3D nature of the hits and therefore absence of fake combinatorial hits. The square dimension provides an equal precision in both orientations and therefore halves the required number of measuring planes and the total material.

Many parts from the existing VELO detector can nevertheless be reused, such as the vacuum vessel and equipment, the motion system, the low and high voltage supply systems and the CO₂ evaporative cooling system.

As will be detailed in later sections, the main design challenges will be to handle the enormous on- and off-chip data rates, to provide efficient and low-mass module cooling to avoid thermal run away, to lower the total material budget for reduced multiple scattering and to obtain a similar or better hit precision as in the current VELO ($\sim 4\text{-}10\mu\text{m}$).

3. The expected vertex detector environment

3.1 Irradiation dose

After 100 fb^{-1} of integrated luminosity, the upgraded detector is expected to accumulate a dose of up to $0.8 \times 10^{16} \text{ n}_{\text{eq}} \text{ cm}^{-2}$ or 370Mrad at 7.5 mm from the beam. This will induce leakage currents in $300\mu\text{m}$ thick silicon sensors of $\sim 300 \mu\text{A}/\text{cm}^2$ at -15°C and bias voltage of 900V. An efficient thermal management will be necessary to avoid thermal runaway, without introducing too much material into the acceptance. The electronics will also be required to be extremely radiation hard and single event upset tolerant.

3.2 Particle occupancies and rates

In phase2, the average particles density per crossing closest to the beam will be 8 particles/cm²/crossing and decreasing with radial distance from the beam as $r^{-1.9}$. These are rather low particle occupancies per event ($\sim 10^{-4}$), but at an event rate of 40 MHz, this represent a particle flux of 320 MHz/cm².

3.3 Quality and reliability requirements

The detector will be enclosed inside a 10^{-6} mbar vacuum tank and any access after installation will be very difficult and only possible during a longer shutdown. This imposes stringent quality and reliability requirements and limits as well the choice of materials or components. For example, outgassing properties must be considered, and great care must be taken with the integrity and leak tightness of the cooling connections.

The power dissipation inside the vacuum tank must be minimized, since all cooling must be conductive and will therefore add to the material budget. Evidently connector reliability is paramount.

4. The conceptual pixel module and detector layout

4.1 Sensor tiles

Three readout asics, with dimensions of 14mm x 18mm, are bump bonded to a common silicon sensor with an approximate size of 43x15mm and with a single guard ring of 500 μ m (Fig 1). At the boundary between readout asics the use of larger pixels avoids loss of detection efficiency.

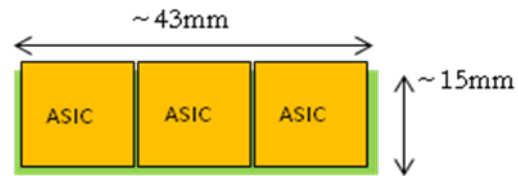
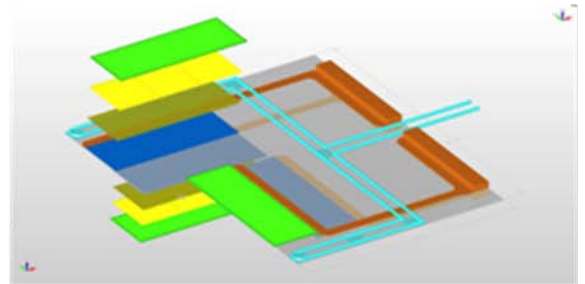
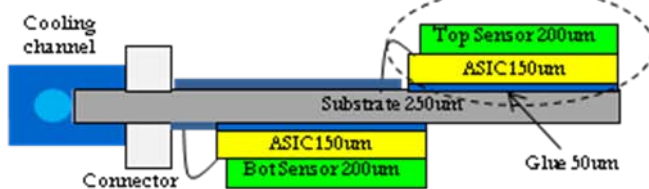


Figure 1 : Sensor tile (dimensions not to scale).

4.2 Modules

Figure 2 : Conceptual module construction.



From previous experience, we aim for a module construction based on a balanced 2-sided design in order to keep the structure planar for ease of construction and to minimize distortion resulting from temperature variations both during construction and operation. The proposed module (Fig 2) will be constructed around a central High Thermal Conductivity (HTC) substrate, made of pCVD diamond or alternatively a carbon fiber clad TPG. This substrate provides the necessary mechanical stability and drains the heat to the peripheral cooling channel. Four sensor tiles are arranged on opposite sides of this substrate such that they can overlap in the transverse plane, minimizing dead areas caused by the sensor guard rings or peripheral circuitry in the asics. The substrate extends about 1cm beyond the edge of the tiles and allows the attachment of a cooling heat sink and the placement of connectors. The innermost edge of the silicon is at 7mm from the beam and the active area starts at 7.5mm from the beam, given a guard ring of 500 μ m. Any possible reduction in either the distance to the beam or the width of the guard ring would directly improve the impact parameter resolution performance of the detector.

4.3 The detector layout

The layout (Fig 3) comprises two movable detector halves on either side of the beam, similar to the current VELO. Each half consists of 26 modules with varying spacing along the beam axis, the minimal pitch being 24mm. The two detector halves

have a relative offset to each other along the beam axis. Also, modules from opposite halves have overlapping sensitive regions for tracks emerging from the interaction point, which is very helpful for precise relative alignment of the detector halves.

The efficiency of this layout for reconstructing, within the LHCb acceptance of

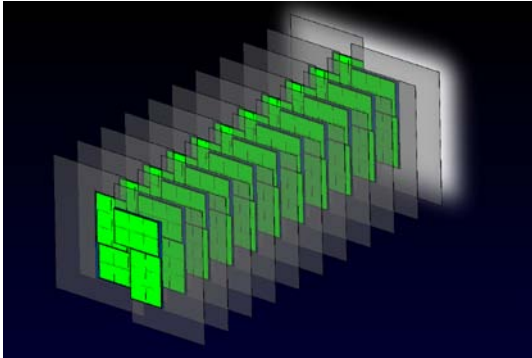


Figure 3 : Conceptual detector layout.

250mrad x 300mrad, all four tracks from a $B_s \rightarrow D_s K$ decay has been simulated to be 98.3%(99.7)% if 4 (3) hits are demanded per track. Assuming that the material contribution of the new foil will be half the current foil, then this layout should achieve a nominal impact parameter resolution performance of $(18 + 27/p_T) \mu\text{m}$, where p_T is the track transverse momentum expressed in GeV/c.

5. The R&D on sensors

5.1 Reduction of the guard ring size

A smaller size will allow the sensitive silicon to be closer to the beam, greatly enhancing the impact parameter resolution. It also reduces the gaps in the module design due to inactive sensor material. Test structures with guard rings down to $100\mu\text{m}$ are under study. The guard ring must withstand 1000V.

5.2 Reduction of the sensor thickness

To reduce the mass in the active area, both the asics and sensors can be thinned after production. It is possible to thin the silicon sensor down to $200\mu\text{m}$ or $150\mu\text{m}$ and even less for readout chips ($50\mu\text{m}$) if a support structure is used. However bowing and handling difficulties may form the limits of what may be achieved here. USC/CNM are producing 200, 150 and $100\mu\text{m}$ p-in-n and n-in-p sensors this year.

5.3 Sensor material

Several options are actively being studied in test beams regarding their charge collection efficiency, leakage currents, charge spreading characteristics and position resolution at the required radiation dose.

5.3.1 Planar Silicon

Substantial amount of experimental data has been accumulated in the last years showing a surprisingly large charge collection in severely irradiated silicon detectors. A $150\mu\text{m}$ planar silicon sensors can provide a signal of $6000e^-$ for a MIP particle even after doses as high as $2 \times 10^{16} \text{ n}_{\text{eq}} \text{ cm}^{-2}$ [2]. After this level of irradiation, thin detectors ($150\mu\text{m}$) also provide a higher signal charge than thicker ($300\mu\text{m}$) at the same bias voltage, because of a charge multiplication at high electrical field [3].

The charge sharing is expected to reduce with irradiation, and this will be studied during our next irradiation and test beam campaigns.

5.3.2 3D pixel detectors

These devices have shown the largest charge collected for any given fluency of any known silicon technology. Only moderate bias voltages, 150 V, are necessary for 100% charge collection for fluencies up to $10^{15} n_{eq}/cm^2$ [4]. Higher radiation doses reduce the collection efficiency, but for $10^{16} n_{eq}/cm^2$ the collected charge at 150 V is still 44% and charge multiplication is also observed at higher bias voltage [5]. The reduced bias voltages also lower the risk for thermal runaway.

3D devices are difficult to fabricate, but the University of Glasgow in collaboration with IMB-CNM Barcelona, have developed a new type of 3D detector known as double-sided 3D sensors, which eases the fabrication difficulties, and has been demonstrated with high yield in three productions runs over the last three years. An additional advantage of 3D technology is that the self-shielding geometry and additional processing can allow devices to be active to within $10\mu m$ of the physical edge.

5.3.3 p-CVD diamond

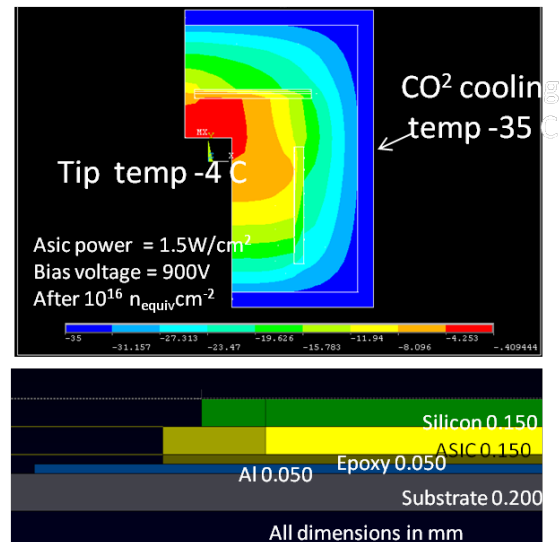
Chemical Vapor Deposition (CVD) diamond has some appealing properties as a sensor element for hybrid pixel modules operating at the extreme radiation fluencies. Given the modest total sensor surface of $\sim 1340 cm^2$, this could be financially affordable for the VELO upgrade. We have acquired some pCVD diamond samples suitable for bump bonding with TIMEPIX devices and have measured the collection length of all the 5 samples with a Sr90 source, obtaining collection lengths between 200 and $250\mu m$. Test beam studies to validate these measurements and to study other properties such as efficiency and spatial resolution are under way.

6. Module cooling

Thermal simulations with ANSYS of simplified module structures have been done, including the temperature and radial dependent leakage current in the silicon. With a CO_2 cooling temperature of $-35 C$ and an ASIC power of $1.5W/cm^2$, the highest temperature on the module is $-4 C$ (Fig 4). The results suggest that a HTC substrate of $200\mu m$ thickness may be adequate; however minimization of the temperature drops in the interfaces between the tiles and substrate and between the substrate and the cooling heat sink are critical in achieving this. Identification of adhesives and a process to achieve repeatable very thin glue layers capable of resisting shear from CTE

differences between the silicon tiles and the substrate will be investigated. As the detector is operated in a secondary vacuum, leakage from the cooling system is avoided by providing a pre-engineered leak tight system and attaching the heat sinks during

Figure 4 : Thermal simulation.



module installation. Development of a demountable low mass heat sink structure compatible with the substrate CTE and adequate thermal performance is a priority.

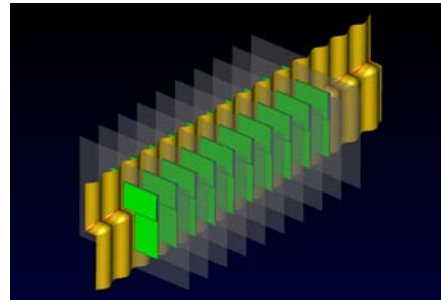
7. The RF foil

The main purpose of the RF foil is to act as a de facto beam pipe, with all its attendant functions, viz., it must: separate the primary (accelerator) and secondary (detector) vacuum, carry the image currents of the beams, withstand the heat load and high radiation of the beam, shield the frontend electronics against beam induced electromagnetic pick-up and be mechanical stiff up to small pressure difference of 5 mbar.

A new RF foil must be designed to accommodate the new modules. We aim to reduce even more its mass, since it is the largest single contributor to the total material thickness of the VELO detector (~50%), adding significant Coulomb scattering to the vertex and tracking errors. A conceptual view of the upgrade RF foil is given in Fig 5.

The materials considered are a workable metal alloy similar to AlMg3, as used successfully in the current RF foil or a new carbon fiber reinforced polymer (CFRP). Work is underway to fabricate coupon samples of different material layups and forming techniques using small molds of the foil design. A testing programme has been developed for determining the resulting curvature profile, uniformity of thickness, mechanical deformation, vacuum sealing, minimum feature size, radiation tolerance etc.

Figure 5 : RF foil.



8. The data readout challenge

As explained in section 3.2, the particle rates will be very high close to the beam and at the highest luminosity, averaging 200 MHz per ASIC. Assuming a worst case average cluster size of 3 pixels and 32 data bits per pixel hit, the data production rate can reach 19Gbit/s in one ASIC! The 32 data bits are composed of 4 bit for TOT ('time-over-threshold') value, 12 bit for bxo ('bunch crossing') identification and 16 bit for the pixel identity. A 30% reduction can be obtained by clustering the data of simultaneous and nearby hits, since the bxo id and some pixel address bits can be shared. This clustering can be optimally done by concentrating the digital logic of a group of 4 by 4 pixels (called a 'superpixel') in a single area and the analog part of the pixels is put on either side of this digital area (fig 6). This brings many advantages, such as space saving (some digital blocks can be shared), a more efficient power and global signal routing, better

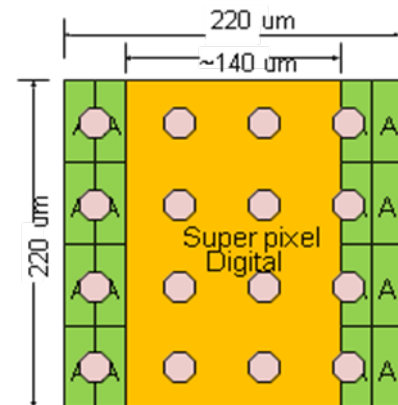


Figure 6 : 4x4 superpixel.

isolation between analog and digital sections and the possibility to synthesize the column logic from a standard library rather than custom cells. A disadvantage is the possible digital noise feedback into bonding pads on top of the digital area.

9. The VELOpix readout ASIC

Simulation studies have shown that the pixel charge must be digitized to 3 or 4 bits to obtain the best spatial accuracy by charge interpolation. A time-over-threshold ADC conversion technique is adequate, since the maximal pixel hit rate is at most ~ 10 kHz. Indeed, a maximal conversion time of 400ns will cause 0.4% dead time in the worst case.

The VELOpix will be developed as a follow up of the TIMEPIX2 that is being designed in 130nm CMOS. The asic contains 256×256 square pixels and measures ~ 14 mm on each side. Each pixel will measure the time-over-threshold (4bit) and the arrival time (12bit) of each hit.

A block diagram (Fig 7) shows the readout architecture to handle the extreme data rates. In a super pixel, the data is clustered and stored in a buffer, which can contain up to 2 clusters. In a next level, the data from 4 super pixels is merged into a single FIFO (400bit) that connects to the column bus, which is 8 bit wide, 40MHz cycle and arbitrated by a rotating token. Finally, the data streams from 16 columns are merged on an output bus (16bit@320MHz) and into a large output buffer. From there, the data is serialized and driven off chip by a high speed port (4 Gb/s). Four such identical sections read the total pixel array. First simulations of this architecture show that the data loss stays below 0.5% in the highest occupancy conditions.

The chip power consumption should stay below 3W, to avoid causing thermal runaway in the sensor.

10. R&D prototyping tools

To aid the qualification of technologies, several tools are being developed, such as laser test stands, vacuum chambers and a particle telescope.

A focused red or near IR laser that will deposit charge in very precise locations in the detectors is operational. Coupled to accurate motion stages, the laser spot can be scanned with sub micron accuracy over the detectors and will allow detailed study of the response of sensors and front end amplifiers as well as effects such as charge sharing, time walk and cross talk.

The vacuum chamber allows measurement of out gassing rates of various materials. Through an IR transparent window, a thermal camera will measure the thermal performance of prototype modules. It will be instrumented with sensors to measure the mechanical deformations.

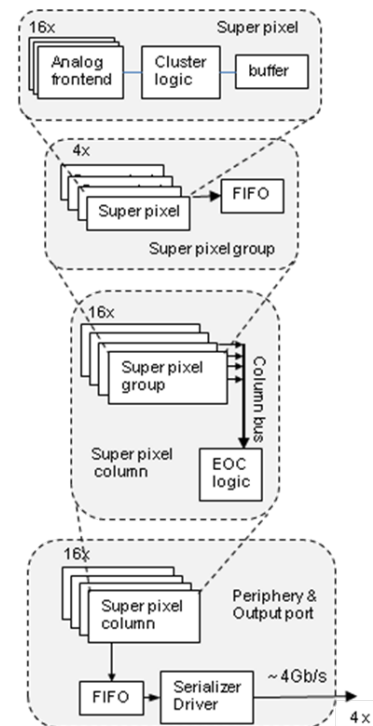


Figure 7 : Readout architecture.

A new 8 plane beam telescope, built with TIMEPIX sensors, has been assembled to make extensive test beam campaigns. It acquires tracks at a rate of 2.5 kHz and provides a hit prediction error of $1.6\mu\text{m}$ at the device under test with a timestamp precision of 1nsec.

11. Conclusions

LHCb plans to install an upgraded detector in 2016. All electronics must be adapted or replaced to be able to read out events at the full 40MHz rate. The VELO detector will be rebuilt based on pixel sensors and the conceptual module and detector layout have been presented. The R&D has started on sensor material, module thermal management, a new RF foil and a new pixel readout ASIC. Tools have been built and are operational for qualifying prototypes.

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