PROCEEDINGS OF SCIENCE

# Atlas Upgrade

**Daniel Muenstermann**[*†]
*TU Dortmund*
*Physik E4*
*D-44221 Dortmund, Germany*
*E-mail:* daniel.muenstermann@cern.ch

Following the commissioning of ATLAS and the LHC, plans to further increase the design luminosity of $1 \cdot 10^{34}\,\mathrm{cm^{-2}s^{-1}}$ towards $5 \cdot 10^{34}\,\mathrm{cm^{-2}s^{-1}}$ (*SuperLHC* or *sLHC*) have been presented. These accelerator upgrades will increase the data rates with which ATLAS has to cope and will also require hardware upgrades of several sub-detectors.
This paper gives an overview of the current plans for upgrades of the ATLAS (inner) detector and highlights the status of developments for the individual sub-detectors. As a first modification, the insertion of a new innermost b-layer is foreseen, the *insertable b-layer* IBL. In addition, upgrades of the trigger are planned to better include tracking information in the trigger decisions.
At luminosities beyond $3 \cdot 10^{34}\,\mathrm{cm^{-2}s^{-1}}$, the occupancy level of parts of the current inner tracker requires a complete replacement. It is planned to use an all-silicon tracker in the future consisting of pixel detectors for the inner layers and silicon strip detectors for the outer layers. The innermost pixel layer has to withstand up to $2 \cdot 10^{16}\,\mathrm{n_{eq}/cm^2}$

*19th International Workshop on Vertex Detectors*
*June 6 -11 2010*
*Loch Lomond, Scotland, UK*

[*]Speaker.
[†]on behalf of the ATLAS collaboration

© Copyright owned by the author(s) under the terms of the Creative Commons Attribution-NonCommercial-ShareAlike Licence. 

PoS(VERTEX 2010)038

## 1. Introduction

The current ATLAS detector[1] was designed to be operated at a luminosity of $1 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and to be able to take data up to an integrated luminosity of 500–700 $\mathrm{fb}^{-1}$ after 10 years. After the successful commissioning of both accelerator and detector, it is planned to further increase the LHC's luminosity in the coming years. This would enable the LHC detectors to take some 1000 $\mathrm{fb}^{-1}$ of data within a rather short period of time which significantly extends the LHC's physics reach[2]. Depending on the details of the accelerator upgrade, ATLAS will have to cope with a significant increase in data rate, occupancy, radiation damage and pile-up which requires upgrades of most sub-detectors. Figure 2 depicts the dramatic effects of a luminosity increase.

This paper will focus on the upgrades of the inner detector. Currently, it consists of a silicon pixel detector[3], a silicon microstrip tracker (SCT)[4] and a gas-based transition radiation tracker (TRT)[5] (see fig. 1). In a first step, a new innermost pixel layer, the so-called *insertable b-layer* (IBL) will be installed together with a new beampipe to improve the impact parameter resolution and compensate possible inefficiencies of the current pixel detector.

As all sub-detectors would become inefficient during the sLHC operation, it is foreseen to replace the whole ATLAS inner detector. Currently, an all-silicon tracker is planned with standard ('long') microstrip sensors between 70 and 100 cm radius, 'short' microstrip sensors in the intermediate region with increased occupancy and pixel sensors within a radius of about 30 cm. For the innermost pixel layer(s), the suitability of standard planar silicon sensors has not yet been established, hence new sensor technologies are also under evaluation.

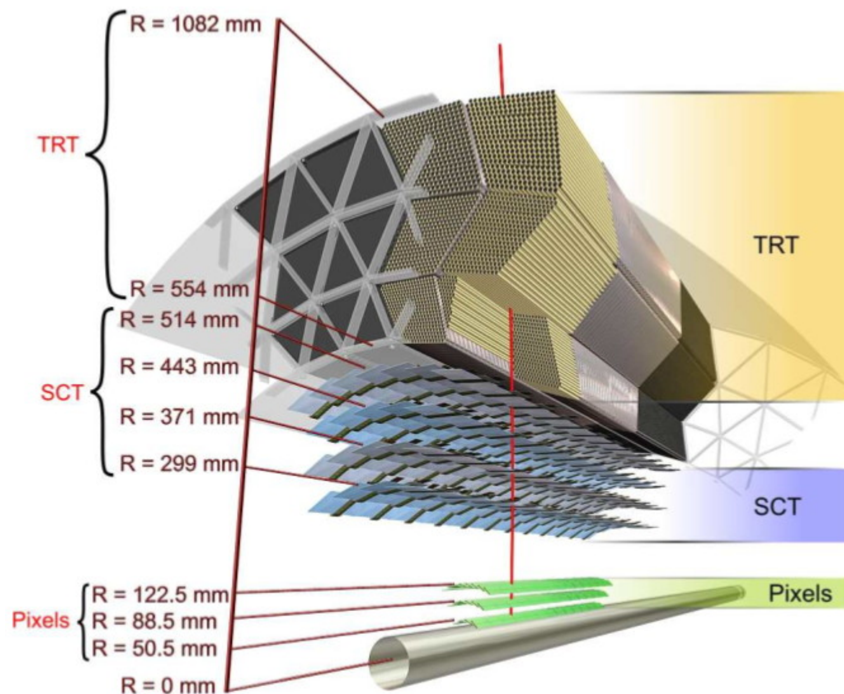
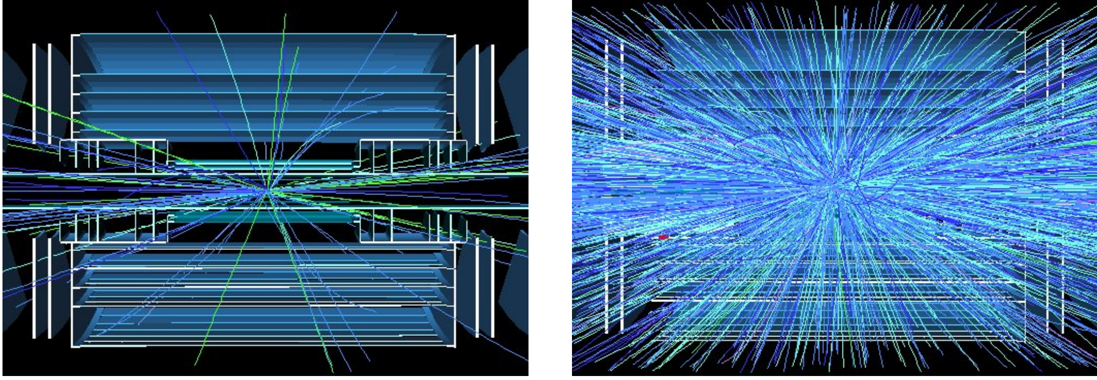



**Figure 1:** Schematic view of the ATLAS Inner Detector with the TRT on top, the SCT layers in the middle and the Pixel detector at the innermost radii. Taken from [1].



PoS(VERTEX 2010)038



(a) Pile-up (5 collisions) at $2 \cdot 10^{33}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$.

(b) Pile-up (400 collisions) at $1 \cdot 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, which includes a safety factor over the maximum expected 200.

**Figure 2:** Pile-up events at different luminosities. Plots provided by A. Abesselam.

## 2. Requirements

Within the coming years, the first goal is of course to reach the nominal design luminosity of $1 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ which is foreseen to be completed[6] in 2016. It is then planned to first increase LHC's luminosity to a level which is usually designated with *LHC ultimate luminosity* or *phase I* in the region of $2-3 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ by a collection of comparatively small upgrades of the machine like the Linac4 installation and collimation upgrades. Later, presumably after 2020, a major upgrade effort (*phase II*) probably including the installation of new interaction region focusing quadrupoles and so-called crab cavities will increase the luminosity further up to about $5 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ (including luminosity levelling).

The ATLAS inner detector design is able to cope with the luminosities of *phase I*, but the

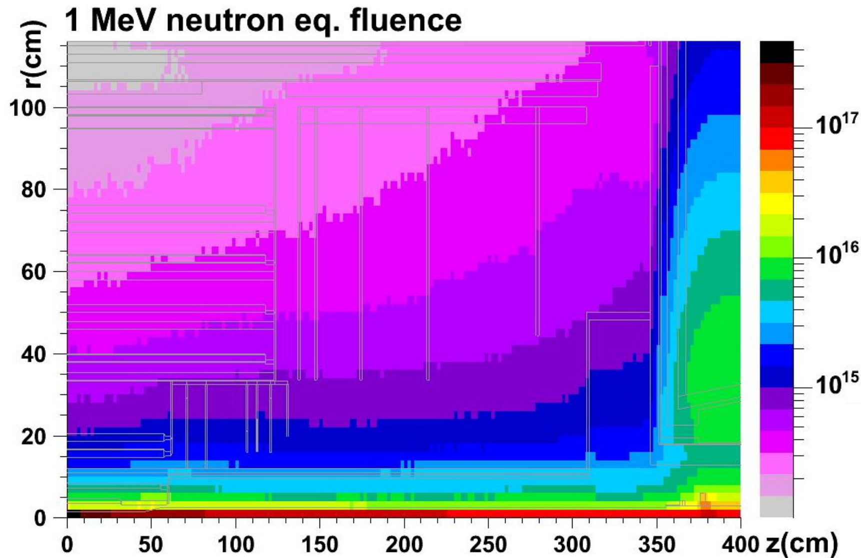



**Figure 3:** Radiation damage: fluences in $\mathrm{n_{eq}/cm^2}$ expected for 3000 $\mathrm{fb}^{-1}$. Usually, a safety factor of 2 is applied to generate the requirements for the sLHC. Taken from [9].



PoS(VERTEX 2010)038

current innermost layer of the pixel detector (*b-layer*) is likely to approach two limits: First, it might have received its design fluence of $1 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ after which its efficiency might deteriorate slowly. Besides, caused by the bus architecture of the FE-I3 pixel readout chip[7], there might be data losses due to bus congestion beyond $3 \cdot 10^{34}\,\mathrm{cm^{-2}s^{-1}}$[8] (see fig. 4(a)).

The requirements of *phase II* are much higher:

- up to 200 pile-up events per bunch-crossing (depending on the upgrade scenario and how/whether luminosity levelling is implemented) which causes large occupancies in many sub-detectors (see fig. 2)
- up to $2 \cdot 10^{16}\,\mathrm{n_{eq}/cm^2}$ of fluence in the innermost pixel layer[9](see fig. 3)

Hence, it is foreseen to replace the complete inner detector in a *phase II* upgrade. In addition, several improvements and upgrades concerning the electronics, trigger and DAQ are planned in both phases.

## 3. Phase I: towards $\mathscr{L} = 3 \cdot 10^{34}\,\mathrm{cm^{-2}s^{-1}}$

### 3.1 Phase I: IBL

By the introduction of a new, smaller diameter Beryllium beampipe, it is possible to use the additional space for the insertion of an additional 4th pixel layer: the *Insertable B-Layer* or IBL (see fig. 4(b)). This layer would improve the impact parameter resolution and the b-tagging and hence enable better and new physics analyses, but it would also be able to compensate a possibly deteriorating b-layer suffering from radiation damage and high pile-up towards the end of phase I. A Technical Design Report[10] is currently being written; it is anticipated to build the IBL by 2015. The IBL faces several technological and engineering challenges:

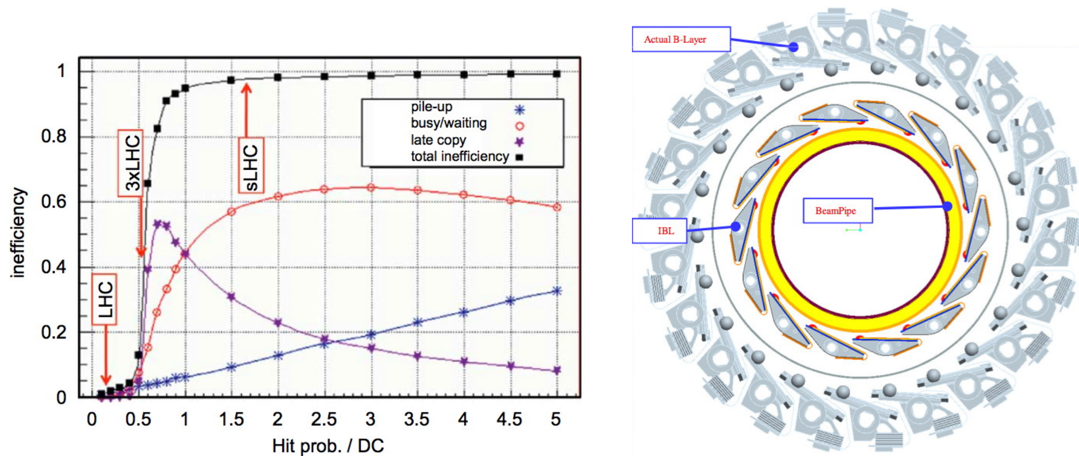
- data rate: FE-I4 readout chip
  As shown in fig. 4(a), the data rate exceeds the capabilities of the FE-I3 readout chip even at the radius of the current b-layer. Therefore, a new readout chip was designed: the FE-I4[8]. In addition to larger data transfer capabilities of 160 Mb/s, there are also several improvements with respect to its predecessor: the chip is very large (about $(20.2 \times 19.0)\,\mathrm{mm}^2$ compared to $(7.6 \times 10.8)\,\mathrm{mm}^2$) which leads to a larger active fraction (89% vs. 74%) and helps to minimize the material budget. It implements a new way to deal with charge sharing and is expected to be more tolerant with respect to ionizing dose (up to 2 MGy). Thanks to being produced in a 130 nm process, the pixel size has been reduced from $50 \times 400\,\mu\mathrm{m}$ to $50 \times 250\,\mu\mathrm{m}$.

- radiation damage: sensor choice
  It is not yet clear whether the current type of pixel sensor (planar *Diffusion Oxygenated Float-Zone* (DOFZ) silicon sensors) is suited for fluences up to $5 \cdot 10^{15}\,\mathrm{n_{eq}/cm^2}$ which has been set as an IBL requirement[1]. However, there are strong indications from investigations with

[1] Due to the small radius, the IBL receives significantly more radiation damage than the current b-layer, even though the end-of-life integrated luminosity is somewhat lower (550 vs. 700 $\mathrm{fb^{-1}}$)



PoS(VERTEX 2010)038




(a) Contributions to inefficiency of the FE-I3 pixel readout chip in dependence of the data rate (measured in hits per double column per bunch crossing). Taken from [8]

(b) Cross section drawing showing the current b-layer, the new beam pipe and the envisaged position of the IBL.

**Figure 4:** IBL: data rate challenge and IBL cross section.

planar silicon strip sensors that this will be the case[13] also thanks to a charge amplification effect seen at high electric field strengths[14, 15]. Therefore, planar sensors are currently being manufactured and will be irradiated and tested in future test beams at CERN and DESY. Other technologies which are promising candidates for radiation hard sensors are 3D silicon sensors[16, 17] and diamond sensors[18]; these will also be tested before a sensor choice is taken in 2011.

- tight envelope: flat staves, active/slim edges
  Due to the very limited space, it is not possible any more to 'shingle' the detector modules in the $z$-direction[2] to get hermetic coverage; the staves have to be flat. To minimize the geometric efficiency losses, the edges of the modules have to be active or at least slim. It is currently foreseen to build either SingleChip modules (1 sensor per FE-I4) or 2-chip modules (1 sensor per 2 FE-I4s). The current ATLAS pixel sensor has an inactive edge width of about 1100 $\mu$m. A reduction to 450 $\mu$m for 2-chip modules is required and inactive edge widths of below 300 $\mu$m have already been achieved with planar pixel sensors. With 3D and diamond sensors, the edges can be 'active' with inefficient margins of only a few tens of $\mu$m.

- beampipe extraction and insertion
  The current pixel package should stay in place, only the old beampipe shall be extracted and replaced. To counteract the gravity sag, the current pipe is suspended by two cruciform supports and two wire suspensions. These will have to be cut, captured and re-used while at the same time the beampipe is supported by the so-called *Long Support Tube* which is slid into the beampipe beforehand. In summary, extraction and insertion of the old and new beampipes is a highly non-trivial engineering problem which is taken care of by a dedicated 'Integration and Installation' workgroup.

[2]The z coordinate runs along the beampipe, in the r-$\phi$ direction the staves will still overlap (*roofing*); see fig. 4(b).



PoS(VERTEX 2010)038

The IBL project is in good shape and is making progress in all fields of development. Further details can be found in the *IBL Technical Design Report*[10].

### 3.2 Phase I: FTK

Another upgrade already in progress is the development of a *Fast TracKer* (FTK)[11] which implements track finding and fitting in hardware and is therefore extremely fast. Today, the track finding and fitting is done at the level-2 processor farm in software; the runtime is on the order of some ms while the complete level-2 trigger decision should take $\approx$ 10 ms. With increasing pile-up and occupancies, this will consume more processing power and will take significantly longer. FTK's runtime is on the order of few tens of $\mu$s even at $3 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. With the reconstructed track information to hand almost instantly, the level-2 trigger can spend the freed up processor time on improved b-tagging or other measures to keep the rate of selected events low. While the current FTK schedule is aimed at $3 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, concepts to extend the reach up to sLHC fluences exist and are being pursued.

## 4. Phase II: sLHC

Towards the end of phase I, both the achieved luminosity as well as the accumulated radiation damage will necessitate the replacement of the current inner detector. To adjust the granularity (and with it the necessary number of readout channels) to the track density, it is foreseen to include three to four different sensor types into the new ATLAS tracker:

- long strip sensors: 2 layers of standard silicon microstrip sensors with $\sim$ 10 cm strip length at outer radii ($\sim 70 - 100$ cm).
- short strip sensors: 3 layers of silicon microstrip sensors with $\sim$ 2.5 cm strip length to reduce the occupancy while keeping the same readout chip at intermediate radii ($\sim 30 - 70$ cm).
- outer layer pixel sensors: $2 - 3$ layers of standard silicon hybrid pixel sensors at radii of $\sim 8 - 35$ cm; the comparatively large area requires a focus on cost-efficient sensors and hybridization methods.
- inner layer pixel sensors: the very severe radiation environment below $\sim$ 8 cm radius might impose the need for new extremely radiation-tolerant technologies such as 3D silicon or diamond pixel sensors.

An illustration of the layer positions can be found in fig. 2. Details on dedicated track-trigger layers within the upgraded tracker can be found in [12].

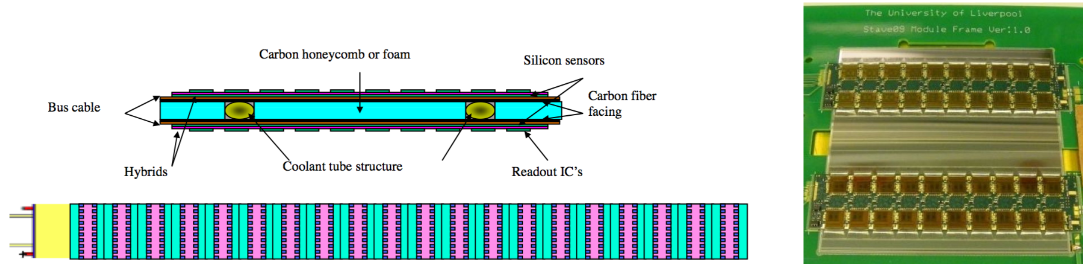
### 4.1 Phase II: Strips

In the current ATLAS tracker, the strip sensors were manufactured as $\mathrm{p}^+$-in-n junction devices which collect holes. These charge carriers have – compared to electrons – a lower mobility and are more affected by radiation damage induced trapping, therefore it is planned to use electron-collecting $\mathrm{n}^+$-in-p sensors for the upgraded tracker[3].

[3] p-bulk silicon of the required purity was not available in the past.



PoS(VERTEX 2010)038




(a) Schematic view of the short strip stave prototype *stave09*. The stave has a total length of 1.2 m and contains 10 short strip sensors of dimensions of about $10 \times 10$ cm. Each of these is wirebonded to 4 rows of ABCN25 readout chips which are connected to 2 hybrids per sensor. The heat is transfered through the sensor into the carbon honeycomb and foam of the stave where two cooling pipes are located. Illustration provided by LBNL.

(b) Photograph of a module for the stave09 assembly. It rests within a PCB frame, the sensor, the hybrids and the ABCN25 readout chips can be seen.

**Figure 5:** Strip detector prototyping: *Stave09*

As there is already experience with the production and operation of 'long strips' sensors, recent R&D efforts have focused on short strip sensors, both as miniatures for irradiation tests and as full-size short-strip sensors. During several prototype productions, different insulation schemes and guard ring designs were tested. Besides, data taken with irradiated miniature microstrip sensors confirmed that the radiation tolerance of $n^+$-in-p sensors well exceeds $1 \cdot 10^{15}\,n_{eq}/cm^2$[13] which is the benchmark fluence for the short strip region (see fig. 3).

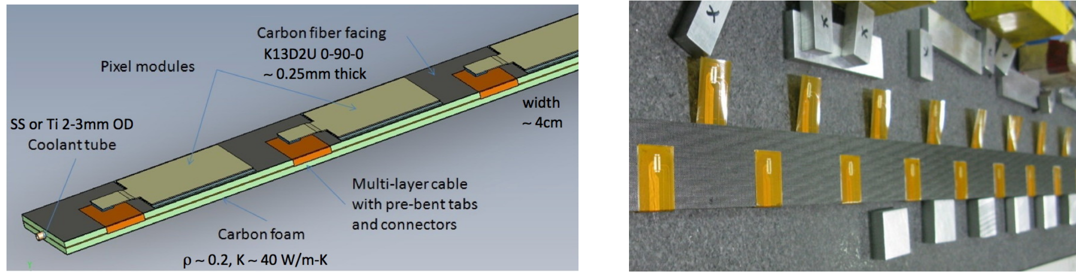
Both short and long strip sensors will be read out by a successor of the ATLAS SCT readout chip ABCD: the *ABCN* chip which was already produced in a 250 nm process and will be used to built first module and stave prototypes. A 130 nm process version will follow later.

Concerning the assembly, the *Stave* concept using single-sided modules is mainly pursued: the sensors are glued directly to a carbon-foam and/or honeycomb based stave structure which contains cooling pipes. Bus cables, hybrids and readout chips are also fixed by glueing. First prototype short strip staves have been built; the *stave09* project is currently aiming to produce a 1.2 m long stave with realistic sensor, hybrid and readout chip coverage (see fig. 5). As an alternative, the *Super-Module* concept is being investigated. Here, double-sided modules are mounted in a rigid frame and the heat from the readout chips sitting on bridges is transfered to the side of the frame where the cooling pipes are running.

### 4.2 Phase II: Pixels

The region of the future pixel detector is subdivided into two domains: For the outer layers, current sensor technology is fully sufficient to cope with the expected occupancy, data rate and radiation damage. However, cost efficiency is an issue: The expected area which must be covered by pixel detectors is at least twice as large as today; the outermost layer might have a radius of almost 30 cm compared to 12.25 cm currently. Ideally, the cost per area should not exceed that of short strips. For the innermost radii, the expected radiation damage (see fig. 3) exceeds the LHC design fluence by a factor of 20. Here, on the other hand, the area to be instrumented is so small that the cost per area is of less relevance.

PoS(VERTEX 2010)038




(a) Schematic view of a double-sided outer layer pixel stave. The stave will have a total lenght of 1.2 m and contain about 15 $(4 \times 4)$ cm$^2$ pixel sensors covered by $2 \times 2$ FE-I4.x readout chips. The heat is transfered through a low-density carbon foam to the cooling pipe.

(b) Photograph of an outer pixel layer stave prototype. The flex cable is running inside the stave, only the connector flaps are visible.

**Figure 6:** Pixel detector prototyping

There are four sensor candidates for the innermost pixel layer: planar silicon[13], 3D silicon[16, 17], pCVD diamond[18] and the gaseous Gossip technology[19]. All technologies have shown promising results, but (also due to the lack of a sufficiently radiation hard readout chip) have not yet been able to demonstrate their performance as a pixel detector after $2 \cdot 10^{16}\,\mathrm{n_{eq}/cm^2}$. The FE-I4 readout chip has not enough bandwidth to cope with the data rate of a sLHC b-layer sensor and will probably not be radiation hard enough. A successor chip ("*FE-I5*") might be realised in a smaller process and/or as a 3D integrated chip[20]. This allows the pixel size to be reduced, lowering the occupancy and improving the resolution.

To be able to access the innermost pixel layer(s) also during rather short maintenance stops, it is currently under discussion to make them quickly extractable on a rail system. Due to the comparatively small sensor area, the construction of the innermost pixel layers will not take as much time as for the outer pixel or strip layers. Hence, current activities focus not yet on prototyping but on radiation hardness studies of the candidate sensor technologies.

For the outer pixel layers, however, the expected fluences will not exceed a few $10^{15}\,\mathrm{n_{eq}/cm^2}$ (see. fig. 3) for which planar pixel sensors are considered radiation hard enough. Because the instrumented area will be much larger than in the current pixel detector (outermost radii at 20 – 30 cm compared to 12.25 cm today), cost efficiency is a major focus of R&D and prototyping.

Major cost driver in the current pixel sensor has been the hybridization process ('bump-bonding'). Within the *ATLAS Planar Pixel Sensors R&D Project* (PPS)[21], different FE-I4 size daisy-chain structures have been developed to investigate cost reduction in this sector by means of reducing machine time with faster, but less precise flip-chipping machines. Besides, less handling steps are expected by moving from a chip-to-chip flipping scheme to a chip-to-wafer scheme which is also currently being explored.

To reduce cost also on the sensor and readout chip side, the usage of 6" wafers (compared to 4" currently) and single-sided $n^+$-in-p sensors (compared to double-sided $n^+$-in-n currently) to optimize the obtained sensor area per handling and processing step is investigated in ongoing p-bulk sensor productions with different vendors. While single-sided processing would increase the number of potential vendors, there are still some concerns to investigate: due to the guard rings

PoS(VERTEX 2010)038

being on the pixel side, the bias voltage will be very close to the readout chip which could lead to discharges. Passivation schemes with a thin BCB[4] layer are currently being tested.

For the outer layers, a double-sided stave assembly of roughly $4 \times 4$ cm large sensors is under consideration that would carry $2 \times 2$ FE-I4.x[5] readout chips. It is conceived that the readout chips will not communicate with a module controller chip (MCC) as at present, but directly via a bus to an end-of-stave card (EOS). This would allow to choose the number of FE-I4.x per EOS according to the expected data rate per chip which is heavily dependent of the layer's radius and thus to optimize the necessary services.

A first prototype of an outer layer stave is being built within the *pixel stave 2010* programme to test mechanical, electrical and thermal properties of a carbon foam stave structure. While a low-density carbon foam is generally envisaged as stave basis, the facing type (carbon-carbon or no facing) and the position of the flex cable (internal or below modules) are under discussion. Fig. 6 displays the idea for the outer staves.

## 5. Other detector parts

While this paper focuses on the vertex detector upgrades, it should be noted that there are upgrades planned in almost every subsystem. As a strongly data-rate sensitive system, the trigger (TDAQ) will face major challenges. As long as it is possible to maintain the current sub-detectors' latencies, however, TDAQ upgrades can mostly be done without long access to the ATLAS detector which will therefore not require a long shutdown. The calorimeters will primarily aim for electronics upgrades allowing an improved level-1 trigger; in the forward region the insertion of a new, warm electromagnetic calorimeter is under discussion to prevent too much energy deposition in the liquid argon of the electromagnetic calorimeter – which *might* otherwise start to boil. In the muon system, a significant number of chambers might have to be replaced due to too high occupancies. These are caused mainly by cavern background which is very hard to simulate; hence decisions can only be taken after measurements have been taken with LHC running at the highest currently possible luminosity.

## 6. Summary

Following the LHC upgrade path towards sLHC, the ATLAS detector has defined upgrade plans for a *phase I* (up to $3 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$) and *phase II* (up to $5 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$). While some sub-detectors will be able to cope with the increased luminosity with just electronics upgrades, others will have to be replaced completely.

For *phase I*, it is foreseen to install an additional, innermost pixel layer (IBL) to improve the impact factor resolution and the b-tagging. The new pixel layer will also be capable of compensating any inefficiency of the current pixel b-layer due to radiation damage or data rate. R&D for the IBL is well advanced, the technical design report[10] is currently being written. In addition, the FTK, a hardware-based track finder and fitter, will be introduced to relieve the level-2 processor farm.

[4] Benzo-cyclo-Butene

[5] These readout chips will very likely be an interation of the currently developed FE-I4 IBL readout chip



PoS(VERTEX 2010)038

To cope with the luminosity of *phase II*, the complete replacement of the ATLAS vertex detector is necessary. Instead of the current arrangement of pixel detector, strip detector (SCT) and transition radiation tracker (TRT), a combination of pixel (subdivision in innermost layer(s) and outer layers) and strip (subdivision into short ($\sim$ 2.5 cm) and long($\sim$ 10 cm) strip) detectors will be installed. Technologies for the innermost pixel layer(s) are currently being investigated with promising results and there are already prototyping efforts ongoing for the short strip and outer pixel layers.

In addition to the replacement of the vertex detector, significant upgrades to the trigger/TDAQ, the calorimeters and the muon system are necessary.

PoS(VERTEX 2010)038

## References

[1] G. Aad et al. [ATLAS Collaboration], *The ATLAS Experiment at the CERN Large Hadron Collider*, JINST **3** (2008) S08003.

[2] F. Gianotti et al., *Physics potential and experimental challenges of the LHC luminosity upgrade*, Eur. Phys. J. C **39** (2005) 293 [arXiv:hep-ph/0204087].

[3] G. Aad et al. [ATLAS Pixel Collaboration], *ATLAS pixel detector electronics and sensors*, JINST **3** (2008) P07007.

[4] A. Abdesselam et al. [ATLAS SCT Collaboration],*The integration and engineering of the ATLAS SemiConductor Tracker barrel*, JINST **3** (2008) P10006.

[5] E. Abat et al. [ATLAS TRT Collaboration], *The ATLAS TRT barrel detector*, JINST **3** (2008) P02014.

[6] M. Lamont, *LHC near and medium term prospects*, in proceedings of *Physics at the LHC 2010*.

[7] I. Peric et al., *The FEI3 readout chip for the ATLAS pixel detector*, NIM A **565** (2006) 178.

[8] M. Barbero et al., *A new ATLAS pixel front-end IC for upgraded LHC luminosity*, Nucl. Instrum. Meth. A **604** (2009) 397.

[9] I. Dawson and L. Nicolas, `https://twiki.cern.ch/twiki/bin/view/Atlas/RadiationBackgroundSimulations`.

[10] The ATLAS collaboration, *ATLAS Insertable B-Layer Technical Design Report*, CERN, 2010, to be published.

[11] A. Annovi *et al.*, *The fast tracker architecture for the LHC baseline luminosity*, in proceedings of *The 2009 Europhysics Conference on High Energy Physics*, PoS(EPS-HEP 2009)136.

[12] R. Brenner., *ATLAS upgrade track trigger*, these proceedings.

[13] G. Casse et al., *Charge multiplication in highly irradiated planar sensors, measurements and simulation*, these proceedings.

[14] G. Kramberger et al., *Edge TCT Measurements*, these proceedings.

[15] J. Lange et al., *Charge Multiplication Properties in Highly-Irradiated Epitaxial Silicon Detectors*, these proceedings.

[16] A. Kok et al., *Fabrication of 3D Silicon Detectors*, these proceedings.

[17] C. Fleta Corral et al., *Laboratory and Testbeam Results on 3D Detectors*, these proceedings.

[18] M. Mikuz et al., *Diamond Detectors*, these proceedings.

[19] N. Hessey et al., *Gaseous Pixel Detectors (Gossip and GridPix) for the ATLAS Inner Tracker at the sLHC*, ATLAS Upgrade R&D proposal, `https://edms.cern.ch/document/808572/1`

[20] P. Pangaud et al., *ATLAS pixel 3-D design using two tiers of electronics*, these proceedings.

[21] D. Muenstermann, *R&D on Planar Pixel Sensor Technology for the ATLAS Inner Detector Upgrade (PPS Proposal)*, CERN, `https://edms.cern.ch/document/966140`.

PoS(VERTEX 2010)038