PROCEEDINGS OF SCIENCE

NA62 Gigatracker

Alexander Kluge*
CERN, CH-1211 Geneva 23, Switzerland
E-mail: Alexander.Kluge@cern.ch

G. Aglieri Rinella[a], V. Carassiti[c], A. Ceccucci[a], E. Cortina[d], J. Daguin[a], G. Dellacasa[b], M. Fiorini[a], S. Garbolino[b], P. Jarron[a], J. Kaplon[a], F. Marchetto[b], E. Martin[d], A. Mapelli[a,f], G. Mazza[b], M. Morel[a], M. Noy[a], G. Nüssle[d], P. Petagna[a], L. Perktold[a], F. Petrucci[c,e], A. Cotta Ramusino[c], P. Riedler[a], A. Rivetti[b], R. Wheadon[b]
[a]CERN, Geneva Switzerland, [b]INFN Torino, Italy, [c]INFN Ferrara, Italy, [d]UCL Louvain la Neuve, Belgium, [e]University Ferrara, [f]EPFL Lausanne Switzerland

The Gigatracker is composed of three hybrid pixel detectors in the rare kaon decay experiment, NA62, at CERN, to be installed by the end of 2012. Each station consists of pixel detectors with 18000 300 μm x 300 μm pixels. In order to suppress background events the Gigatracker measures the arrival time of particles with a time binning of 100 ps. Particle hits are then correlated with the signals of a ring imaging cherenkov detector in the experimental setup . The system is operating in vacuum at a temperature of 5 °C or below. Expected radiation levels are $\approx 10^5$ Gy and 2 x 10^{14} 1 MeV neutron equivalent per cm^2 over 100 days of operation. This paper describes the detector system, two alternative read out demonstrator ASICs and two cooling options which are considered for final implementation.

19th International Workshop on Vertex Detectors
June 6 -11 2010
Loch Lomond, Scotland, UK

*Speaker.

PoS(VERTEX 2010)040

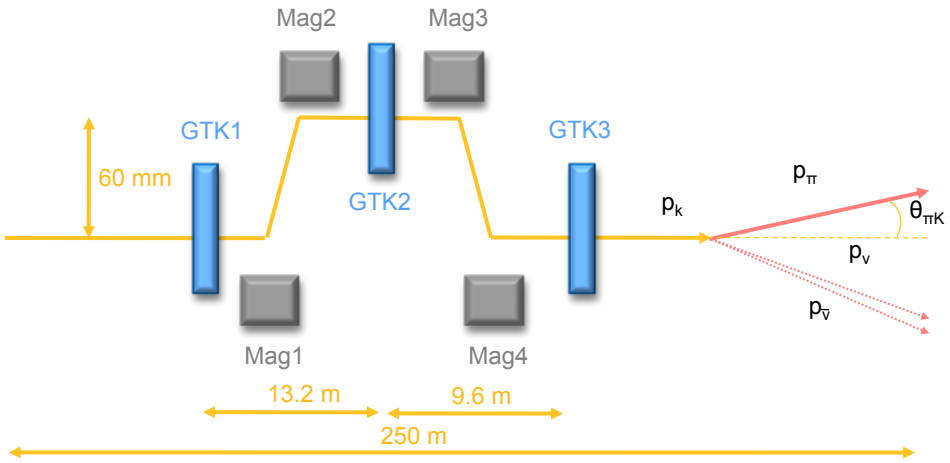

Figure 1: GTK configuration and illustration of decay.

1. Detector Introduction

The Gigatracker (GTK) is a hybrid pixel detector composed of three pixel planes in the rare kaon decay experiment, NA62, at CERN [1]. It is a spectrometer that provides precise measurements of momentum, time and angle of the incoming 75 GeV/c kaon beam. Fig. 1 shows the GTK setup in the beam line with four achromat magnets, deviating the beam for the momentum measurement. On the right side of the illustration the kaon decaying into one pion, one neutrino and one anti-neutrino is shown.

The GTK measures the momentum with a relative resolution of $\sigma(p_K)/p_K \approx 0.2$ % and the outgoing polar angle with a resolution of ≈ 16 μrad using 300 μm x 300 μm large pixels. To meet the resolution requirements the beam spectrometer is installed in vacuum with a minimal amount of material crossed by the beam to preserve the beam divergence and to limit beam hadronic interactions. At the end of the NA62 experimental setup a ring imaging cherenkov detector (RICH) detector identifies decay pions. Hits from the RICH and the GTK are matched in arrival time to suppress kaons which have not decayed in the NA62 vacuum tank. Thus the GTK also measures the arrival time for each particle of the beam. Due to the high particle rate of 750 MHz, the specification for the time resolution for the background separation on every single track using all three stations is 150 ps (rms) or below. A maximum time resolution requirement of 200 ps per station has been set. However, the hardware development aims for values below that. The TDC bin in the read-out application specific integrated circuit (ASIC) has been set to 100 ps.

Each station is made of one hybrid silicon pixel detector with a total sensor size of 29.3 mm x 63.1 mm containing 18000 pixels arranged in a matrix of 90 x 200 elements. With this configuration the detector matches the expected beam dimensions of $\approx$ 60 mm x 27 mm. The amount of material crossed by the beam at each station influences the angle measurement. The total amount of material per station has been required not to exceed 0.5 % X_0. The beam region is completely covered by one single, fully active silicon sensor bump-bonded to 2 x 5 read-out chips. Fig. 2 shows the intensity distribution in the highest rate station 3. The expected fluence for a typical 100 days

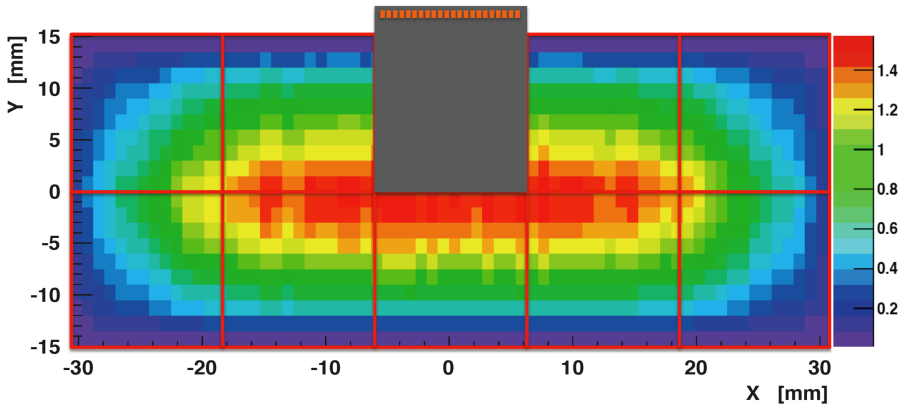

Figure 2: Beam intensity in station 3 and ASIC configuration

run time year is 2 x 10^{14} 1 MeV neutron equivalent per cm^2 in the central region of the sensor. This value is comparable to those expected in the inner layers of the LHC trackers over ten years of operation and requires the sensors and the application specific integrated circuits to cope with the high radiation environment. In order to reduce the radiation induced leakage current on the relatively large sensor the operating temperature is set to 5°C or below. The very low mass of the detector, the operation in vacuum and the need of limiting the leakage current increase due to radiation damage demands a very efficient and reliable cooling system.

The ASICs are accessed only from the top or the bottom of the assembly. Thus wire bond connections to the read-out chip are placed only on one side of the ASIC. The active pixel matrix extends to the other 3 sides of the chip. That way no additional material to connect the ASICs is placed inside the active beam area. The pixels which are connected to the border of the read-out ASICs are made wider to cover the area between the ASICs and maintain geometrical coverage.

Table 1 summarizes the specifications. The combination of high particle rate, the output data rate of up to 6 Gbit/s per chip, the time binning of 100 ps, and the low material budget of 0.5 % X_0 present a novel challenge for the implementation of a pixel detector. The p-in-n silicon sensor thickness has been studied in simulation, and an overall thickness of 200 μm was found to be compatible with the signal requirements for precise timing information together with the material budget constraints. The silicon assembly of the sensor and read-out ASIC thinned down to 100 μm without cooling amounts to 0.33 % of a radiation length X_0.

2. Pixel Application Specific Integrated Circuit ASIC

The implementation of the read-out ASIC is demanding as the read-out data rate of up to 6 Gbit/s and the corresponding digital activity on the ASIC must not degrade the performance of the time stamping sensitive front-end. Crucial for the implementation is an effective separation of the analog and digital domain. Two principles are being considered for this implementation. Simulations cannot show which of the two approaches can deliver a more robust design. Thus two demonstrator 130 nm CMOS technology ASICs have been implemented and are discussed in the following sections.

Parameter	
Number of pixels per chip	1800 = 45 x 40
Size of pixels	300 μm x 300 μm
Active area per chip	12 mm x 13.5 mm = 162 mm^2
ASIC design time binning	100 ps
Sensor size	27.0 mm x 60.8 mm = 1641.6 mm^2
Thickness of sensor	200 μm
Type of sensor	p in n
Thickness of read-out chip	100 μm
Dynamic input range	0.7 - 10 fC, 5000 - 60000 electrons
Design particle rate per chip	105 MHz
Rate of center pixel	114 kHz
Rate of center column	2.7 MHz or 0.66 MHz/mm^2
Average rate per pixel	58 kHz
Max. dead time	1 % (2 % in beam center)
Data transfer rate per chip	6 Gbit/s
Total dose in 1 year	6 x 10^4 Gy
Neutron flux in 100 days	2 x 10^{14} 1 MeV neutron equivalent cm^{-2}
Max. Material budget/thickness	0.5 % X_0 per station
Operating temperature	-20 to 5 °C
Operating vacuum	10^{-6} bar

Table 1: Minimum GTK system requirements.

2.1 End-of-column architecture

2.1.1 End-of-column description

Fig. 3 shows a block diagram of the final EOC chip architecture [2]. The EOC option employs simple pixel cells containing the amplifier, time-over-threshold (ToT) discriminator and a transmission line driver per pixel cell, which sends the discriminated signal to the EOC region of the chip. There a delay locked loop (DLL) based TDC [3] [4] time tags the rising and falling edge of the discriminator signal with a time bin of 100 ps. The leading edge time stamp provides information of the hit arrival time and the trailing edge provides input charge amplitude information used to correct time walk. At the time of the leading edge, a synchronous coarse clock counter value is latched to increase the dynamic range of the TDC to 12.8 μs. In the chip 5 pixels in a column are multiplexed together and connected to one TDC using a combinatorial hitArbiter circuit. Simulation shows that the hit efficiency for the worst-case centre column stays above 99.5 %. Pixel hit addresses and rising and falling time tag words are sent to a buffer FIFO before the data are serialized and sent out of the chip. In this architecture no clock signals are distributed over the clock matrix, reducing possible interference with the analog electronics and data are only transmitted to the EOC circuits once a hit has been registered. The digital processing and transmission units are geographically separated from the analog front-end electronics. However, each discriminator signal needs to be sent to the EOC area without degradation of the timing information. Both the DLL and the read-out

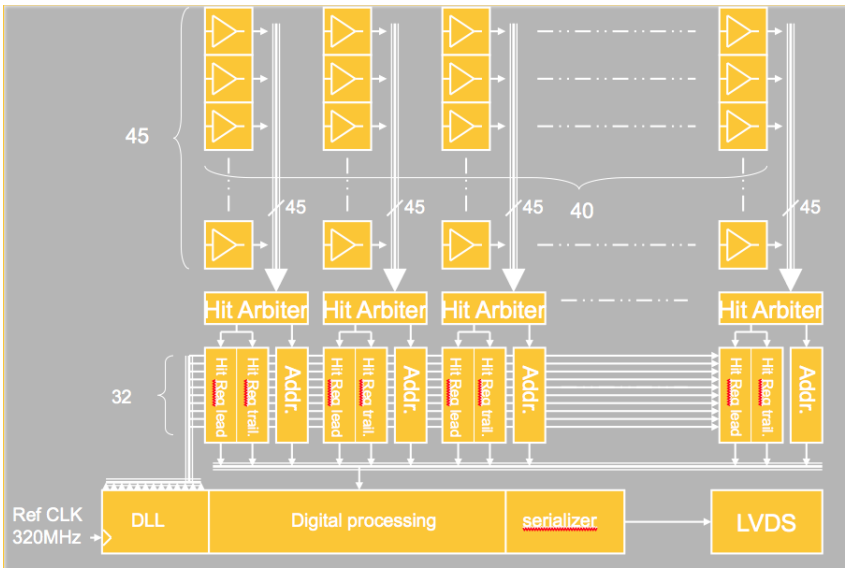

Figure 3: EOC architecture block diagram

are operated with a 320 MHz clock.

The demonstrator contains one full 45 pixel column arranged in an S-shape to save silicon area. In addition to this column, test structures with 15 pixels have been included for the characterization of the analog pixel cell. The homogeneity of the pixel matrix will be evaluated. This demonstrator serves experimentally as proof of principle for the entire chain from analog pixel input, via the amplification stages and discriminator to the transmission line amplifier, transmission line and receiver, the hit arbiter logic and the TDC. The implementation of the individual blocks is as for the final chip. The layout of the EOC circuits largely follows the 300 μm pitch defined by the width of the column. The data encoding and read-out from the TDC has been simplified as the implementation is straightforward. The demonstrator is organized in such a way that the 45 pixel column feeds a set of 9 hit arbiters and 18 hit registers connected to one DLL. Rising and falling edge hit registers of the 9 pixel groups are read out using 9 x 320 MHz serializers independently. In order to asses the influence of digital noise on the DLL and analog parts, the read-out clock can be switched on and off for each of the 9 streams independently. A set of 9 test pixels is connected to a second instance of the EOC column logic and operates independently. Test outputs along the processing chain allow qualification of individual blocks.

2.1.2 End-of-column test results

A fully automated test system based on an FPGA processor board has been setup. The setup allows the injection of charge pulses into each of the 60 pixels on the chip. The injected charge can be varied from 0.7 fC to 10 fC, the injection time can be swept with respect to the 320 MHz master clock in steps of 10 ps and the time duration of the charge injection into the front-end can be varied from 2.5 ns to 6 ns. The system is programmable, data points are stored automatically and are analyzed off-line.

In the following section results for the EOC demonstrator are shown. At the moment all measurements with exception of noise and gain studies have been performed without the sensor bump bonded to the read-out ASIC. Further information can be found in [5].

Front-end performance

The equivalent noise charge of the front-end without sensor is 130 electrons and with the sensor connected is 180 electrons. These values are in accordance with simulations and have been measured by evaluating directly the output of the pre-amplifier and by evaluation of the width of the turn-on S-curve. Fig. 4 (bottom right) shows an s-curve of the read-out ASIC bump bonded to the silicon assembly. The time walk and time-over-threshold duration can be seen in fig. 4 (top left). t_1 and t_2 stand for the first and second crossing of the threshold respectively. Fig. 4 (top right and bottem left), gives the jitter on t_1 and t_2 for several thresholds over the input charge. The t_1 jitter for the most probable input charge of 2.4 fC is below 55 ps. T_2 jitter values are about double the value which can be explained by the shallower signal shape of the shaper signal after the peak. These jitter values do not contribute equally to the time walk compensated jitter, but the t_2 jitter contribution needs to be weighted by the gradient of the time over threshold t_2-t_1 and t_1. The maximum time walk is 2.2 ns and the variation of the time-over-threshold signal duration is 7 ns peak-to-peak. The ratio between these to numbers is around 1/3.3.

Time-to-digital-converter (TDC)

The TDC measurements have been done by bypassing the analog front-end and injecting digital pulses on test inputs directly to the TDC. The TDC works at the nominal 320 MHz frequency, but has been tested successfully even up to 450 MHz. Fig. 5 shows the differential and integral non-linearity giving values of 0.17 and 0.27 of an LSB of 98 ps. It should be noted that in this application all TDCs are fully calibrated. Thus the effects of the integral non-linearity can be compensated for off-line. The jitter of the TDC is 10 ps rms.

Full chain measurements

The full chain measurements have been conducted by injecting charge to the front-end and evaluating the time code of leading and trailing edge coming from the output serializers. That means that the entire front-end, the transmission line driver, the transmission line, its receiver, the TDC and the digital read-out are included in these measurements. The t_1 and t_2 time tags have been analyzed and corrected providing a measure of the final time resolution. The time resolution in this application is composed of a systematic error given by the remaining time walk correction error and the random error of all components involved expressed as jitter. In order to assess the full chain resolution these two values need to be combined.

The measurement has been done in such a way that the input signal delay with respect to the clock has been swept from 0 to 3.13 ns over the whole clock period in steps of 10 ps. For each of these time sweep offsets the input charge has been varied and the time-walk compensation has been applied. Fig. 6 (top left) shows the time walk after compensation, t_0, for a selected time offset of 1000 ps after the rising edge of the TDC clock. The error bars on the corrected time of the input charge correspond to the weighted sum of the full chain jitter of t_1 and ToT pulse width t_2-t_1. In order to assess the quality of the compensation a histogram with the deviations from the expected time value has been filled for all delay offset from 0 to 3.125 ns. Fig. 6 (bottom left) gives this histogram of the t_0 residuals averaged over all phases and charges. The RMS width of the distribution is 10 ps corresponding to the systematic uncertainty added by the time walk

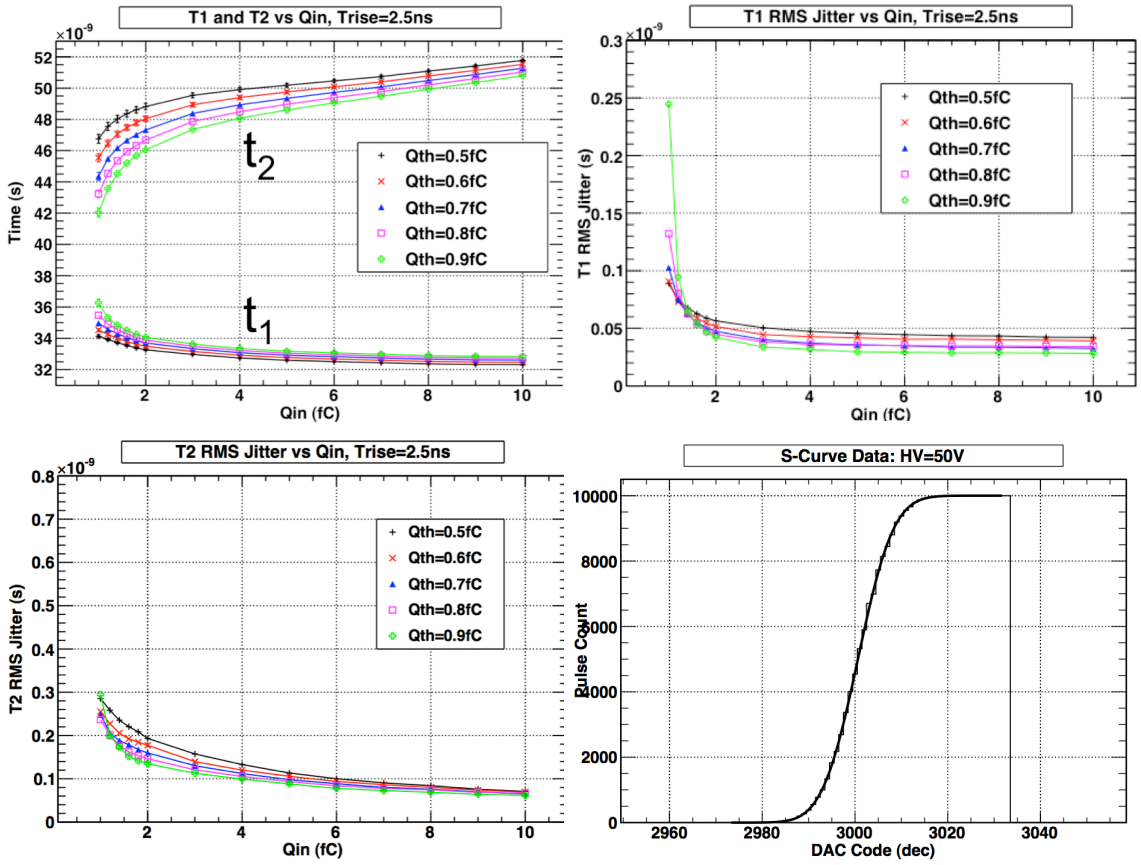

Figure 4: Top left: Analog front end response for t_1 and t_2 over input charge for 2.5 ns input charge injection duration. **Top right:** t_1 rms jitter versus input charge for several thresholds and input signal charge injection duration of 2.5 ns. **Bottom left:** Analog front-end t_2 rms jitter over input charge for several threshold values and input signal charge injection duration of 2.5 ns. **Bottom right:** Turn-on S-curve for a read-out ASIC bump-bonded sensor.

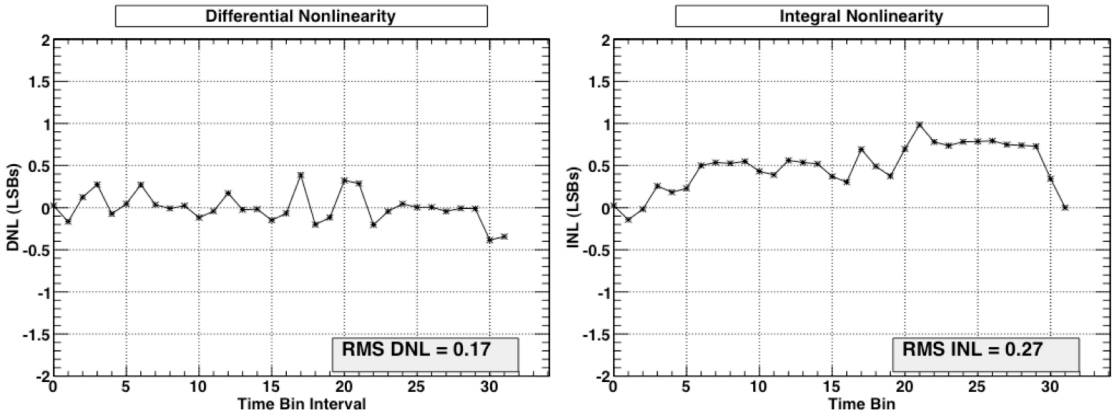

Figure 5: TDC differential (left) and integral (right) non-linearity.

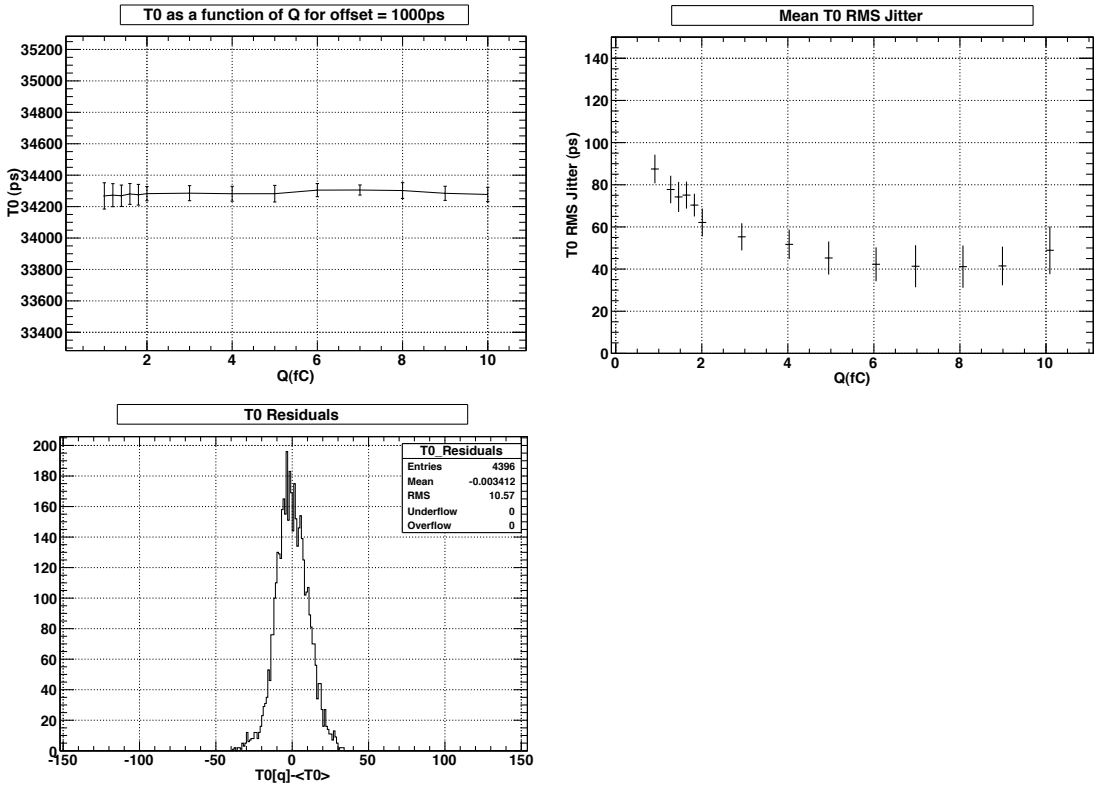

Figure 6: Top left: Full chain time walk t_0 after compensation. **Top right:** Jitter t_0 or time walk correction error measured with electrical test pulses. **Bottom left:** t_0 residuals for all phase offsets and all charge measurement points.

compensation. Fig. 6 (top right) shows the jitter on t_0 from actual measurements with electrical test pulses. The mean error on the t_0 measurements for the most probable charge of 2.4 fC is around 60 ps.

One of the critical issues in the EOC architecture is the transmission of the discriminator signals along transmission lines to the EOC area. The furthest pixel is 12 mm from the transmission line receiver. In order not to degrade the jitter performance by shallow rise times at the end of the transmission line the driver boost the edges with pre-emphasis circuits. The jitter versus the distance from the EOC area was evaluated and no significant trend was found. That means that the transmission of the discriminator signals does not contribute to the overall jitter.

2.2 TDC in Pixel option

2.2.1 P-TDC description

The other ASIC implementation option is based on pixel cells which contain one pre-amplifier, one constant fraction discriminator to compensate for time walk and one TDC in each cell. This way each pixel cell time tags independently the hit arrival time and sends only digital and thus signals more immune to noise to the EOC area of the chip. However, the clock for the read-out control and for the precision TDC in each cell needs to be transmitted all over the pixel matrix.

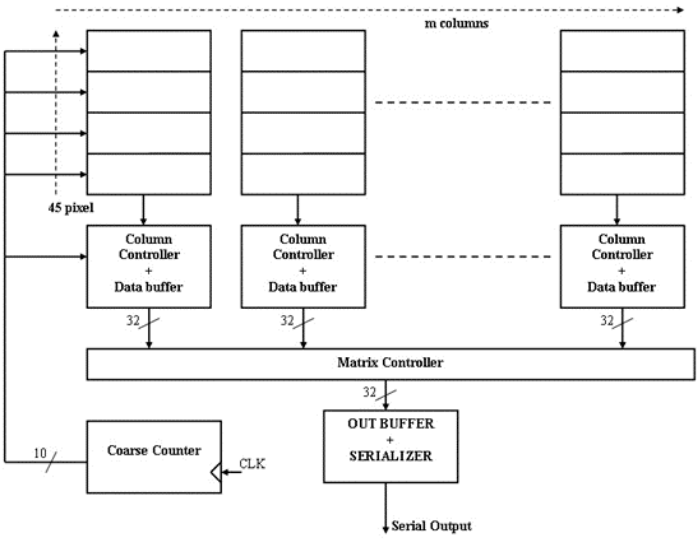

Figure 7: Block diagram of the P-TDC option.

In the P-TDC most of the signal processing, including time to digital conversion and multi-event buffering, is performed inside each pixel. Fig. 7 shows a simplified block diagram of the P-TDC architecture. Each column, 45 pixels, is read-out by a dedicated controller. The data are then merged and prepared for the output serializer.

The time walk error is corrected at the analog level with a constant fraction discriminator (CFD). The master clock of the chip has a design frequency of 160 MHz. The clock pulses are counted and the resulting word is Gray-encoded and sent to all pixels. When a hit is flagged by the CFD, the value present on time-stamp bus is latched into local registers, providing a first coarse estimation of the event time. In each pixel, a TDC based on a Time to Amplitude Converter (TAC) generates a voltage proportional to the interval between the hit and the next clock edge by charging a capacitor with a constant current source. The resulting voltage is then digitized, providing the required fine time measurement.

The analog section can be divided into three main blocks: the front-end amplifier, the CFD and the TDC. In order to minimize the risk of digital noise pick-up a fully differential topology is used for both the front-end amplifier and the CFD. In each pixel, a TDC based on a Time to Amplitude Converter (TAC) generates a voltage proportional to the interval between the hit and one of the clock edges by charging a capacitor with a constant current source. The resulting voltage is then digitized, providing the required fine time measurement. The ADC employs a Wilkinson topology: the capacitor of the TAC is discharged by a small current and the clock pulses necessary to restore the baseline are counted. The time needed for the fine time measurement may reach up to 1 μs in the worst case. Since the maximum expected rate per pixel is 140 kHz, a multi-buffering scheme is mandatory and it has been implemented with two FIFOs, one analog and one digital. The digital FIFO allows the storage of up to four values of the coarse counter, while the analog one, formed by four capacitors, accommodates the corresponding fine time measurements.

The digital section of the pixel is composed of the digital FIFO that stores the coarse counter

values, the logic controlling the TAC, the TDC and the interface to the End of Column readout. One of the possible drawbacks of the P-TDC option is that the many digital gates in the pixel are directly on the beam trajectory. The protection against Single Event Upset is therefore a primary concern and is addressed through the systematic use of Hamming encoding.

The key goal of the design of a P-TDC demonstrator ASIC was to have a chip as complete as possible, so that all the critical issues associated to this option could be evaluated and a future extension to a larger, final ASIC could be done with a minimal risk. The digital circuitry that merges the data coming from different columns and generates the serial output stream has not been included in this version.

The prototype ASIC contains two long columns with the final number of pixels (45) and one short column with 15 pixels. Two spare pixels are provided for debugging purposes. In order to have an acceptable form factor, the long columns have been folded in three segments.

At the time of the publication the tests on the P-TDC architecture have been started but the test system is not yet fully developed. The general functionality of the ASIC has been successfully tested. Tests using electrically injected pulses, laser test pulses and beam tests are foreseen to qualify the P-TDC option.

3. GTK cooling

The main specifications for the implementation of the GTK cooling are an electronics power dissipation of 32 W per station and a maximum operation temperature of 5 °C, however, an operation temperature of −20 °C is aimed at, as the operation lifetime of a module increases from 50 days when operated at a temperature of 5 °C to 100 days when operated at the cooler temperature of −20 °C. The degradation of the module performance is due to the increase of the sensor leakage current when exposed to radiation. The cooling must withstand the high radiation levels and must be compatible with the low overall maximum material budget of 0.5 % X_0.

Two cooling options are under consideration. One employs liquid cooled micro-channels in a silicon base plate to which the silicon assembly is mechanically and thermally connected. The other option is based on a 100 K cold gaseous nitrogen flow in a metallic vessel with Kapton openings.

In the following sections the options are described briefly.

3.1 Micro-channel cooling

Micro-channel cooling has created industrial interest as a compact way to dissipate high heat loads of several hundreds of W/cm^2 [6]. The idea is to apply the industrial principles but reducing power dissipation by a factor of 100 and at the same time reducing the material thickness. A silicon base plate carries micro channels with the dimensions in the order of 100 μm x 100 μm. A second silicon plate is bonded onto the base plate and acts as cover of the channels. Cooling fluid is circulated through micro connectors. Full size prototypes have been made to optimize the cooling performance and develop the manufacturing process to achieve a total silicon thickness of 150 μm (0.18 % X_0) or less.

The prototype cooling plates are illustrated in Fig. 8. The left image shows the cooling wafer with a heating foil to emulate the electronics heat load. On the right image, the other side of the cooling wafer with two micro connectors is shown. The prototypes are designed according to

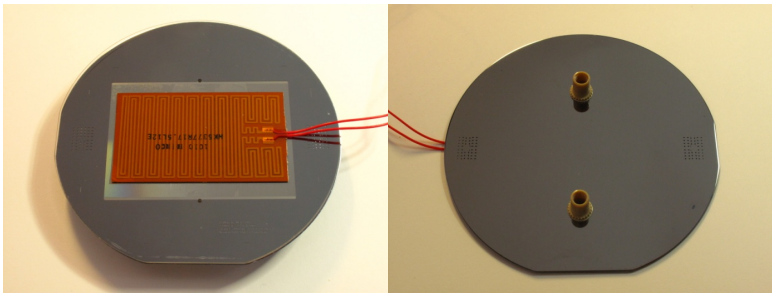

Figure 8: Prototype micro channel cooling devices.

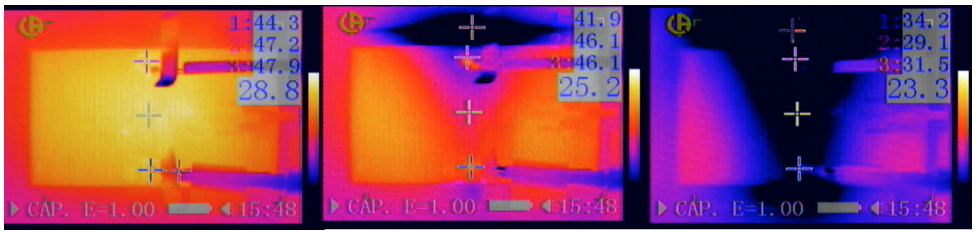

Figure 9: Thermal images of full scale prototype during startup; dummy head load with no cooling (left), image taken when cooling starts (middle), image taken after a few seconds of cooling flow (right). In each image at the top right the small numbers correspond to the temperature at the three aligned crosses. The larger number indicates the minimum temperature in the image.

the results obtained from computational fluid dynamics (CFD) and structural strength simulations. Ongoing development efforts aim to manufacture thin micro-channels allowing a minimal plate thickness and an effective manifold to evenly distribute the cooling fluid, C_6F_{14}, while keeping the pressure drop between inlet and outlet at practicable level. Structural simulations reproduce well the mechanical failure with increasing pressure. The devices currently under test have a cooling area of 50 x 60 mm^2. They consist of an array of 100 x 100 μm^2 parallel channels, 48 mm long, separated by silicon walls of 25 μm thickness . Two 100 μm deep rectangular distribution manifolds of 60 x 1 mm connect all the micro channels together at both ends and allow for fluid distribution from the inlet and outlet holes. Injection and collection of fluids is performed through capillaries screwed into a micro connector placed at the centre of each manifold. Fig. 9 shows thermal images taken with an IR camera of the full scale prototype during startup of the cooling system. It can be seen that cooling channels heated by heating foils (rectangular shape in the left image) are successively cooled down when the micro channels are filled the with cooling fluid, C_6F_{14} (middle and right image). In the left images the dummy thermal load is turned on and no coolant is circulating. The middle images was taken when the the coolant started flowing. The right image was taken after a few seconds of circulation when the temperature of the dummy load was lowered by more than 15 °C.

3.2 GTK gas cooling

The other cooling option is the construction of a vessel housing the GTK module and cooling

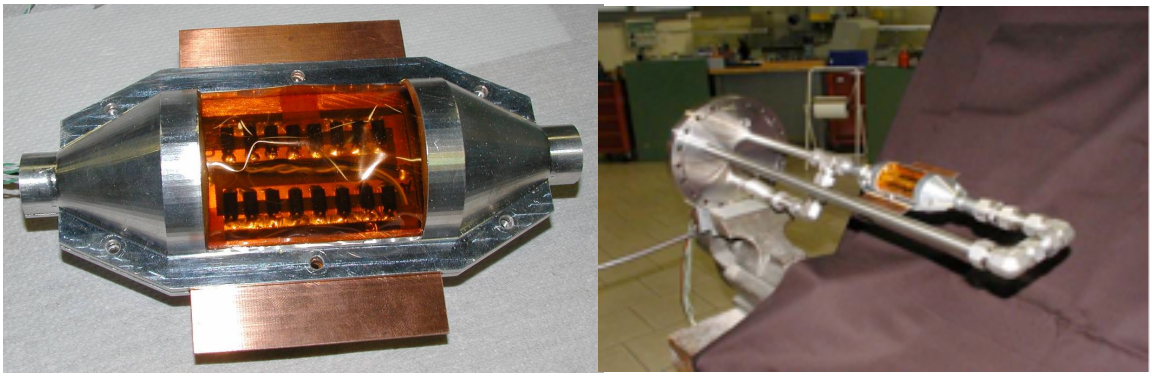

Figure 10: Full scale gas cooling prototype (left). Full gas cooling prototype circuit.

it via a flow of cold gaseous nitrogen. The nitrogen will enter the vessel at a temperature of 100 K. The cold flow will keep the operation temperature of the module below 5 °C. Fig. 10 shows a full scale prototype. In this design the GTK is installed between two cylindrical Kapton walls, 40 μm thick, supported by an aluminum frame. A second pair of thinner (10 μm) Kapton walls is inside the vessel surrounding the sensor/ASIC assembly, providing a smooth gas flow over the detector surface. The total thickness crossed by the beam is (2 x 40) + (2 x 10) = 100 μm Kapton. The radiation length for this polymide film $(C_{22}\ H_{10}\ N_2\ O_5)_m$ is 28.6 cm, therefore the total material budget of the vessel is 0.035 % X_0. The detector assembly is electrically connected to a carrier printed circuit board, which provides power and signal connections. However, the assembly is thermally decoupled from the carrier board; the sliding support compensates for the different thermal expansion coefficients of the materials.

A structural analysis has been performed and gives low mechanical stress values (less than 2 MPa) and displacements both for the vessel and the detector. The simulation and calculations give a breaking pressure for 50 μm thick Kapton foils of 0.49 MPa (4.9 bar). Destructive tests confirmed these values. Considering a nominal pressure inside the vessel of 2 bar, the safety factor is 2.5. A full cooling system prototype was setup. In the test the nominal thermal detector dissipation of 32 W was emulated by electrical resistors. The test show that a temperature uniformity better than $\approx$ 2 °C was achieved with a 7m^3/h flow rate.

4. Electro-mechanical integration

Each of the three GTK stations will be installed inside a dedicated vacuum vessel at three different positions along the NA62 experiment beam line. Due to the radiation damage in the sensors, the modules need to be replaced on a regular basis. The electro-mechanical integration is based on the principle that one GTK module, the assembly and its services, is an integral and compact component, which can be inserted and removed with a minimal intervention in the vessel. The Gigatracker assembly carrier is a printed circuit board that supports mechanically the assembly and provides all power supplies, control and differential read-out signal connections. It carries optical components outside the vacuum vessel and acts as vacuum feed-through for the electrical lines and the cooling connections. Fig. 11 (left) shows a drawing of the GTK assembly carrier and

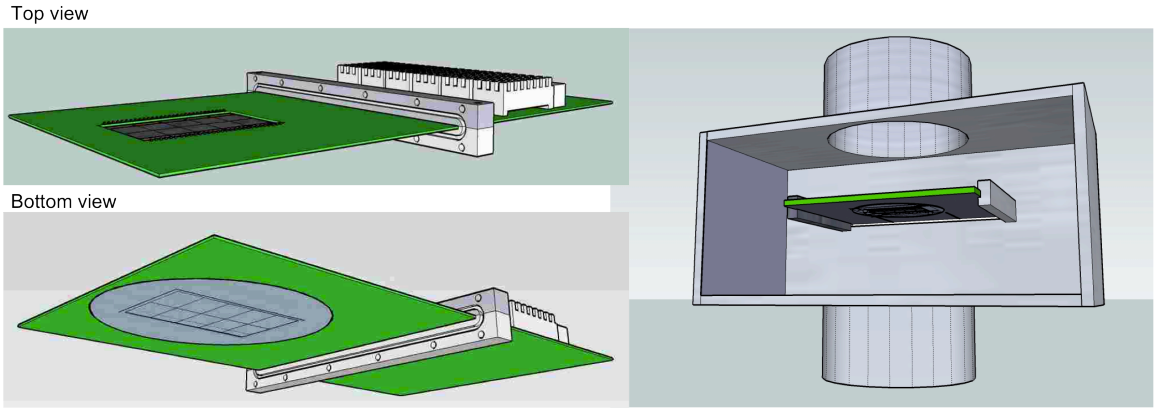

Figure 11: GTK module with assembly carrier (left). GTK vacuum vessel with inserted GTK module.

the GTK vacuum vessel. On the left hand side the assembly carrier printed circuit board has an opening for the sensor assembly. In the middle a flange with an O-ring is tightly glued around the PCB acting as vacuum feed-through. On the right hand side optical components, already outside the vacuum, are placed. Fig. 11 (right) shows the module inserted in the vessel. In order to avoid the need of a precise pitch adapters for the wire bond connection to the printed circuit board, a staggered wire bonding scheme is proposed where the pitch in the PCB does not need to match the ASIC pitch of 73 μm. The cooling connections will be integrated in the flange (not shown in the figure). More details can be found in [7].

5. Summary

The NA62 GTK is composed of three hybrid pixel detector stations. Each station contains 18000 pixels of 300 μm x 300 μm size. The arrival time of the hits in each pixels is time tagged with a resolution of 200 ps rms or better. Each station has a material budget of 0.5 % X_0 or better. The development of all components is currently under way. P-in-n sensors of the size 27.0 mm x 60.8 mm with 18000 pixels are bump bonded to 2 rows of 5 read-out chips covering the entire beam area. Two demonstrator ASICs have been manufactured. For the EOC demonstrator the electrical test results without the sensor bonded give a full resolution of 60 ps for the most probable charge of 2.4 fC. The front-end noise without sensor is 130 electrons equivalent noise charge and 180 electrons with the sensor bonded. The P-TDC ASIC option is functionally working but full characterization is underway. The GTK is in vacuum and subject to high radiation dose which require a reliable but light material cooling solution in order to increase the lifetime of the module. Two options are under consideration; a silicon base plate with integrated micro-channels and a 100 K nitrogen gas cooling. Both solutions are investigated and full scale prototypes show promising results. The electro-mechanical integration and module design is driven by the need to exchange the module on a periodic basis after 50 to 100 days. An integration concept has been designed allowing a fast replacement with automatic mechanical alignment.

References

[1] Anelli, G., et al., Proposal to measure the rare decay $K^+ \rightarrow \pi^+ \nu\bar{\nu}$ at the CERN SPS, CERN-SPSC-2005-013.

[2] Jarron, P., et al. Pixel Read-Out Architectures for the NA62 GigaTracker, Proceedings of the Proceedings of the TWEPP 2008-09-26, Topical Workshop on Electronics for Particle Physics 2008.

[3] Mota, M., Christiansen, J., A High-Resolution Time Interpolator Based on a Delay Locked Loop, IEEE Journal of Solid-State Circuits, Vol. 34, No. 10, Oct. 1999, pp 1360-1366.

[4] Mester, C., A multi-channel 24.4 ps bin size Time-to-Digital Converter for HEP applications, Proceedings of the TWEPP 2008-09-26, Topical Workshop on Electronics for Particle Physics 2008.

[5] Noy, M. et al., Characterisation Of The NA62 GigaTracker End Of Column Readout ASIC, to be submitted to Proceedings of Topical Workshop on Electronics for Particle Physics 2010, JINST.

[6] B. Agostini et al., State of the Art of High Heat Flux Cooling Technologies, Heat Transfer Engineering, Volume 28, Issue 4 April 2007, pg 258 - 281.

[7] Morel, M. et al., The electro-mechanical integration of the NA62 Giga Tracker time tagging pixel detector, to be submitted to Proceedings of Topical Workshop on Electronics for Particle Physics 2010, JINST.